AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

1.8-in COLOR TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A M - 1 2 8 1 6 0 H 8 T N Q W - 0 0 H
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2006/5/26	-	New Release	Eric
2006/8/10	-	Rename TF176220-62-0 to AM-128160H8TNQW -00H and revised all T.B.D data.	John
2006/12/12	4	Change the temperature range on page 4.	John
2007/2/22	7	Change the View angle on page 7	John

1 Features

Main LCD 1.8 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments. The Main-LCD adopts one backlight with High brightness 2-lamps white LED.

(1) Construction: 1.8” a-Si color TFT-LCD with White LED Backlight and FPC.
(2) Main LCD : 2.1 Amorphous-TFT 1.8 inch display, transmissive, Normally white type, 12 o’clock.
2.2 128(RGB)X160 dots Matrix,1/160 Duty.
2.3 LCD controller is HX8310 or Equivalent.
2.4 Real 262K colors display:
65K: Red-5bit, Green-6bit, Blue-5bit (16-bit interface)

(3) 8-bit high speed bus interface and high speed RAM-write function.
(4) Direct data display with display RAM.
Main LCD Internal RAM capacity: 46,080bytes
(5) MPU interface: 8 bits 80-serise parallel interface is available.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 34.0 (W) x 63.93(H) x 3.55 (D) Max.	mm
Main LCD	Pixel pitch	0.222 (W) x 0.222(H)	mm
	Active area	28.416 (W) x 35.52 (H)	mm
	Viewing area	29.816 (W) x 36.92 (H)	mm
Weight		Approx. 6.7	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power Supply for Logic	VDD – GND	-0.3	+4.6	V	
Power Input Voltage	Vci	-0.3	+4.6	V	
Power Supply for LED backlight	LED A – LED K	-0.5	+7.2	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80°C Min. –30°C	Note 1: Non-condensing
Operating temperature	Max. +70°C Min. -20°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCD

(V_{DD}=2.8V, Ta=25 °C)

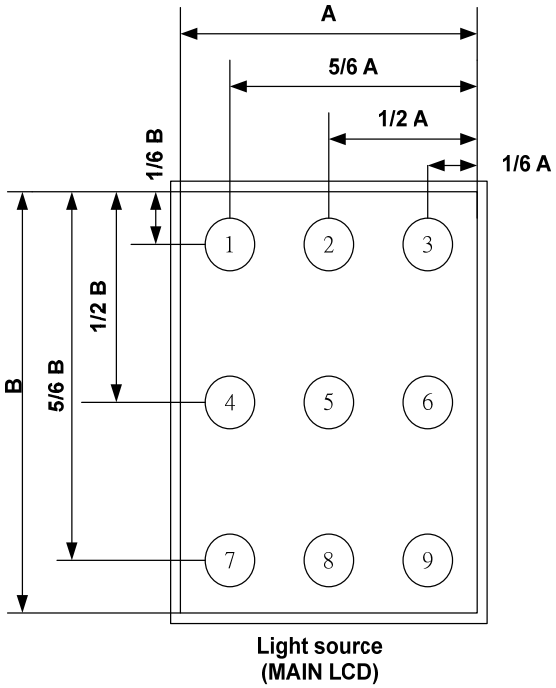
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.2	2.8	3.3	V
Power input voltage	Vci		2.5	-	3.3	V
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I_{DD}		-	2.5	4	mA
Consumption current of LED	I_{LED}	V_{LED}=6.8V	-	15	20	mA

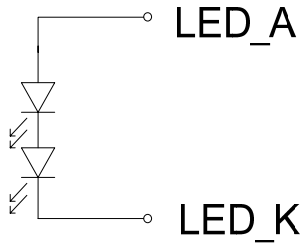
※ 1. 1/160 duty

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =15mA	-	6.8	7.2	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	2-chip serial	12	15	20	mA
Power Consumption	P_{BL}	I_f =15mA	-	102	-	mW
Uniformity (with L/G)	-	I_f=15mA	80%*1	-	-	
Luminous color	White					
Chip connection	2 chip serial connection					

Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

Driving codition:1/160 Duty

LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	-	15	30	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	-	30	50		
Contrast ratio	CR	25°C	150	200	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	7.5	-	%	
Visual angle range front and rear	θ	25°C	(θf)15 (θb)35			De-gree	φ = 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 45 (θr) 45			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			150			Cd/m2	V_{LED}=6.8V, 15mA Full White pattern

5-2 CIE (x, y) chromaticity (1/160 Duty Ta = 25°C)

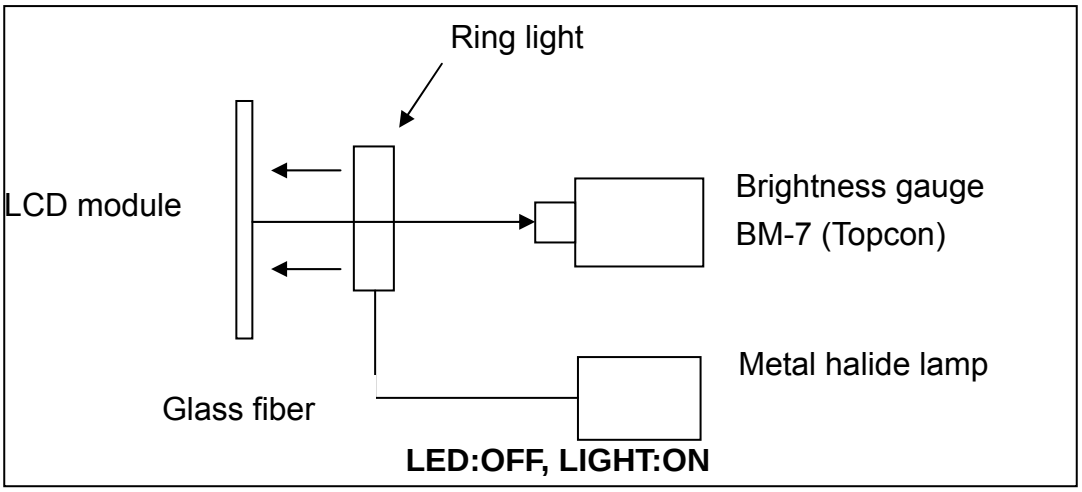
Main LCD: (1/160 Duty Ta = 25°C)

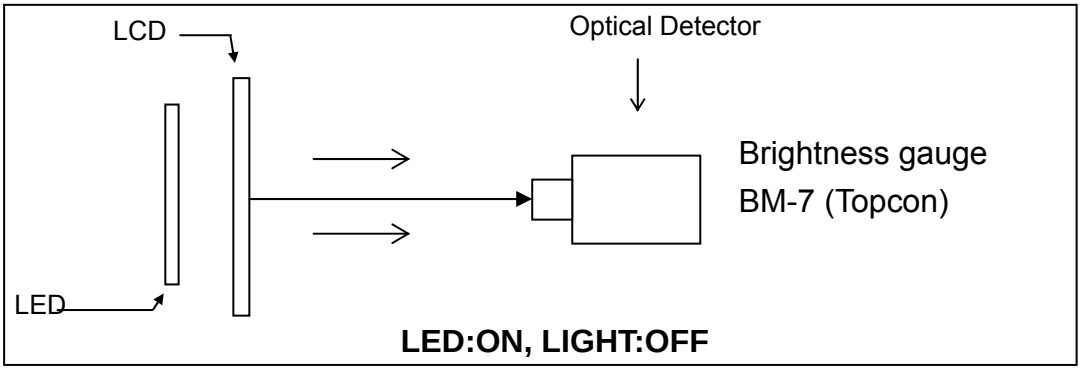
Item	Symbol	Transmissive			Conditions
		Min.	Std.	Max.	
Red	x	0.530	0.563	0.600	θ =0° , φ =0°
	y	0.300	0.336	0.360	
Green	x	0.290	0.319	0.370	θ =0° , φ =0°
	y	0.500	0.535	0.560	
Blue	x	0.110	0.142	0.170	θ =0° , φ =0°
	y	0.140	0.171	0.200	
White	x	0.270	0.303	0.340	θ =0° , φ =0°
	y	0.310	0.341	0.370	

Light source

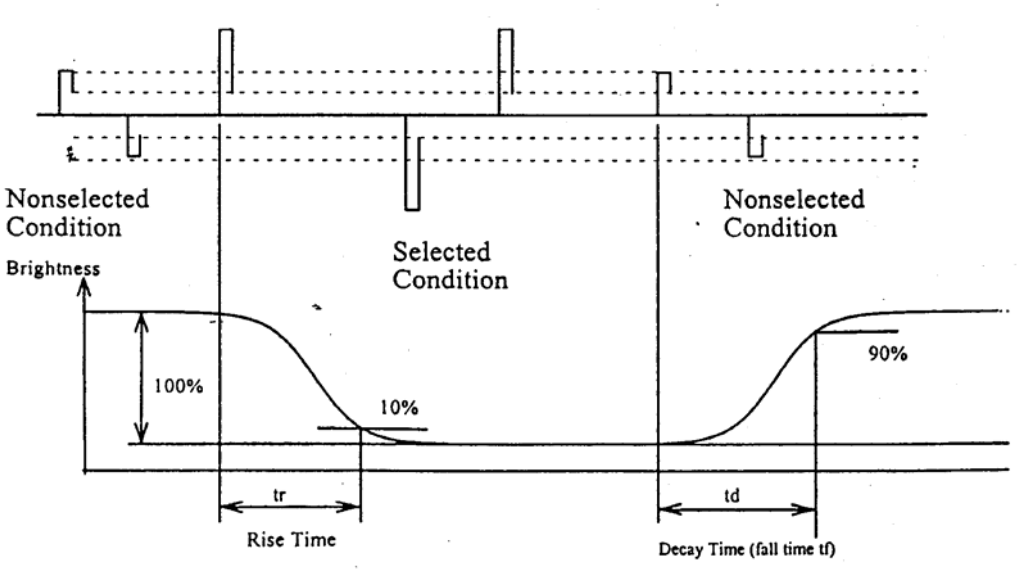
Item	Symbol	Value			Conditions
		Min.	Std.	Max.	
Light source	x	0.28	0.315	0.34	θ =0° , φ =0°
	y	0.28	0.305	0.34	
Main LCD brightness		900	1100	-	Unit: cd/m^2 (I_{LED}=15mA)

NOTE 1: Optical characteristic measurement system

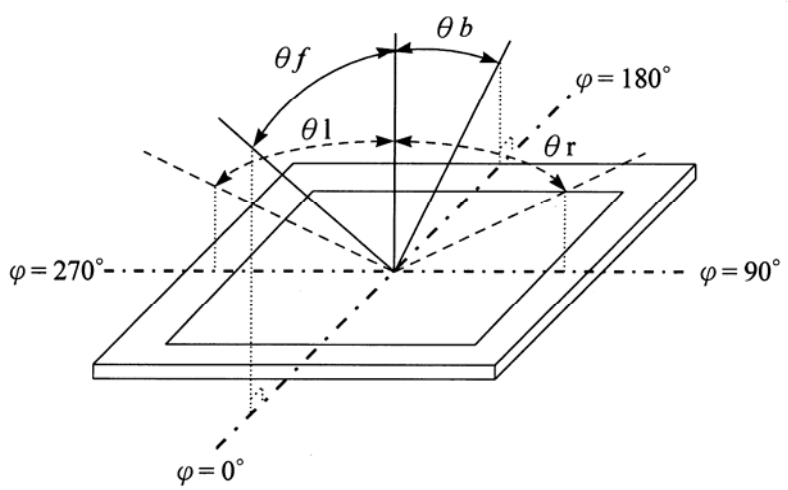




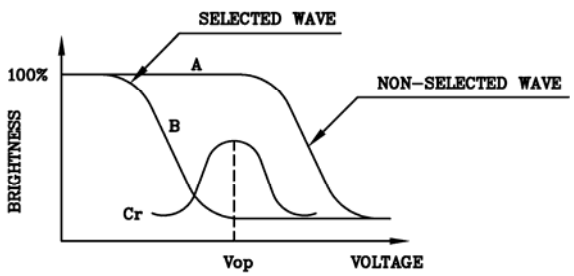
NOTE 2: Response tome definition



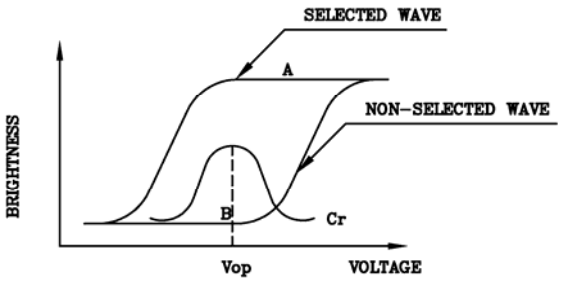
NOTE 3: φ 、θ definition



NOTE 4: Contrast definition



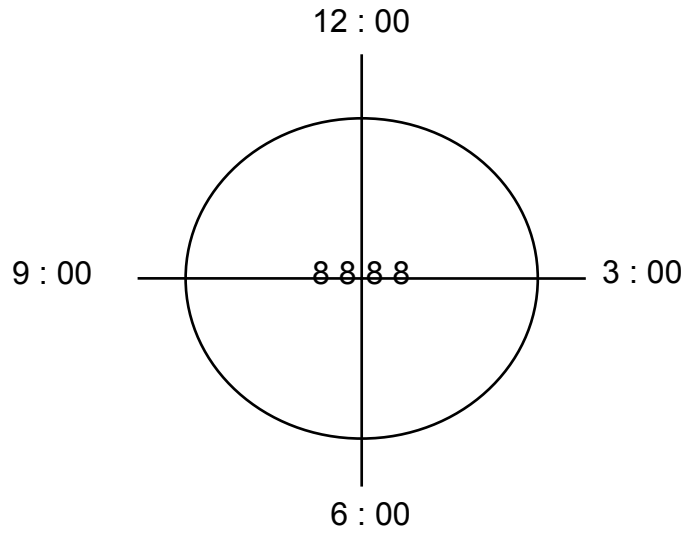
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

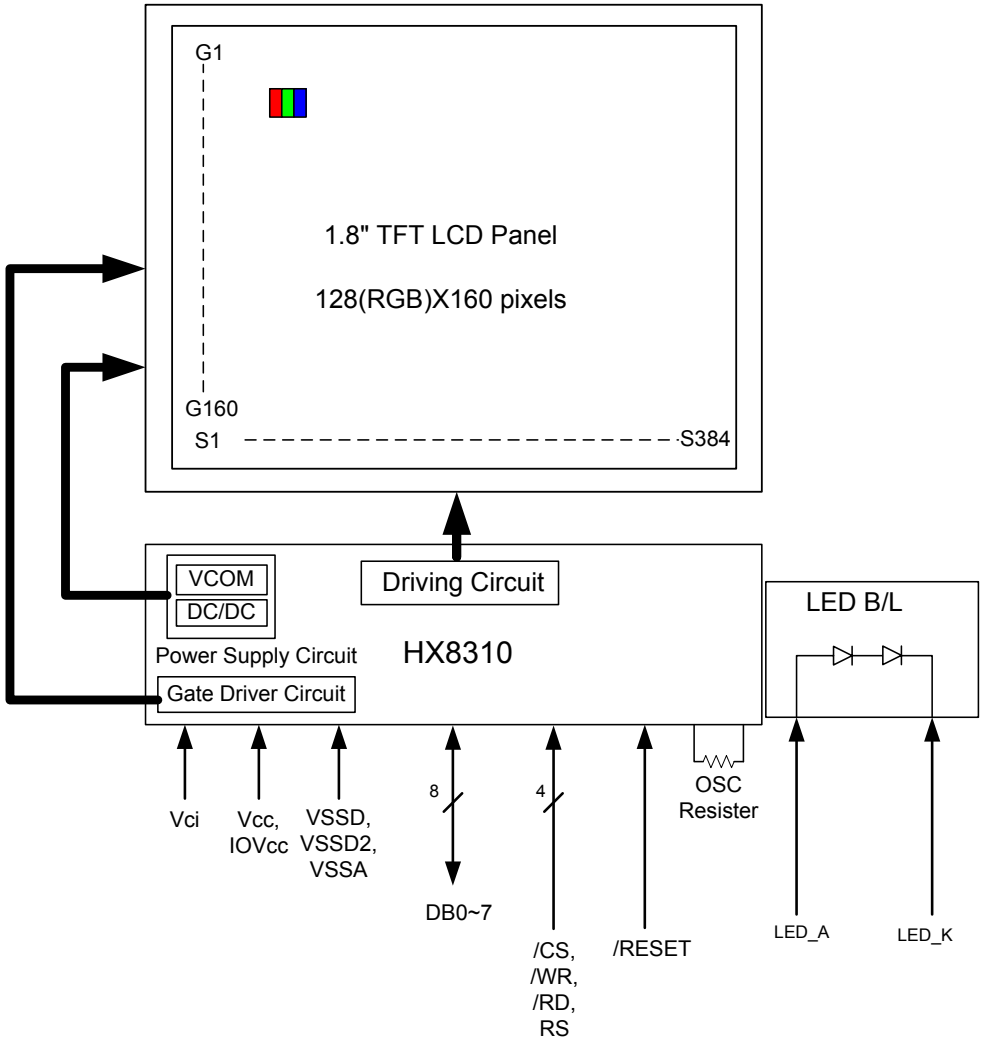
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type,12 o'clock.
Display composition: 128 x RGB x 160 pixels
LCD Driver : HX8310
Back light: White LED x 2 (I_{LED}=15mA)



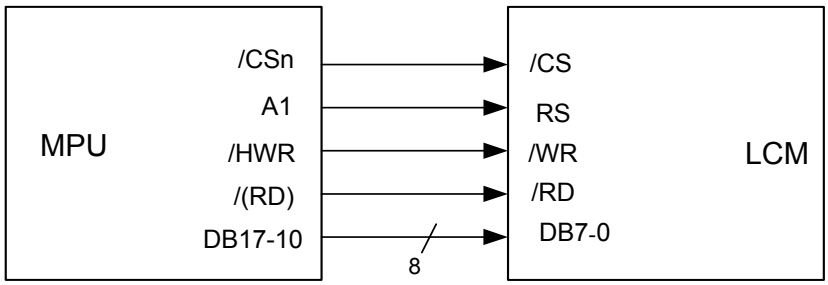
7 Interface specifications

Pin No.	Terminal	Functions
1	K	LED Backlight K terminal
2	A	LED Backlight A terminal
3	GND	GND-terminal for analog circuit
4	VDD	Power input terminal (System Power)
5	NC	No Connection
6	NC	No Connection
7	/CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.
8	/RESET	Main LCD Reset terminal, active “L”
9	RS	The signal for register index or register command select . Low: Register index or internal status (in read operation); High: Register command.
10	/WR	Write clock terminal , active “L” (80 series interface)
11	/RD	Read clock terminal , active “L” (80 series interface)
12	D7	Data Bus for 8-bits, 80-series MPU
13	D6	
14	D5	
15	D4	
16	D3	
17	D2	
18	D1	
19	D0	
20	GND	GND-terminal for analog circuit

7.1 System interface

IM bits setting and the type of system interface for Main LCD

IM0	MPU-interface Mode	DB Pin
1	80-system 8-bit Interface	DB17-10

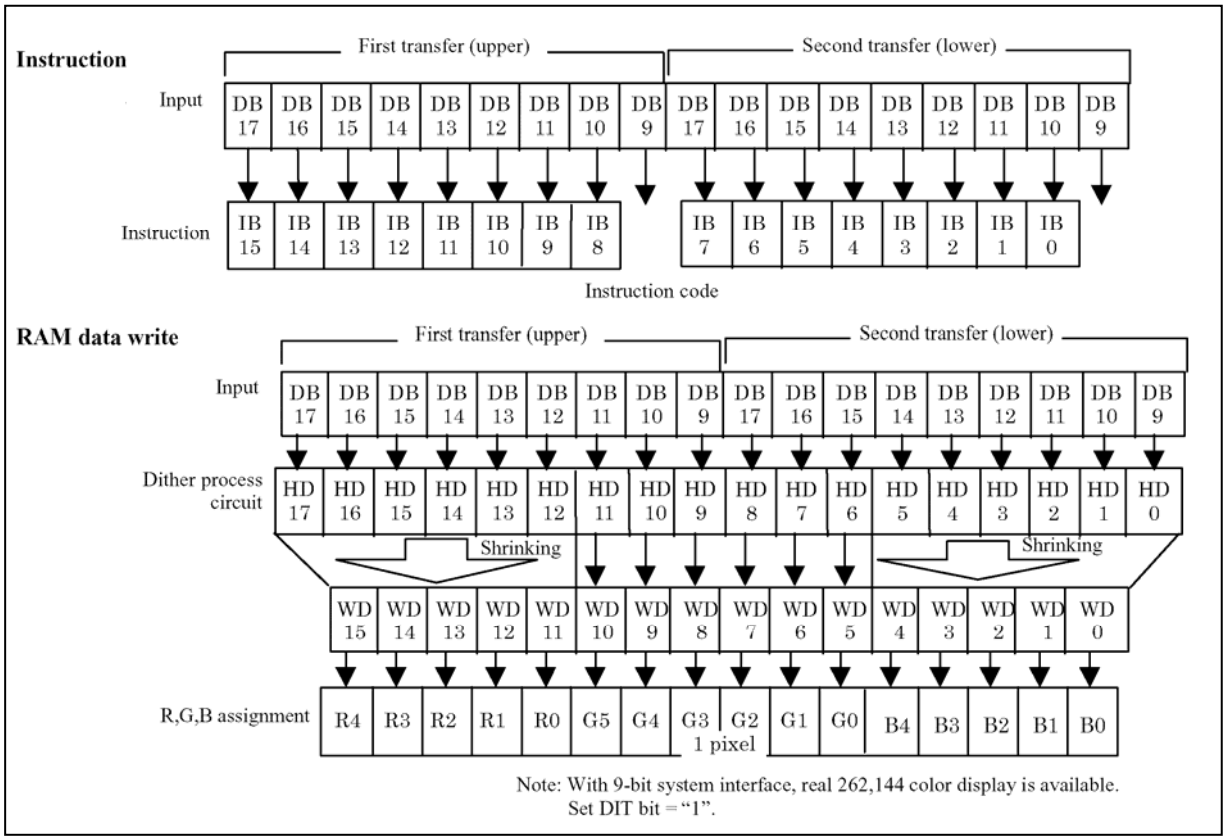


System Interface

7.2 80-system 8-bit interface

80-system 8-bit parallel data transmission is executed by setting IM3/2/1/0 pins to GND/GND/Vcc/Vcc levels respectively. Fixed unused pins DB9-DB0 to the VCC or GND level. When writing into the index register, the upper byte (8bits) must be written.

Data format for 8-bit interface



8 INSTRUCTION DESCRIPTIONS

8.1 Instruction List

Reg. No.	Register	R/W	RS	Upper Code								Lower Code							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	1
R01h	Driver output control	0	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
R02h	LCD drive AC control	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1)	0	1	0	0	0	0	0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
R04h	Power control (2)	0	1	CAD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R05h	Entry mode	0	1	DIT	0	0	BGR	0	0	HWM	0	0	0	VD1	VD0	AM	LG2	LG1	LG0
R06h	Compare register	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0
R08h																			
R09h																			
R0Ah																			
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
R0Ch	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
R0Dh	Power control (4)	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH 3	VRH 2	VRH 1	VRH 0
R0Eh	Power control (5)	0	1	0	0	VCO MG	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0
R0Fh	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN 4	CSN 3	SCN 2	SCN 1	SCN 0
R10h																			
R11h	Vertical scroll control	0	1	0	0	00	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R12h																			
R13h																			
R14h	First display drive position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	S12	SS11	SS10
R15h	Second display drive position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
R16h	Horizontal RAM address position	0	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VAS4	VSA3	VSA2	VSA1	VSA0

: Setting disable

Reg. No.	Register	R/W	RS	Upper Code								Lower Code							
				IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R18h																			
~																			
R1Fh																			
R20h	RAM Write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0
R21h	RAM address set	0	1	AD15-8 (Upper)								AD15-8 (Lower)							
R22h	RAM data write	0	1	Write Data (Upper)								Write Data (Lower)							
	RAM data read	1	1	Read Data (Upper)								Read Data (Lower)							
R23h																			
~																			
R2Fh																			
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	VRP03	VRP02	VRP01	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN03	VRN02	VRN01	VRN01	VRN00

: Setting disable

8.2 Instruction Explanation

Symbol	Function
L7-0	Indicates the position of raster-row driving the LCD.
SS	Select the output shift direction of the source drivers. 0: The output shift direction S1→S384 1: The output shift direction S384→S1
GS	Select the output shift direction of the gate drivers. 0: The output shift direction G1→G160 1: The output shift direction G160→G1
SM	Changes scan order of the gate driver.
NL4-0	Specify the number of lines for the LCD drive. Number of lines for the LCD drive can be adjusted for every eight raster-rows.
FLD1-0	Sets the number of fields during the n-field interlaced driving.
B/C	0: a B-pattern waveform is generated and alternates in every frame for LCD drive. 1: n raster-row waveform is generated and alternates in each raster-row specified by bits EOR and NW5-NW0 in the LCD driving waveform control register.
EOR	When B/C=1 and EOR=1, the odd/even frame select signals and the n-rater-row reversed signal are alternated.
NW5-0	Specify the number of raster-rows n that will alternate at the C-pattern waveform when B/C is “1”.
BT2-0	Change the step-up scale of the step-up circuit.
DC02-00	Select the operating frequency for the step-up circuit.
AP2-0	Adjust the amount of fixed current form the fixed current source in the OP-AMP for the LCD. AP2-0: “000” Halt the operation of OP-AMP to reduce the current consumption.
SLP	1: The sleep mode is selected.
STB	1: The standby mode is selected.
CAD	Set up based on retention capacitor configuration of the TFT panel 0: Using Cst composition. 1: Using Cadd composition.
VC2-0	Adjust the reference voltage for VREG1OUT, VREG2OUT and VciOUT to the optional ratio of Vci.
VRL3-0	Set magnification of amplification for VREG2OUT voltage.
PON	An operation starting bit for the booster circuit3. 0: Stop operation. 1: Start operation.

Symbol	Function
VRH3-0	Set the scale for amplifying VREG1OUT voltage.
VCOMG	1: VcomL voltage can output to negative voltage (-5V). 0: VcomL voltage becomes GND and stops the amplifier of the negative voltage.
VDV4-0	Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. When VCOMG=0, this setting is invalid.
VCM4-0	Set the VcomH voltage (The higher voltage during Vcom AC driving).
HWM	1: data are written to the GRAM in high speed.
I/I1-0	1: The address counter is automatically incremented by 1, after data are written to the GRAM. 0: The address counter is automatically decremented by 1, after data are written to the GRAM.
AM	Set the direction in which the address counter is updated automatically after data are written to the GRAM. 0: The address counter is updated in the horizontal direction. 1: The address counter is updated in the vertical direction.
DIT	1: Hard dither mode is selected.
LG2-0	Compare the data read from the GRAM or write data written from the MPU with the compare registers (CP15-0) by a compare/logical operation and write the result to the GRAM.
CP15-0	Set the value for the compare register, which the data read out from the GRAM or data written to the GRAM.
BGR	Reverse the order from R,G, and B to B,G and R for 16-bit data to be written to the GRAM. 1: CP15-0, WM15-0 bits are automatically changed in the same way.
PT1-0	Normalize the source outputs when non-display area is driven is the partial display mode.
VLE2-1	VLE1=1: Vertical scroll is executed on the 1st screen. VLE2=1: Vertical scroll is executed on the 2nd screen.
CL	1: The eight color display mode is selected.
SPT	1: an LCD is driven with 2 divided screens.
REV	1: The screen is the display area is inverted.
GON	0: The gate-off level is VGH.
D1-0	D1 = 1 the graphic display is ON. D1 = 0 the graphic display is OFF. (the data are remained in the GRAM) D1-0: “01” the internal display operates, even through the actual display is off. D1-0: ”00” both the internal display operations and display operation on the panel are halted.
RTN3-0	Set the 1H (1 raster-row) period.

Symbol	Function
DIV1-0	Set the division ratio of clocks for internal operations.
EQ1-0	Equalized period
SDT1-0	Determine the amount of delay for the source output from the falling-edge of the gate output.
NO1-0	Specify the amount of non-overlap time for the gate output.
SCN4-0	Set the scanning starting position of the gate driver.
VL7-0	Specify scroll length at the scroll display for vertical smooth scrolling.
SS17-10	Specify the driving start position for the first screen in a line unit.
SE17-10	Specify the driving end position for the first screen in a line unit.
SS27-20	Specify the driving start position for the second screen in a line unit.
SE27-20	Specify the driving end position for the second screen in a line unit.
HSA7-0/HEA7-0	Specify the horizontal start/end positions of a window for access in memory.
VSA7-0/VEA7-0	Specify the vertical start/end positions of a window for access in memory.
WM15-0	These bits write-mask the data to be written to the GRAM by a bit unit.
AD15-0	Mask initial settings for the GRAM address in the address counter (AC).
WD15-10	All data are expanded into 18 bits internally before being written to the GRAM.
RD15-0	Read 16-bit data from the GRAM.
PKP52-00	The γ fine adjustment registers for positive polarity.
PRP12-00	The γ gradient adjustment registers for positive polarity.
VRP14-00	The amplitude adjustment registers for positive polarity.
PKN52-00	The γ fine adjustment registers for negative polarity.
PRN12-00	The γ gradient adjustment registers for negative polarity.
VRN14-0	The amplitude adjustment registers for negative polarity.

8.3 Reset Function

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. Must be reset after the power is supplied. The time required for the /RESET input is at least 1ms. When the power supply is reset while the power supply is ON, wait at least 10ms after the power has been supplied until the RC oscillation frequency become stabilized. While waiting, do not make initial settings for the instruction set, nor access to the GRAM.

Register	Initial State of Instructions
Start oscillation	Executed
Driver output control	NL4-0=”10101”, SS=”0”, CS=”0”
LCD driving AC control	FLD1-0=”01”, B/C=”0”, NW5-0=”000000”
Power control (1)	BT2-0=”000”, DC2-0=”000”, AC2-0=”000” : LCD power off, SLP=”0”, STB=”0” : Standby mode off
Power control (2)	CAD=”0”
Entry mode set	DIT=”0”, BGR=”0”, HWM=”0”, I/D1-0=”11” : Increment by 1, AM=”0” : Horizontal direction LG2-0=”000” : Replace mode
Compare register	CP15-0 : “0000 0000 0000 0000”
Display control	PT1-0=”00”, VLE2-1=”00” : No vertical scroll, SPT=”0”, GON=”0”, DTE=”0”, CL=”0” : 65,536-color mode, REV=”0”, D1-0=”000” : Display off
Frame cycle control	NO1-0=”00”, SDT1-0=”00”, EQ1-0=”00” : No equalization, DIV1-0=”00” : 1 divided clock, RTN3-0=”0000” : 16 clock in 1H period
Power control (3)	VC2-0=”000”
Power control (4)	VRL3-0=”0000”, PON=”0”, VRH3-0=”0000”
Power control (5)	VCOMG=”0”, VDV4-0=”00000”, VCM4-0=”00000”
Gate scan starting position	SCN4-0=”00000”
Vertical scroll	VC7-0=”0000 0000”
1st screen division	SE17-10=”1111 1111”, SS17-10= ”0000 0000”
2nd screen division	SE27-20=”1111 1111”, SS27-20=”0000 0000”
Horizontal RAM address position	HEA7-0=”1000 0011”, HSA7-0=”0000 0000”

Register	Initial State of Instructions
Vertical RAM address position	VEA7-0=”1010 1111”, VSA7-0=”0000 0000”
RAM write data mask	WM15-0=”0000H” : No mask
RAM address set	AD15-0= “0000H”
γ control	PKP02-00=”000”, PKP12-10=”000”, PKP22-20=”000”, PKP32-30=”000” PKP42-40=”000”, PKP52-50=”000”, PRP02-00=”000”, PRP12-10=”000” PKN02-00=”000”, PKN12-10=”000”, PKN22-20=”000”, PKN32-30=”000” PKN42-40=”000”, PKN52-50=”000”, PRN02-00=”000”, PRN12-10=”000” VRP14-10=”00000”, VRP02-00=”0000”, VRN14-10=”00000”, VRN03-00=”000”

9 Timing Characteristics

80-system Bus interface Timing Characteristics (Main LCD)

Normal write mode (HWM=0) (Ta=25°C VCC = 2.2~2.4V)

Item		Symbol	Conditions	MIN	MAX	Unit
Bus cycle time	Write	t_{CYCW}		600	-	ns
	Read	t_{CYCR}		800	-	ns
Write low-level pulse width		PW_{LW}		90	-	ns
Read low-level pulse width		PW_{LR}		350	-	ns
Write high-level pulse width		PW_{HW}		300		ns
Read high-level pulse width		PW_{HR}		400		ns
Write/Read rise/fall time		t_{WRr}, t_{WRf}		-	25	ns
Set up time (RS to CS,WR,RD)		t_{AS}		10	-	ns
Address hold time		t_{AH}		5	-	ns
Write data set up time		t_{DSW}		60	-	ns
Write data hold time		t_H		15	-	ns
Read data delay time		t_{DDR}		-	200	ns
Read data hold time		t_{DHR}		5	-	ns

High-speed Write mode (HWM=1) (Ta=25°C VCC = 2.2~2.4V)

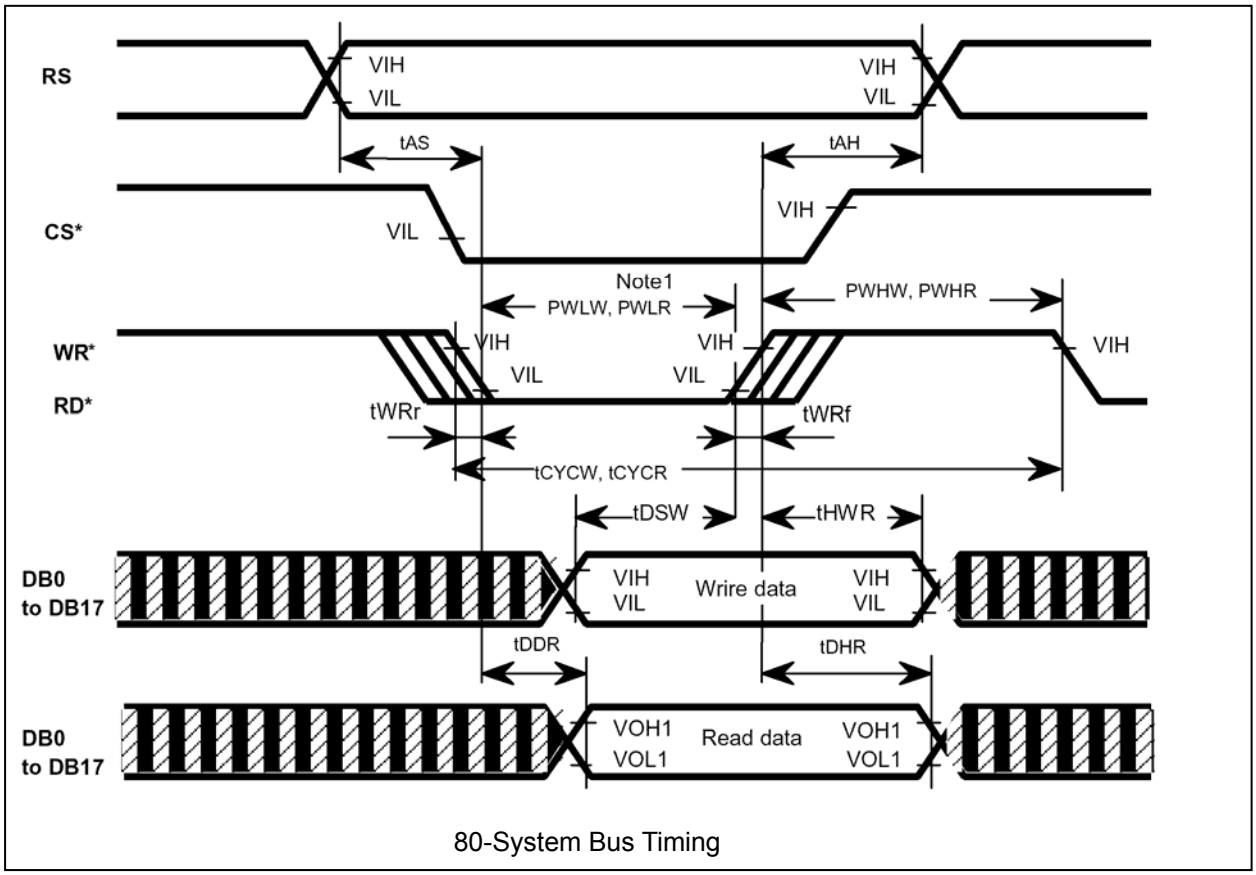
Item		Symbol	Conditions	MIN	MAX	Unit
Bus cycle time	Write	t_{CYCW}		200	-	ns
	Read	t_{CYCR}		800	-	ns
Write low-level pulse width		PW_{LW}		90	-	ns
Read low-level pulse width		PW_{LR}		350	-	ns
Write high-level pulse width		PW_{HW}		90		ns
Read high-level pulse width		PW_{HR}		400		ns
Write/Read rise/fall time		t_{WRr}, t_{WRf}		-	25	ns
Set up time (RS to CS,WR,RD)		t_{AS}		10	-	ns
Address hold time		t_{AH}		5	-	ns
Write data set up time		t_{DSW}		60	-	ns
Write data hold time		t_H		15	-	ns
Read data delay time		t_{DDR}		-	200	ns
Read data hold time		t_{DHR}		5	-	ns

Normal write mode (HWM=0) (Ta=25°C VCC = 2.4~3.3V)

Item		Symbol	Conditions	MIN	MAX	Unit
Bus cycle time	Write	t_{CYCW}		200	-	ns
	Read	t_{CYCR}		300	-	ns
Write low-level pulse width		PW_{LW}		40	-	ns
Read low-level pulse width		PW_{LR}		150	-	ns
Write high-level pulse width		PW_{HW}		100		ns
Read high-level pulse width		PW_{HR}		100		ns
Write/Read rise/fall time		t_{WRr}, t_{WRf}		-	25	ns
Set up time (RS to CS,WR,RD)		t_{AS}		10	-	ns
Address hold time		t_{AH}		2	-	ns
Write data set up time		t_{DSW}		60	-	ns
Write data hold time		t_H		2	-	ns
Read data delay time		t_{DDR}		-	100	ns
Read data hold time		t_{DHR}		5	-	ns

High-speed Write mode (HWM=1) (Ta=25°C VCC = 2.4~3.3V)

Item		Symbol	Conditions	MIN	MAX	Unit
Bus cycle time	Write	t_{CYCW}		100	-	ns
	Read	t_{CYCR}		300	-	ns
Write low-level pulse width		PW_{LW}		40	-	ns
Read low-level pulse width		PW_{LR}		150	-	ns
Write high-level pulse width		PW_{HW}		40		ns
Read high-level pulse width		PW_{HR}		100		ns
Write/Read rise/fall time		t_{WRr}, t_{WRf}		-	25	ns
Set up time (RS to CS,WR,RD)		t_{AS}		10	-	ns
Address hold time		t_{AH}		2	-	ns
Write data set up time		t_{DSW}		60	-	ns
Write data hold time		t_H		2	-	ns
Read data delay time		t_{DDR}		-	100	ns
Read data hold time		t_{DHR}		5	-	ns

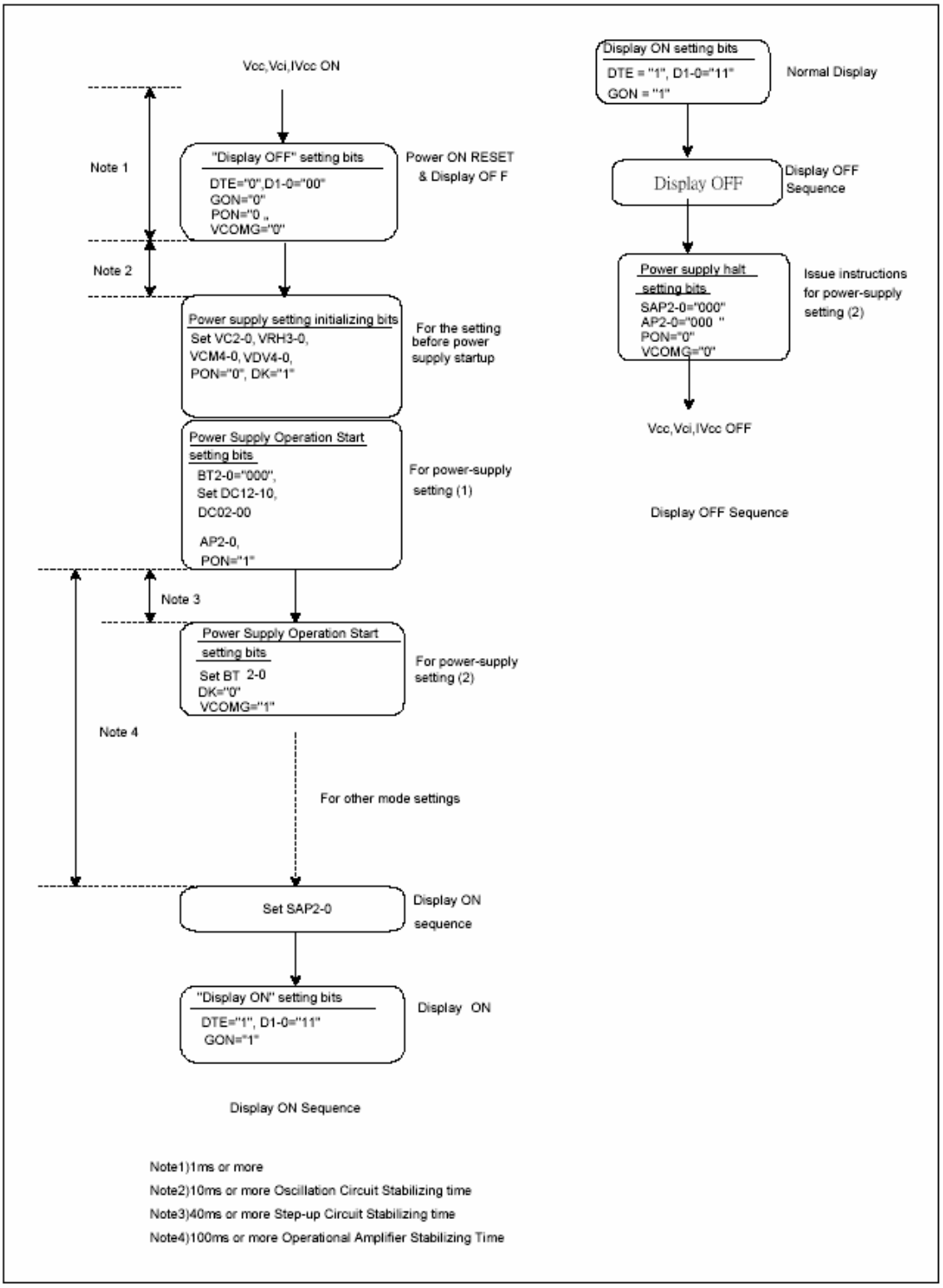


80-System Bus Timing

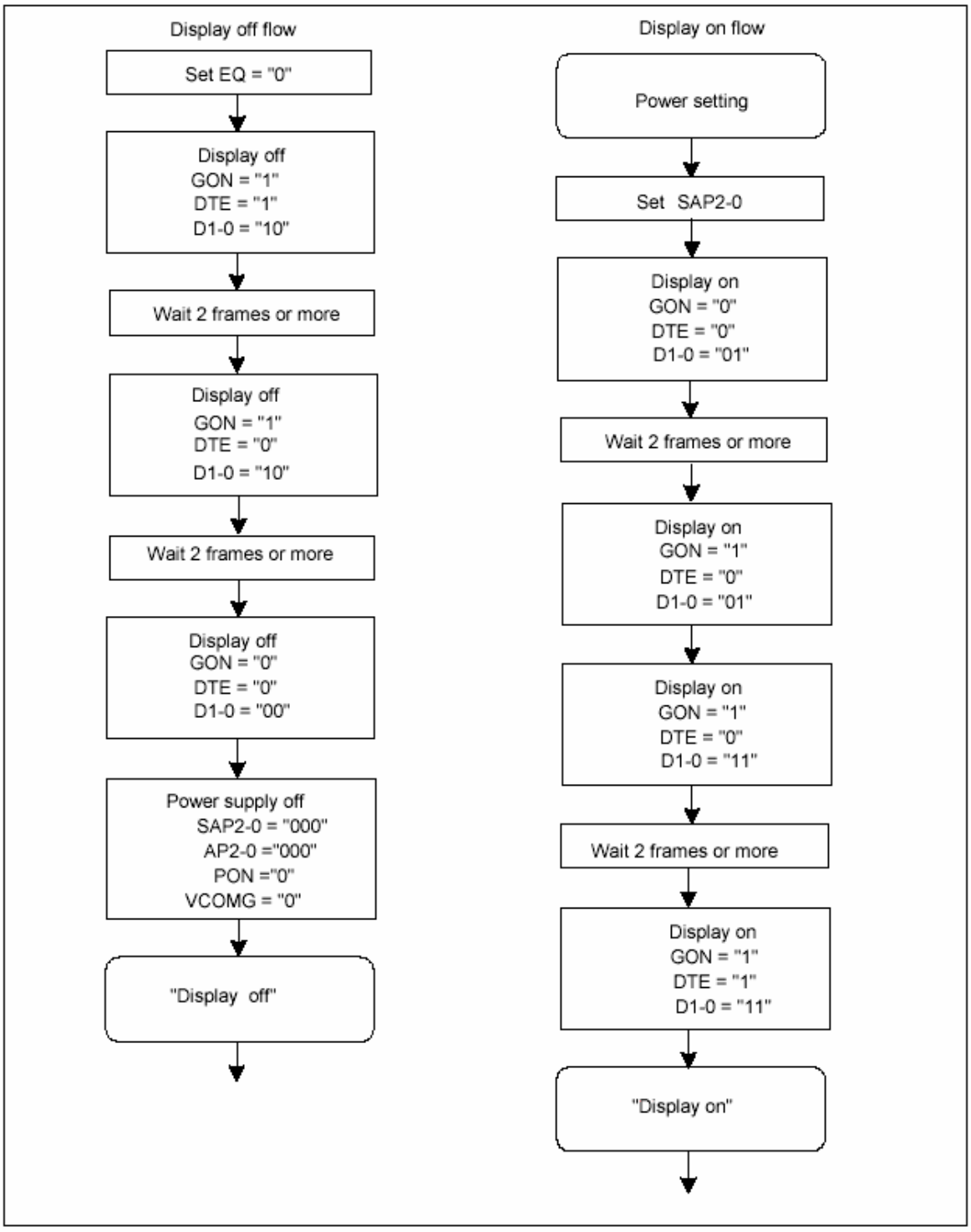
Note 1) PWEL is specified during the overlap period. (SC*="Low", WR* or RD*="Low")

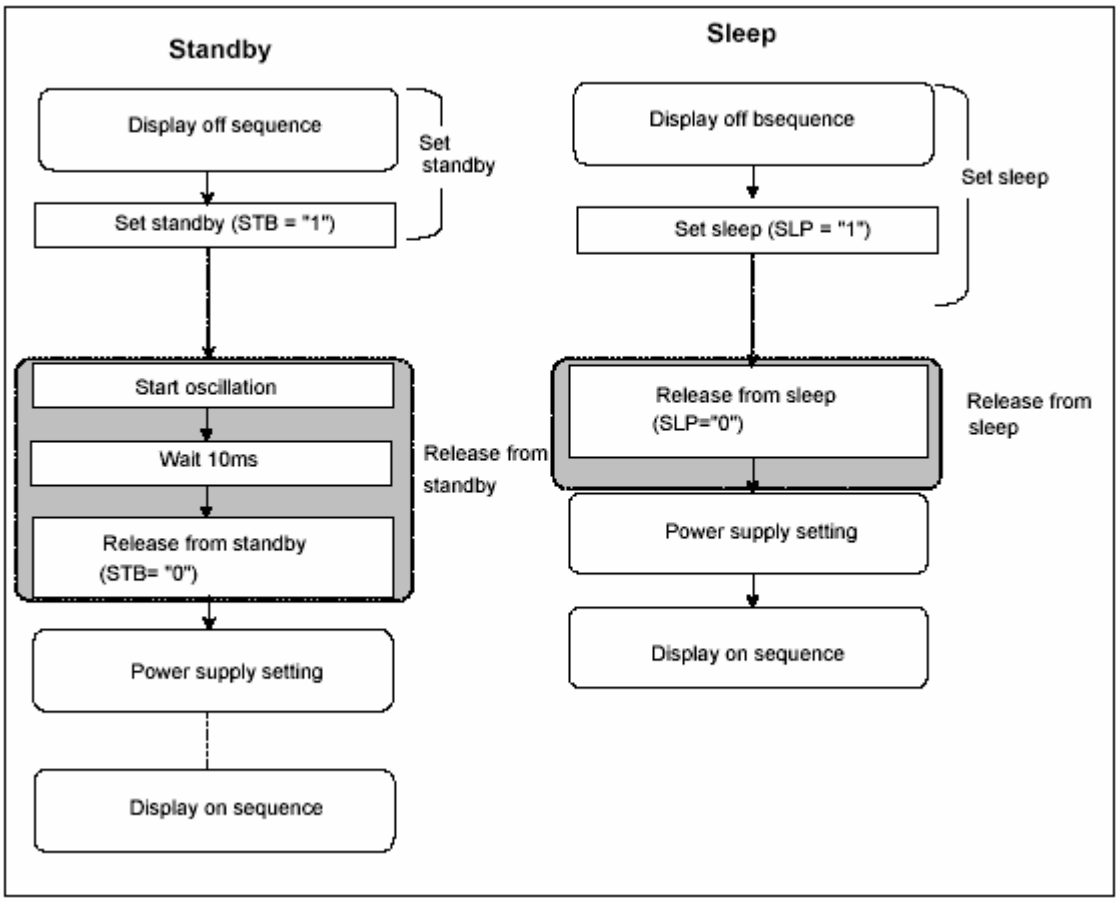
Note 2) When using 16-bit bus interface, parallel data can be transferred through DB17-10 pin and DB8-1. DB9 and DB0 must be fixed to "Vcc" or "GND".

10 SETUP FLOW OF POWER SUPPLY



11 INSTRUCTION SETUP FLOW




Standby
Display off sequence
Set standby
Set standby (STB = "1")
Start oscillation
Wait 10ms
Release from standby
(STB= "0")
Release from standby
Power supply setting
Display on sequence
Sleep
Display off bsequence
Set sleep
Set sleep (SLP = "1")
Release from sleep
(SLP="0")
Release from sleep
Power supply setting
Display on sequence

12 QUALITY AND RELIABILITY

12.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

12.2 SAMPLING PLAN

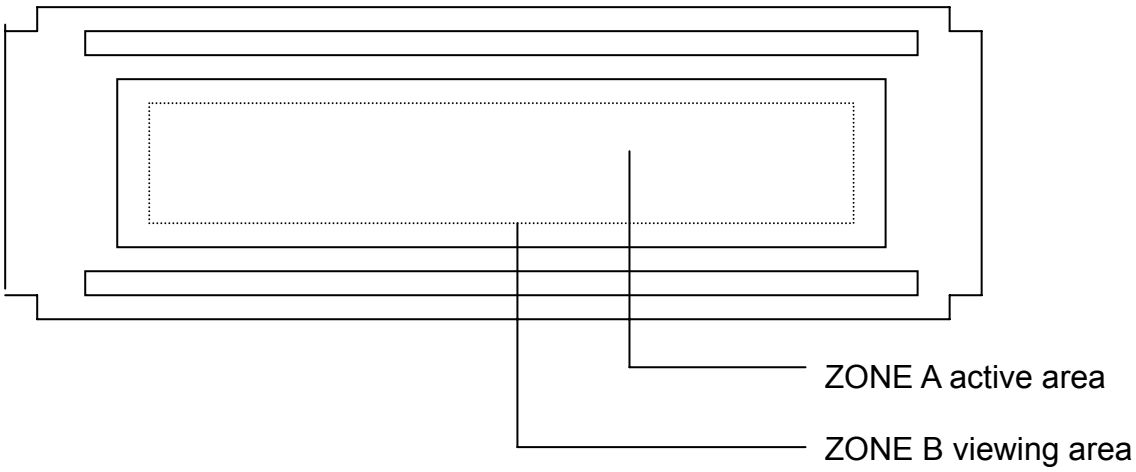
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

12.3 ACCEPTABLE QUALITY LEVEL

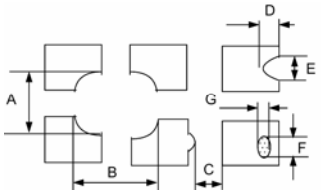
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

12.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



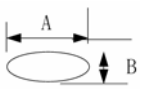
12.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line (I)</td><td><table><tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < W ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < W ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < W ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
<tr><td>8</td><td>dot defect</td><td><table><tr><td>Bright dot</td><td>N≦1</td></tr><tr><td>Dark dot</td><td>N≦3</td></tr><tr><td>Total dot defect
(Bright dot + Dark dot)</td><td>N≦3</td></tr><tr><td>Minimum distance between dark dot and dark dot</td><td>L≧5 mm</td></tr></table></td><td>Minor</td></tr>
<tr><td>9</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there’re to two or more pinholes per dot</td><td>Minor</td></tr>
</table>

<table>
<tr><td>10</td><td>Blemish & Foreign matters

Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>11</td><td>Scratch on Polarizer

  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr><tr><td></td><td>L > 2.0</td><td>1</td></tr><tr><td>0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr><tr><td></td><td>L ≤ 1.0</td><td>Ignore</td></tr><tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr></table>Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>12</td><td>Bubble in polarizer</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.20</td><td>Ignore</td></tr><tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr><tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr><tr><td>0.80 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>13</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>14</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>16</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
<tr><td>17</td><td>Parts alignment</td><td>1. LSI, IC lead width is more than 50% beyond pad outline.
2. Chip component is off center and more than 50% of the leads is off the pad outline.</td><td>Minor

Minor</td></tr>
<tr><td>18</td><td>Conductive foreign matter (Solder ball, Solder chips)</td><td>1. 0.45< φ ,N≧1
2. 0.30< φ ≤0.45 ,N≧1
φ :Average diameter of solder ball (unit: mm)
3. 0.50<L ,N≧1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td></tr>
<tr><td>19</td><td>Faulty PCB correction</td><td>1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB.
2. Short circuited part is cut, and no resist coating has been performed.</td><td>Minor

Minor</td></tr>
</table>

12.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

13 USE PRECAUTIONS

13.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

13.2 Installing precautions

1) To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

13.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

13.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

13.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

14 MECHANICAL DRAWING