AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

2.0-in COLOR TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A M - 1 7 6 2 2 0 J T N Q W - 0 0 H
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2005/12/23	-	New Release	Emil
2006/2/9	-	Change Part No. from TF-176220-35-0 to AM-176220JTNQW-00H	Eric
		Revised All T.B.D data.	Eric
2006/2/20	12-15	Interface support 8/9/16/18-bit MPU Interface.	Eric
2006/3/10	3,37	Change LCD viewing direction to 12H.	Eric
2006/12/7	7	Change LCD viewing angle.	John
	4	Change the shape dimensions	

1 Features

This single-display module is suitable for cell phone application. The Main-LCD adopts one backlight with High brightness 3-lamps white LED.

(1) Construction: 2.0” a-Si color TFT-LCD, White LED Backlight, and FPCB.

(2) Main LCD : 2.1 Amorphous-TFT 2.0 inch display, transmissive, Normally white type, 12 o’clock.
2.2 176(RGB)X220 dots Matrix,1/220 Duty.
2.3 Narrow-contact ledge technique.
2.4 Main LCD Driver IC: HX8309
2.5 Real 262K colors display:
262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)
Dithering 262K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)

(3) Low cross talk by frame rate modulation
(4) Direct data display with display RAM
(5) Partial display function: You can save power by limiting the display space.
(6) MPU interface: 8/9/16/18-bit 80-Series, parallel interface.
(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*37.68(W) x 69.84(H) x3.14 (D) Max.	mm
Main LCD	Pixel size	0.06 (W) x 0.18 (H)	mm
	Active area	31.68 (W) x 39.6 (H)	mm
	Color filter area	31.68 (W) x 43.4 (H)	mm
Weight		TBD	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+3.3	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70 °C Min. -20 °C	Note 1: Non-condensing
Operating temperature	Max. +60 °C Min. -10 °C	Note 1: Non-condensing

Note 1：Ta≦+40 °C・・・・Max.85%RH

Ta＞+40 °C・・・・The max. humidity should not exceed the humidity with 40 °C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 °C)

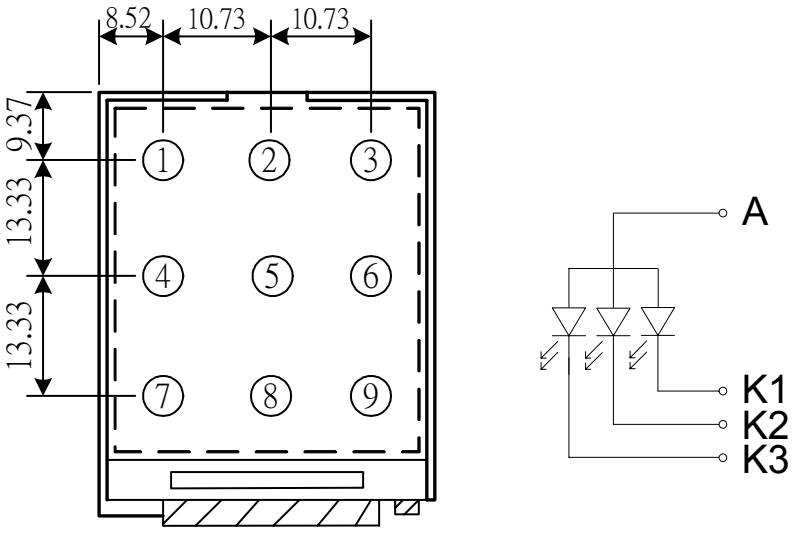
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.4	3.0	3.3	V
High-level input voltage	V_{IHC}		0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{ILC}		0		0.2V_{DD}	V
Consumption current of VDD	I_{DD}	LED OFF	-	4	5	mA
Consumption current of LED	I_{LED_ON}	V_{LED_ON}=3.3V	-	45	55	mA

※ 1. 1/220 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =45mA	3.2	3.3	4	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	3-chip parallel	40	45	55	mA
Power Consumption	P_{BL}	I_f =45mA	-	162	-	mW
Uniformity (with L/G)	-	I_f=45mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	3.3V 45mA	2400	-	-	cd/m^2
Luminous color	White					
Chip connection	3 chip parallel connection					

Bare LED measure position:



*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/220 Duty in case except as specified elsewhere Ta = 25°C)

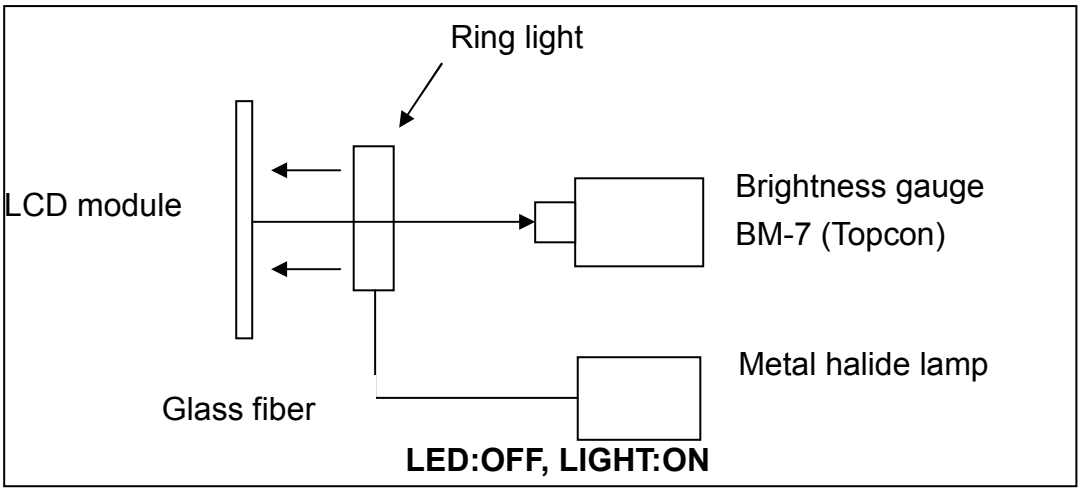
LED backlight transmissive module:

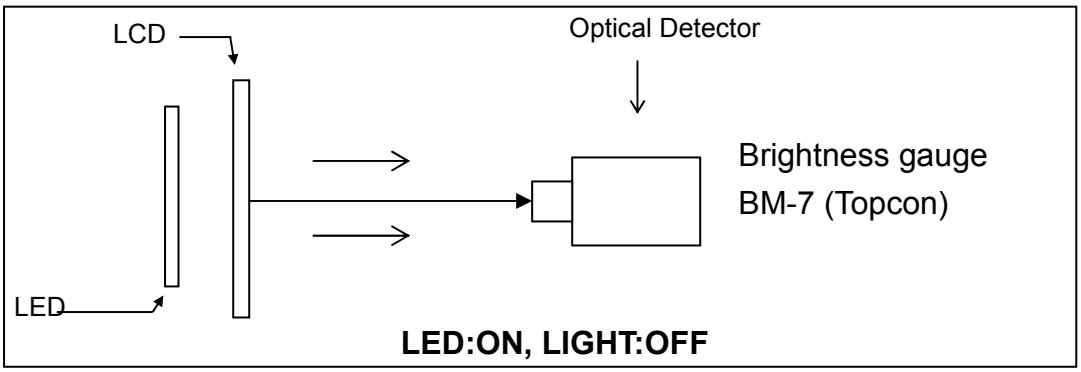
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	-	15	30	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	-	35	50		
Contrast ratio	CR	25°C	150	200	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	6	-	%	
Visual angle range front and rear	θ	25°C	(θf)15 (θb) 35			De-gree	φ= 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 45 (θr) 45			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			150			Cd/m2	V_{LED}=3.3V, 45mA Full White pattern

5.2 CIE (x, y) chromaticity (1/220 Duty Ta = 25°C)

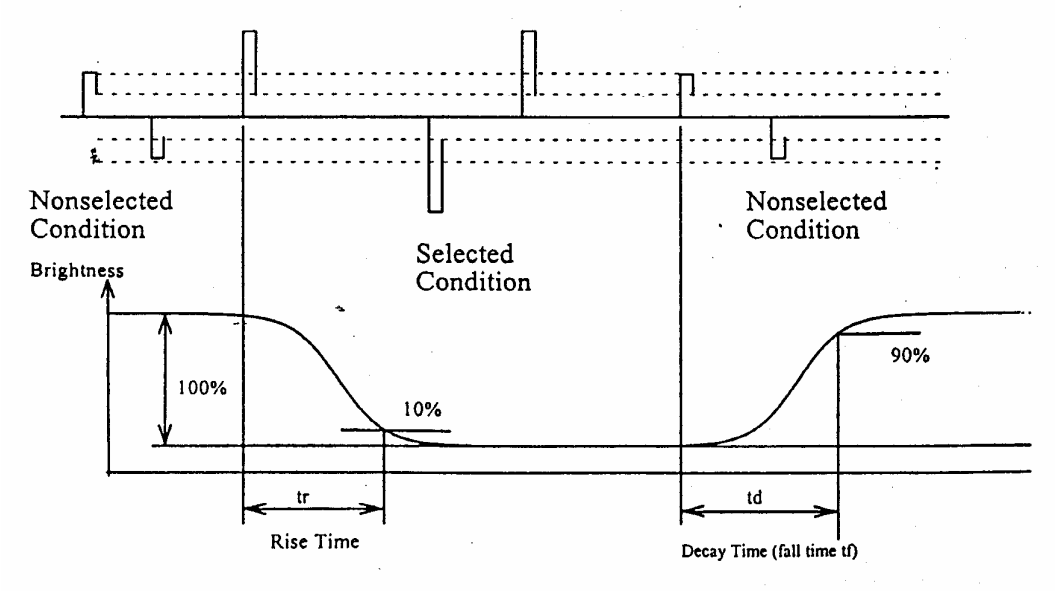
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	0.610	0.640	0.670	θ=0°, φ=0°
	Y	0.315	0.645	0.375	
Green	X	0.267	0.297	0.327	θ=0°, φ=0°
	Y	0.554	0.584	0.614	
Blue	X	0.101	0.131	0.161	θ=0°, φ=0°
	Y	0.120	0.142	0.172	
White	X	0.283	0.313	0.343	θ=0°, φ=0°
	Y	0.325	0.355	0.385	

NOTE 1: Optical characteristic measurement system

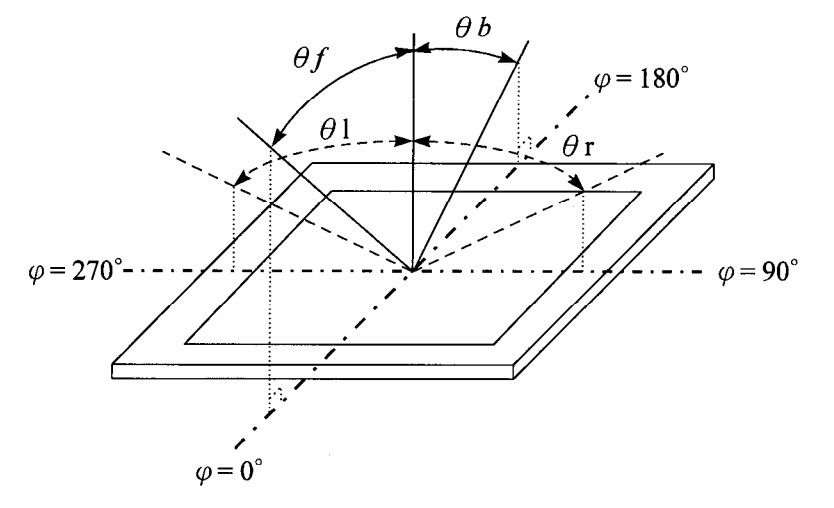




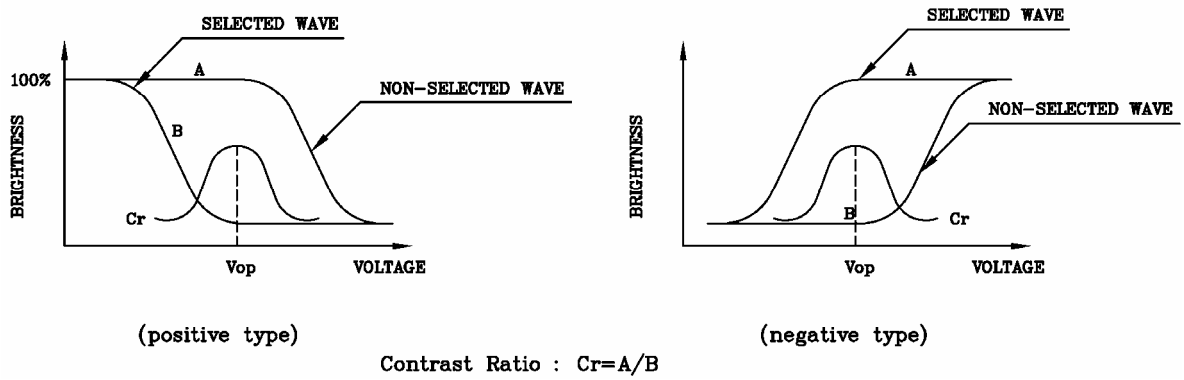
NOTE 2: Response tome definition



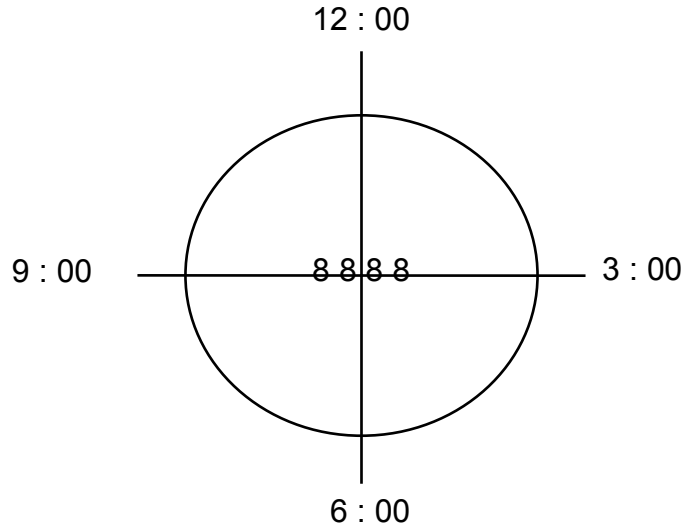
NOTE 3: φ 、θ definition



NOTE 4: Contrast definition



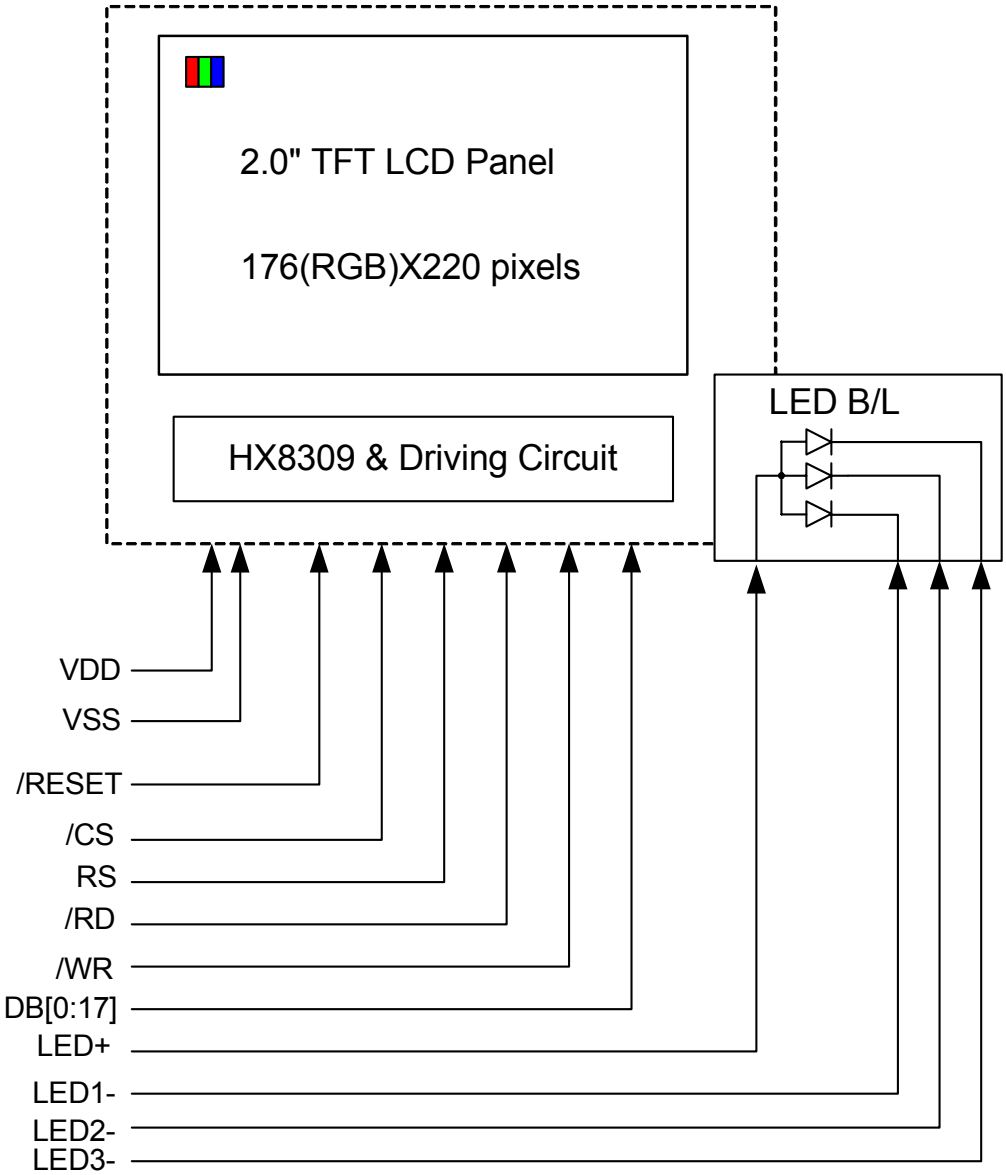
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 176 x RGB x 220 dots
LCD Driver : HX8309
Back light: White LED x 3 (I_{LED}=45mA)



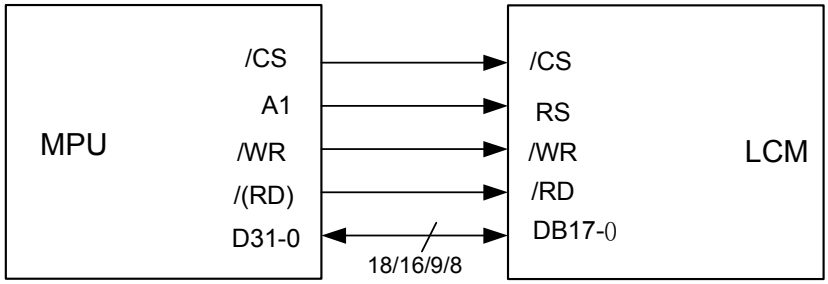
7 Interface specifications

Pin No.	Terminal	Functions
1	DUMMY1	DUMMY PIN
2	GND1	GND-terminal for analog circuit.
3	VCC1	Power supply for the internal logic circuit. (VCC=2.2~3.3V)
4	CS	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed.
5	RS	The signal for register index or register command select . Low: Register index or internal status (in read operation); High: Register command.
6	/WR	Write clock terminal, active “L” (80 series interface).
7	/RD	Read clock terminal, active “L” (80 series interface).
8	IM0	Select MPU Interface type (8/9/16 bits) by IM0 and IM3.
9	DB0	MPU interface for 80-system input. 18-bits: Connection DB17-0 16-bits: Connection DB17-10 and DB8-1 pins. Unused pins must be fixed to VDD or GND level.
10	DB1	
11	DB2	
12	DB3	
13	DB4	
14	DB5	
15	DB6	
16	DB7	
17	DB8	
18	IM3	Select MPU Interface type (8/9/16 bits) by IM0 and IM3.
19	DB9	MPU interface for 80-system input. 18-bits: Connection DB17-0 16-bits: Connection DB17-10 and DB8-1 pins. 9-bits: Connection DB17-9 pins. 8-bits: Connection DB17-10 pins. Unused pins must be fixed to VDD or GND level.
20	DB10	
21	DB11	
22	DB12	
23	DB13	
24	DB14	
25	DB15	
26	DB16	
27	DB17	
28	RESET	LCD Reset terminal, active “L”.
29	VC1	Power supply for Step-up circuit. (VCi=2.5~3.3V)
30	VCC2	Power supply for the internal logic circuit. (VCC=2.2~3.3V)
31	GND2	GND-terminal for analog circuit.
32	DUMMY2	DUMMY PIN

7.1 System interface

IM bits setting and the type of system interface for LCD

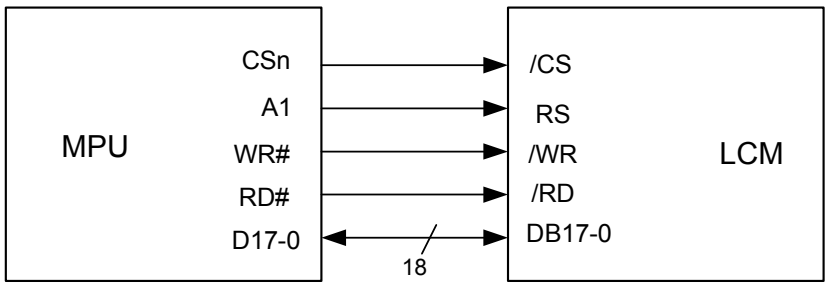
IM0	IM3	MPU interface mode	DB pins
0	0	16-bit bus interface, 80-system	DB17-10, 8-1
0	1	18-bit bus interface, 80-system	DB17-0
1	0	8-bit bus interface, 80-system	DB17-10
1	1	9-bit bus interface, 80-system	DB17-9



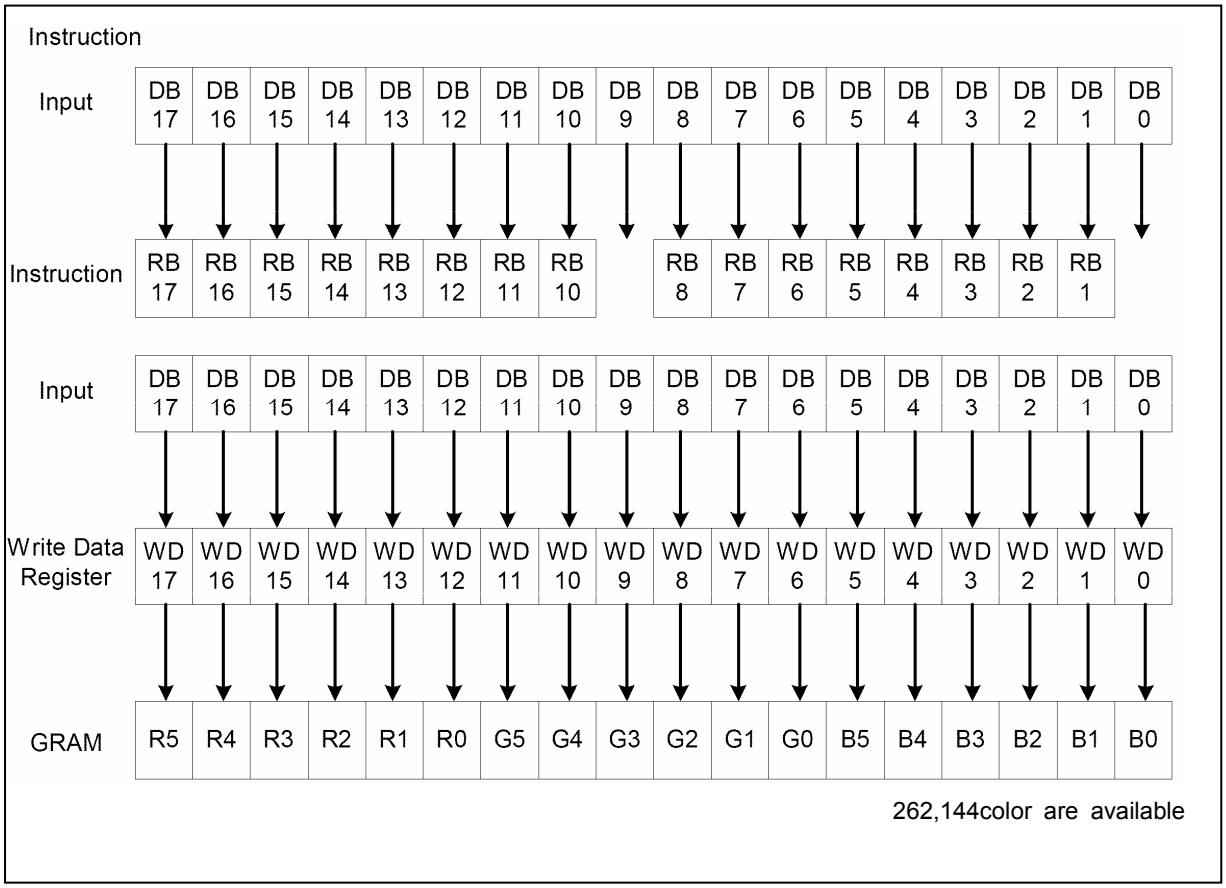
System Interface

7.2 80-system 18-bit interface

The 80-system 18-bit parallel data transfer can be used bye setting IM3 & IM0 pins to “10”. The below picture is the example of interface with i80Microcomputer and data format of 18-bit system interface.

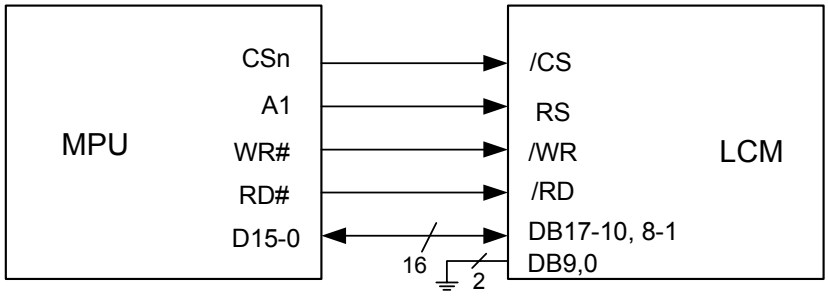


Data format for 18-bit interface

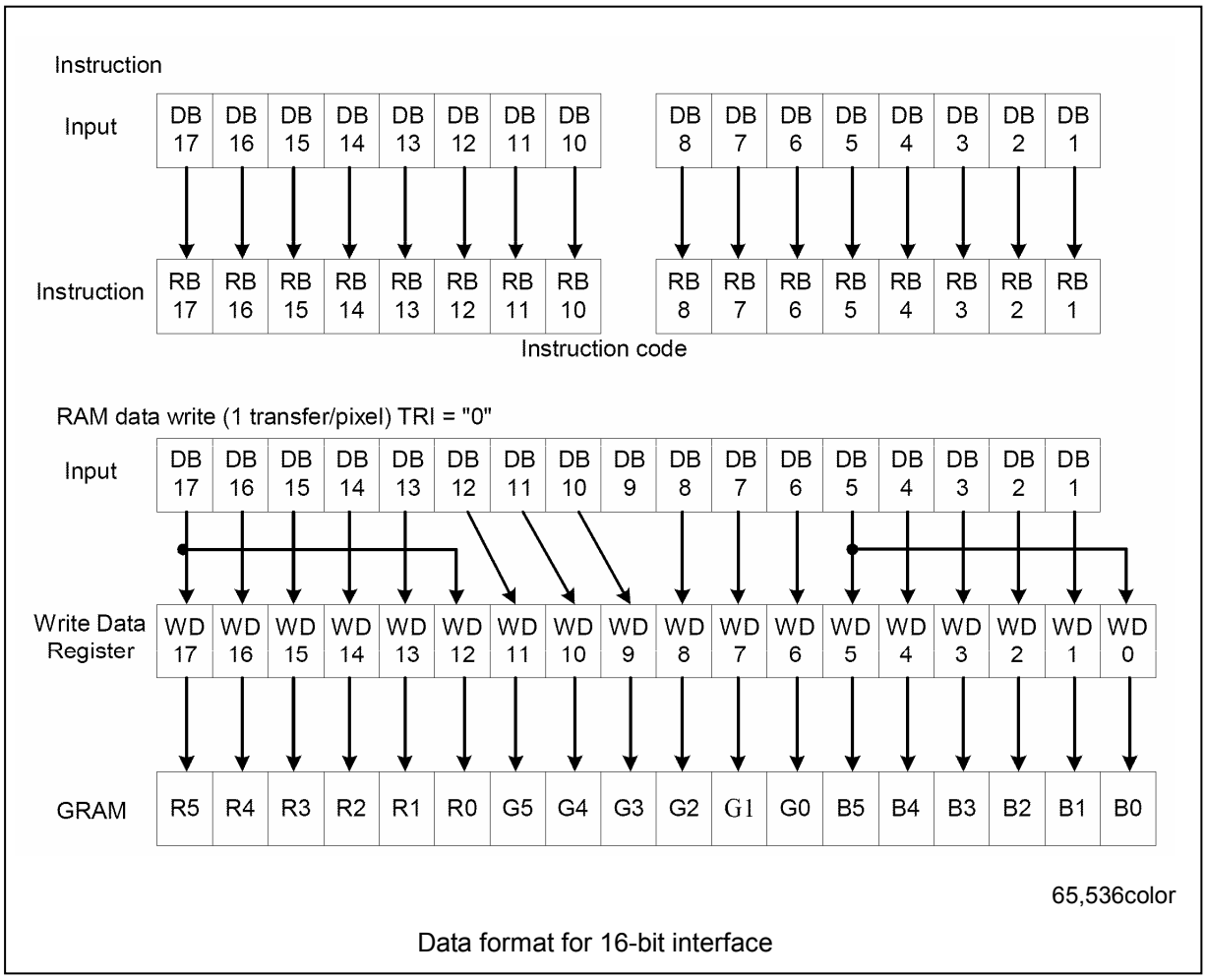


7.3 80-system 16-bit interface

The 80-system 16-bit bus parallel data transfer can be used bye setting IM3 & IM0 pins to “00”. The data written to GRAM is expended to 18-bit bys data automatically in the LSI. Unused pin(DB9,DB0) must be fixed to the VDD or GND level.



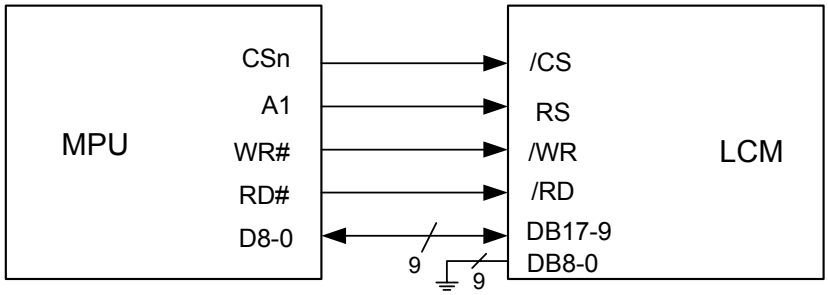
Data format for 16-bit interface



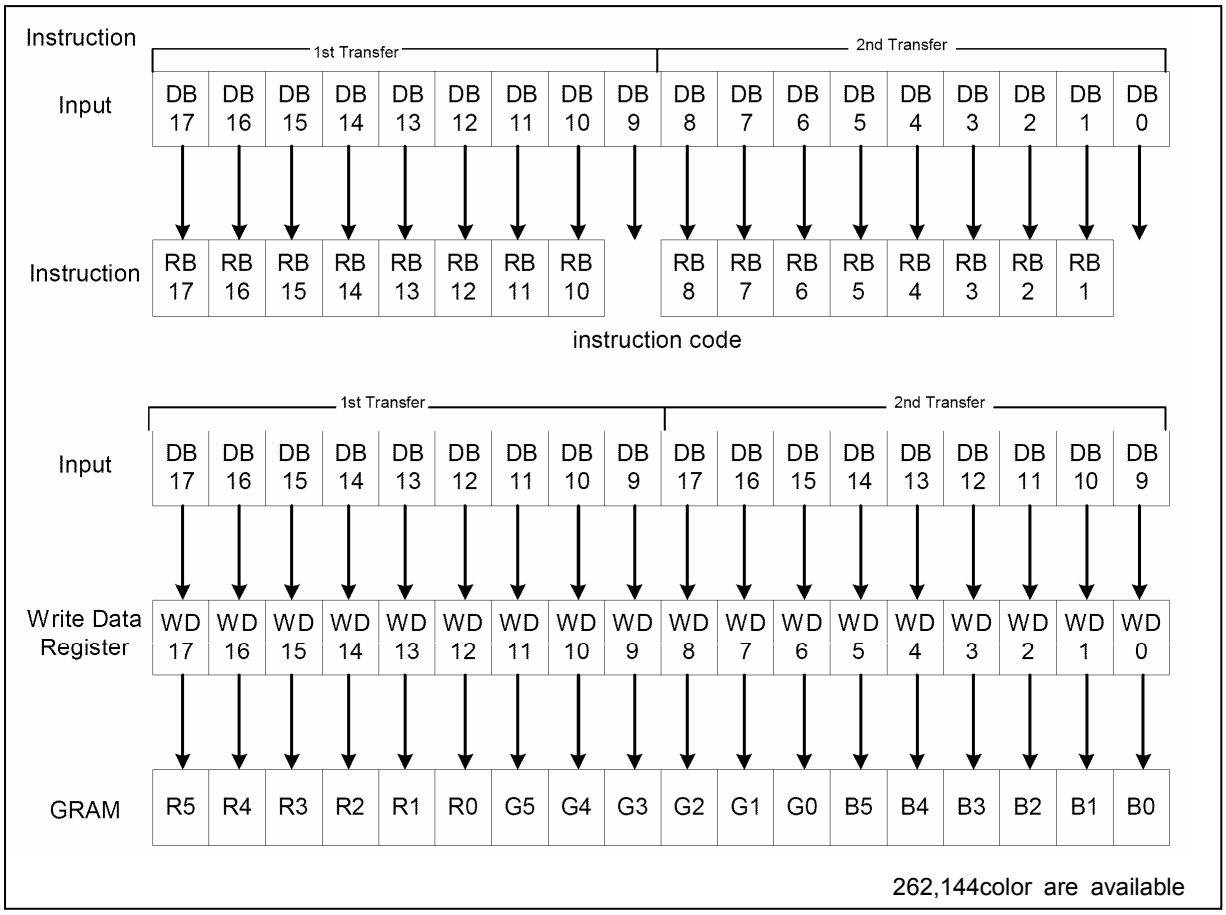
Data format for 16-bit interface

7.4 80-system 9-bit interface

The 80-system 9-bit bus parallel data transfer can be used bye setting IM3 & IM0 pins to “11”. In 80-system 9-bit bus parallel data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper nine bits, and then the upper nine bits are transferred first. Unused pin(DB8-0) must be fixed to the VDD or GND level. Ensure that upper bytes have to be written when writing the index register.

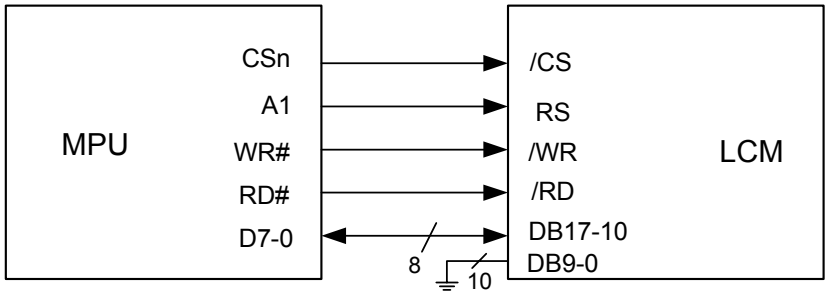


Data format for 9-bit interface

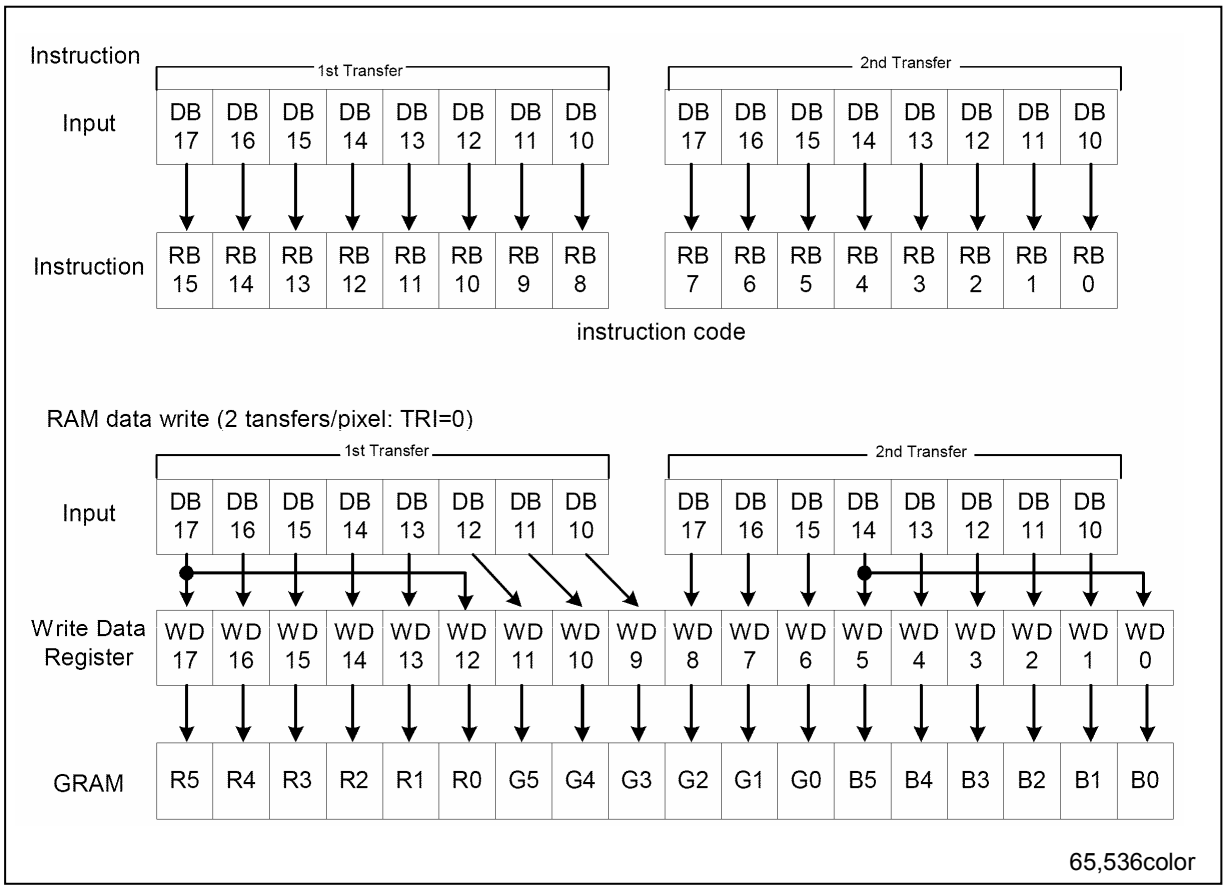


7.5 80-system 8-bit interface

The 80-system 8-bit bus parallel data transfer can be used bye setting IM3 & IM0 pins to “01”. In 80-system 8-bit bus parallen data transfer mode, the 16-bit bus instruction and GRAM write data are divided into lower and upper eight bits, and then the upper eight bits are transferred first. Furthermore, the GRAM write data can be expended into 16-bit bus automatically in internal process. Unused pin(DB9-0) must be fixed to the VDD or GND level.



Data format for 16-bit interface



7.6 Instruction List

Register No.	Register	R/W	RS	Upper Code							Lower Code								Instructions
				RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	
IR	Index	W	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SR	Status Read	R	0	L7	L6	L5	L4	L3	L2	L1	L0	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
R00h	Oscillation Start	W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
	Device Code Read	R	1	1	0	0	0	0	0	1	1	*	0	0	0	1	0	0	1	
R01h	Driver Output Control	W	1	0	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	*	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (1)	NL0 (1)	
R02h	LCD AC driving Control	W	1	0	0	0	0	FLD (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
R03h	Entry Mode	W	1	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	HWM (0)	0	0	0	I/D1 (1)	I/D0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
R04h	Compare Register (1)	W	1	0	0	0	CP11 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
R05h	Compare Register (2)	W	1	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	
R07h	Display Control (1)	W	1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
R08h	Display Control (2)	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
R09h	Display Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	
R0Bh	Frame Cycle Adjustment Control	W	1	GD1 (0)	GD0 (0)	SDT1 (0)	SDT0 (0)	CE1 (0)	CE0 (0)	DIV1 (0)	DIV0 (0)	0	0	DM1 (0)	DM0 (0)	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
R0Ch	External Display Interface Control	W	1	0	0	0	0	0	0	0	RM (0)	0	0	0	DM (0)	0	0	RIM1 (0)	RIM0 (0)	
R10h	Power Control (1)	W	1	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	AP2 (0)	AP1 (0)	AP0 (0)	0	DK (1)	SLP (0)	STB (0)	
R11h	Power Control (2)	W	1	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)	
R12h	Power Control (3)	W	1	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
R13h	Power Control (4)	W	1	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
R21h	RAM Address Set	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
R22h	RAM data Write/Read	W	1	RAM WD17-0 /RAM (RD17-0)																
R23h	RAM Write Data Mask (1)	W	1	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)			
R24h	RAM Write Data Mask (2)	W	1	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
R30h	r Control (1)	W	1	0	0	0	0	0	MP 12 (0)	MP 11 (0)	MP 10 (0)	0	0	0	0	0	MP 02 (0)	MP 01 (0)	MP 00 (0)	
R31h	r Control (2)	W	1	0	0	0	0	0	MP 32 (0)	MP P31 (0)	MP 30 (0)	0	0	0	0	0	MP 22 (0)	MP 21 (0)	MP 20 (0)	
R32h	r Control (3)	W	1	0	0	0	0	0	MP52 (0)	MP 51 (0)	MP 50 (0)	0	0	0	0	0	MP 42 (0)	MP 41 (0)	MP 40 (0)	
R33h	r Control (4)	W	1	0	0	0	0	0	CP 12 (0)	CP 11 (0)	CP 10 (0)	0	0	0	0	0	CP 02 (0)	CP 01 (0)	CP00 (0)	
R34h	r Control (5)	W	1	0	0	0	0	0	MN12 (0)	MN11 (0)	MN10 (0)	0	0	0	0	0	MN02 (0)	MN01 (0)	MN00 (0)	
R35h	r Control (6)	W	1	0	0	0	0	0	MN32 (0)	MN31 (0)	MN30 (0)	0	0	0	0	0	MN22 (0)	MN21 (0)	MN20 (0)	
R36h	r Control (7)	W	1	0	0	0	0	0	MN52 (0)	MN51 (0)	MN50 (0)	0	0	0	0	0	MN42 (0)	MN41 (0)	MN40 (0)	
R37h	r Control (8)	W	1	0	0	0	0	0	CN12 (0)	CN11 (0)	CN10 (0)	0	0	0	0	0	CN02 (0)	CN01 (0)	CN00 (0)	
R38h	r Control (9)	W	1	0	0	0	OP14 (0)	OP13 (0)	OP12 (0)	OP11 (0)	OP10 (0)					OP03 (0)	OP02 (0)	OP01 (0)	OP00 (0)	
R39h	r Control (10)	W	1	0	0	0	ON14 (0)	ON13 (0)	ON12 (0)	ON11 (0)	ON10 (0)				SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
R40h	Gate Scan Start Position	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R41h	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	
R42h	First Screen Driving Position	W	1	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	SS17 (0)	
R43h	Second Screen Driving Position	W	1	SE27 (1)	SE26 (1)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (0)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
R44h	Horizontal RAM Address Position	W	1	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	-SA2 (0)	HSA1 (0)	HSA0 (0)	
R45h	Vertical RAM Address Position	W	1	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	

7.7 Instruction Explanation

<table>
<tr><th colspan="5">Input Parts</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM3-1, IM0</td><td>I</td><td>4</td><td>VSSD/ IOVcc</td><td>Select the MPU interface mode as listed below
<table>
<tr><th>IM0(ID)</th><th>IM1</th><th>IM2</th><th>IM3</th><th>MPU interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-bit bus interface,80-system</td><td>DB17-10,8-1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface , 80-system</td><td>DB17-10</td></tr>
<tr><td>ID</td><td>0</td><td>1</td><td>0</td><td>Serial data transfer interface</td><td>DB1-0</td></tr>
<tr><td>*</td><td>1</td><td>1</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-bit bus interface,80-system</td><td>DB17-0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>9-bit bus interface, 80-system</td><td>DB17-9</td></tr>
<tr><td>*</td><td>*</td><td>1</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
</table>
Note: If the serial data transfer interface was selected, IM0 pin is used like the ID setting for the device code in transfer data.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed. Must be connected to VSSD if not in use.</td></tr>
<tr><td>VLD</td><td>I</td><td>1</td><td>MPU</td><td>Fix to VSSD</td></tr>
<tr><td>RS</td><td>I</td><td>1</td><td>MPU</td><td>The signal for register index or register command select.
Low: Regis ter index or internal status (in read operation);
High: Register command.
Connect to IOVcc or VSSD level when serial data transfer interface is selected.</td></tr>
<tr><td>E_NWR</td><td>I</td><td>1</td><td>MPU</td><td>Serves as a write signal and writes data at the rising edge in i80 system interface.
Serves as the synchronous clock signal in serial data transfer interface.</td></tr>
<tr><td>RW_NRD</td><td>I</td><td>1</td><td>MPU</td><td>Low: Write ； High: Read)
Serves as a read signal and reads data at the low level in i80 system interface. Fix it to IOVcc or VSSD level when using serial data transfer interface.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>1</td><td>MPU</td><td>A data ENABLE signal in RGB I/F mode. Fix the unused pin to either the VSSD level or the IOVcc level.
Low: Selected (access enabled)
The polarity of the ENABLE signal is inverted by the EPL bit.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>Enable</td><td>Update</td></tr>
<tr><td>0</td><td>1</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>0</td><td>Disable</td><td>Keep</td></tr>
<tr><td>1</td><td>1</td><td>Enable</td><td>Update</td></tr>
</table></td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame s ynchronizing signal. Fix to the IOVcc level when not used.
If VSPL=0: Active low.
If VSPL=1: Active high.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Frame synchronizing signal. Fix to the IOVcc level when not used.
If HSPL=0: Active low.
If HSPL=1: Active high.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal. Fix to the IOVcc level when not used.
If DPL=0: Data are input on the rising edge of DOTCLK.
If DPL=1: Data are input on the falling edge of DOTCLK.</td></tr>
<tr><td>PD0~17</td><td>I</td><td>18</td><td>MPU</td><td>An 18-bit bus RGB data bus in 80-system interface mode. Fix the unused pins to either the VSSD level or the IOVcc level.
6-bit bus: use PD17-PD12
16-bit bus: use PD17-PD13 and PD11-PD1
18-bit bus: use PD17-PD0</td></tr>
</table>

Input Parts				
Signals	I/O	Pin Number	Connected with	Description
NRESET	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied.
VcomR	I	1	Variable Resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VGAM1OUT and VSSD. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HX8306A.
Vci1	I	1	VciOUT	A reference voltage for the step-up circuit1. Connect to an external power supply of 2.75V of less when not using an internal reference voltage.
VLCD	I	1	VLCDC	A power supply for the source driver outputs. A reference voltage for the step-up circuit2
VGH	I	1	VGHC	A power supply for the TFT LCD' s gate driver. Connect to VGHC.
VGL	I	1	VGLC	A power supply for the TFT LCD' s gate driver. Connect to VGLC.
VCL	I	1	VCLC	A power supply for the VcomL level. Connect to VCLC.
TEST1	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
TEST2	I	1	VSSD	A test pin. Make sure to fix it to the VSSD level.
VGS	I	1	VSSD or external resistor	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
Vci	I	1	Power supply	For analog power supply. Connect to an external power supply 2.5V~3.3V.
VciLVL	I	1	Power Supply	Generates a reference voltage (VciOUT, REGP) from the VciLVL level according to the ratio determined by the VC2-0 BITS. Connect to Vci on the FPC.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	6	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0_SDI	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Input pin in Serial Data Transfer interface. The input data is latched by the rising edge of the SCL signal on the chip.
DB1_SDO	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Output pin in Serial Data Transfer interface. The data is output by the falling edge of the SCL signal on the chip.
DB2~17	I/O	16	MPU	Operates liked a 18-bit bi-directional data bus 8-bit bus: use DB8-DB1 9-bit bus: use DB8-DB0 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 Connected unused pins to the IOVcc or VSSD level.
REGP	I/O	1	Test pin	A test pin for VGAM1OUT. Disconnect it.
VGAM1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM2 between VSSD and VLCD from the reference voltage between Vci and VSSD that is generated internally. VGAM1OUT serves as a source driver grayscale reference voltage VGAM2, a VcomH level reference voltage, and a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT = 3.0 ~ (VLCD – 0.5)V
VTESTS	I/O	1	Open	A test pin. Disconnect it.
TVCOMHI	I/O	1	Open	A test pin for VcomH. Disconnect it.
TVCOMLI	I/O	1	Open	A test pin for VcomL. Disconnect it.
TVMAG	I/O	1	Open	A test pin for VcomL. Disconnect it.
TESTO1~4	-	4	-	Dummy pads. Disconnect them.
DUMMY1,2,13	-	3	-	Dummy pads. Disconnect them.
DUMMY3-12,14-19	-	16	-	Dummy pads. Can be connected to the wiring to the COG panel.
DUMMYR1-9	-	9	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3, DUMMYR4 and DUMMYR5 are short-circuited within the chip. DUMMYR6, DUMMYR7, DUMMYR8, and DUMMYR9 are short circuited within the chip.
VGLDUM1~4	-	4	-	Outputs the internal VGL level. Use as dummy gate output pins.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B	I/O	2	Step-up Capacitor	Connect to the step-up capacitors according to the step-up factor. Leave this pin open if the internal step-up circuit is not used.
C21A,C21B C22A,C22B	I/O	6	Step-up Capacitor	Connect these pins to the capacitors for the step-up circuit 2. According to the step-up rate. When not using the step-up circuit2, disconnect them.
OSC1,OSC2	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
DB0_SDI	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Input pin in Serial Data Transfer interface. The input data is latched by the rising edge of the SCL signal on the chip.
DB1_SDO	I/O	1	MPU	Operates liked an 18-bit bi-directional data bus. 8-bits bus I/F: DB17-10 9-bits bus I/F: DB17-9 16-bits bus I/F: DB17-10, 8-1 18-bits bus I/F: DB17-0 Connected unused pins to the IOVcc or VSSD level. When Serial Data Output pin in Serial Data Transfer interface. The data is output by the falling edge of the SCL signal on the chip.
DB2~17	I/O	16	MPU	Operates liked a 18-bit bi-directional data bus 8-bit bus: use DB8-DB1 9-bit bus: use DB8-DB0 16-bit bus: use DB17-DB10 and DB8-DB1 18-bit bus: use DB17-DB0 Connected unused pins to the IOVcc or VSSD level.
REGP	I/O	1	Test pin	A test pin for VGAM1OUT. Disconnect it.
VGAM1OUT	I/O	1	Stabilizing capacitor or power supply	A reference voltage for VGAM2 between VSSD and VLCD from the reference voltage between Vci and VSSD that is generated internally. VGAM1OUT serves as a source driver grayscale reference voltage VGAM2, a VcomH level reference voltage, and a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VGAM1OUT = 3.0 ~ (VLCD – 0.5)V
VTESTS	I/O	1	Open	A test pin. Disconnect it.
TVCOMHI	I/O	1	Open	A test pin for VcomH. Disconnect it.
TVCOMLI	I/O	1	Open	A test pin for VcomL. Disconnect it.
TVMAG	I/O	1	Open	A test pin for VcomL. Disconnect it.
TESTO1~4	-	4	-	Dummy pads. Disconnect them.
DUMMY1,2,13	-	3	-	Dummy pads. Disconnect them.
DUMMY3-12,14-19	-	16	-	Dummy pads. Can be connected to the wiring to the COG panel.
DUMMYR1-9	-	9	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3, DUMMYR4 and DUMMYR5 are short-circuited within the chip. DUMMYR6, DUMMYR7, DUMMYR8, and DUMMYR9 are short circuited within the chip.
VGLDUM1~4	-	4	-	Outputs the internal VGL level. Use as dummy gate output pins.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
Vcc	-	1	Power supply	A power supply for the internal logic. VCC = 2.4 ~ 3.3V
IOVcc	-	1	Power supply	Power supply for internal core logic when VDC is disabled. Voltage range: 1.65 ~ 3.3V if VDC is disabled. Tie together with VCC if VDC is enabled.
VSSA	-	1	Power supply	Analogy ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSD	-	1	Power supply	Ground for the internal RAM. VSSD = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
V0P,V61P	I or O	2	Stabilizing capacitor	Outputs from the internal positive polarity operational amplifier when it is on (when SAP2-0 = "001", "010", "011", "100", and "101"). Connect to a capacitor to stabilize the amplifier.
V0N,V61N	I or O	2	Stabilizing capacitor	Outputs from the internal negative polarity operational amplifier when it is on (when SAP2-0 = "001", "010", "011", "100", and "101"). Connect to a capacitor to stabilize the amplifier

7.8 Reset Function

Te 8309-A is internally initialized by NRESET input. During the reset period, no instruction or GRAM data access from MPU can be accepted. The reset input must be held for at lease 1ms. Do not access the GRAM or initially set the instruction until the R-C oscillation frequency is stable after power has been supplied(10ms).

8 Timing Characteristics

8.1Timing Characteristics

Read / Write Characteristics (8080-series MPU)

80-system (18/16 Bit))Bus Timing Characteristics

<<Normal Write Mode(HWM=0),IoVcc=1.65V-2.4V / VCC=2.4~3.3V >>

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	350	-	-
	Read	tCYCR	ns	500	-	-
Write low-level pulse width		PWLW	ns	40	-	-
Read low-level pulse width		PWLR	ns	250	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	200	-	-
Write/Read rise/fall time		tWRr,WRf	ns	-	-	25
Set up time	(RS to NCS,E_NWR)	tAS	ns	5	-	T.B.D
	(RS toNCS,RE_NRD)		ns	5	-	-
Address hold time		tAH	ns	5	-	-
Write data set up time		tDSW	ns	15	-	-
Write data hold time		tH	ns	15	-	-
Read data delay time		tDDR	ns	-	-	200
Read data hold time		tDHR	ns	5	-	-

<<Normal Write Mode(HWM=0),IoVcc2.4V-3.3V / VCC=2.4~3.3V >>

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	300	-	-
	Read	tCYCR	ns	500	-	-
Write low-level pulse width		PWLW	ns	40	-	-
Read low-level pulse width		PWLR	ns	250	-	-
Write high-level pulse width		PWHW	ns	30	-	-
Read high-level pulse width		PWHR	ns	200	-	-
Write/Read rise/fall time		tWRr,WRf	ns		-	25
Set up time	(RS to CS*,WR*)	tAS	ns	-	-	-
	(RS to RD*)		ns	5	-	-
Address hold time		tAH	ns	5	-	-
Write data set up time		tDSW	ns	15	-	-
Write data hold time		tH	ns	15	-	-
Read data delay time		tDDR	ns	-	-	80
Read data hold time		tDHR	ns	5	-	-

<<High-Speed Write Mode(HWM=1),IoVcc = 1.65V-2.4V / VCC=2.4V~3.3V>>

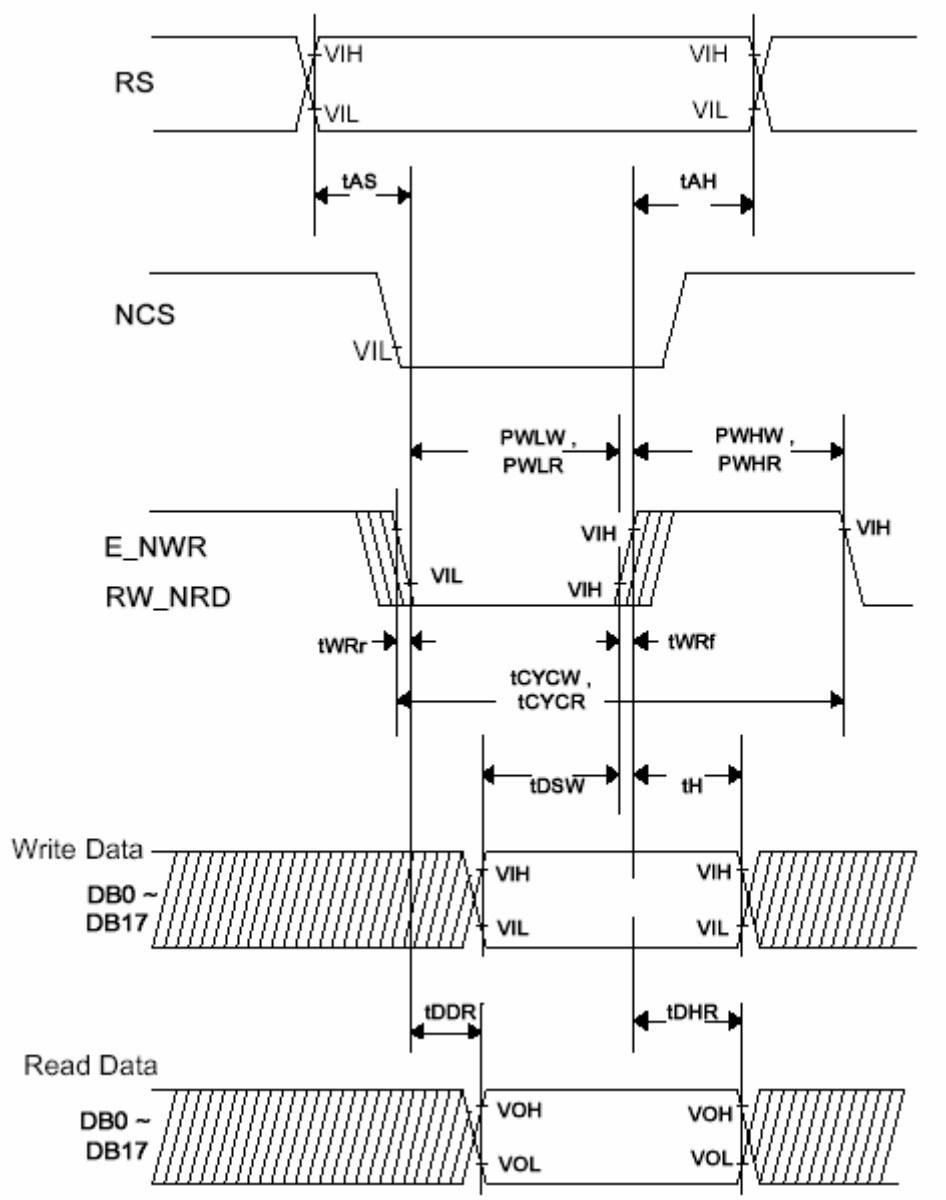
Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	100	-	-
	Read	tCYCR	ns	500	-	-
Write low-level pulse width		PWLW	ns	40	-	-
Read low-level pulse width		PWLR	ns	250	-	-
Write high-level pulse width		PWHW	ns	30	-	-
Read high-level pulse width		PWHR	ns	200	-	-
Write/Read rise/fall time		tWRr,WRf	ns	-	-	25
Set up time	(RS to NCS,E_NWR)	tAS	ns	5	-	-
	(RS toNCS,RE_NRD)		ns	5	-	-
Address hold time		tAH	ns	5	-	-
Write data set up time		tDSW	ns	15	-	-
Write data hold time		tH	ns	20	-	-
Read data delay time		tDDR	ns	-	-	200
Read data hold time		tDHR	ns	5	-	-

<<High-Speed Write Mode(HWM=1),IoVcc = 2.4V-3.3V / Vcc=2.4~3.3V >>

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	tCYCW	ns	100	-	-
	Read	tCYCR	ns	500	-	-
Write low-level pulse width		PWLW	ns	40	-	-
Read low-level pulse width		PWLR	ns	250	-	-
Write high-level pulse width		PWHW	ns	30	-	-
Read high-level pulse width		PWHR	ns	200	-	-
Write/Read rise/fall time		tWRr,WRf	ns	-	-	25
Set up time	(RS to CS*,WR*)	tAS	ns	5	-	-
	(RS to RD*)		ns	5	-	-
Address hold time		tAH	ns	5	-	-
Write data set up time		tDSW	ns	15	-	-
Write data hold time		tH	ns	20	-	-
Read data delay time		tDDR	ns	-	-	200
Read data hold time		tDHR	ns	5	-	-

Reset Timing Characteristics

Item	Symbol	Unit	Min	Typ	Max
Reset"low"level width	tRES	ms	1	-	-
Reset rise time	trRES	us	-	-	10

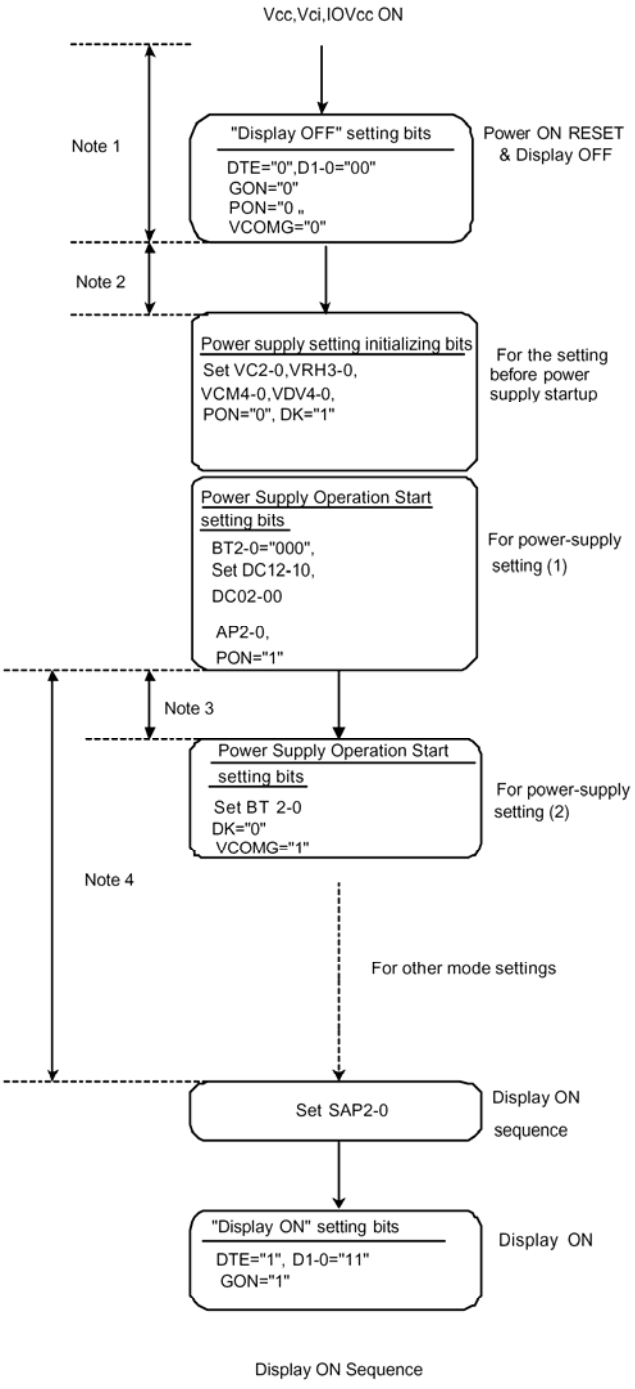


80-System Bus Timing

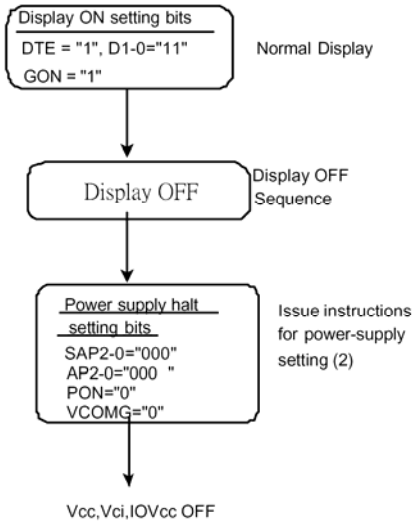
Note 1) PWEL is specified during the overlap period. (SC*="Low", WR* or RD*="Low")

Note 2) When using 16-bit bus interface, parallel data can be transferred through DB17-10 pin and DB8-1 and DB0 must be fixed to "Vcc" or "GND".

9 SETUP FLOW OF POWER SUPPLY

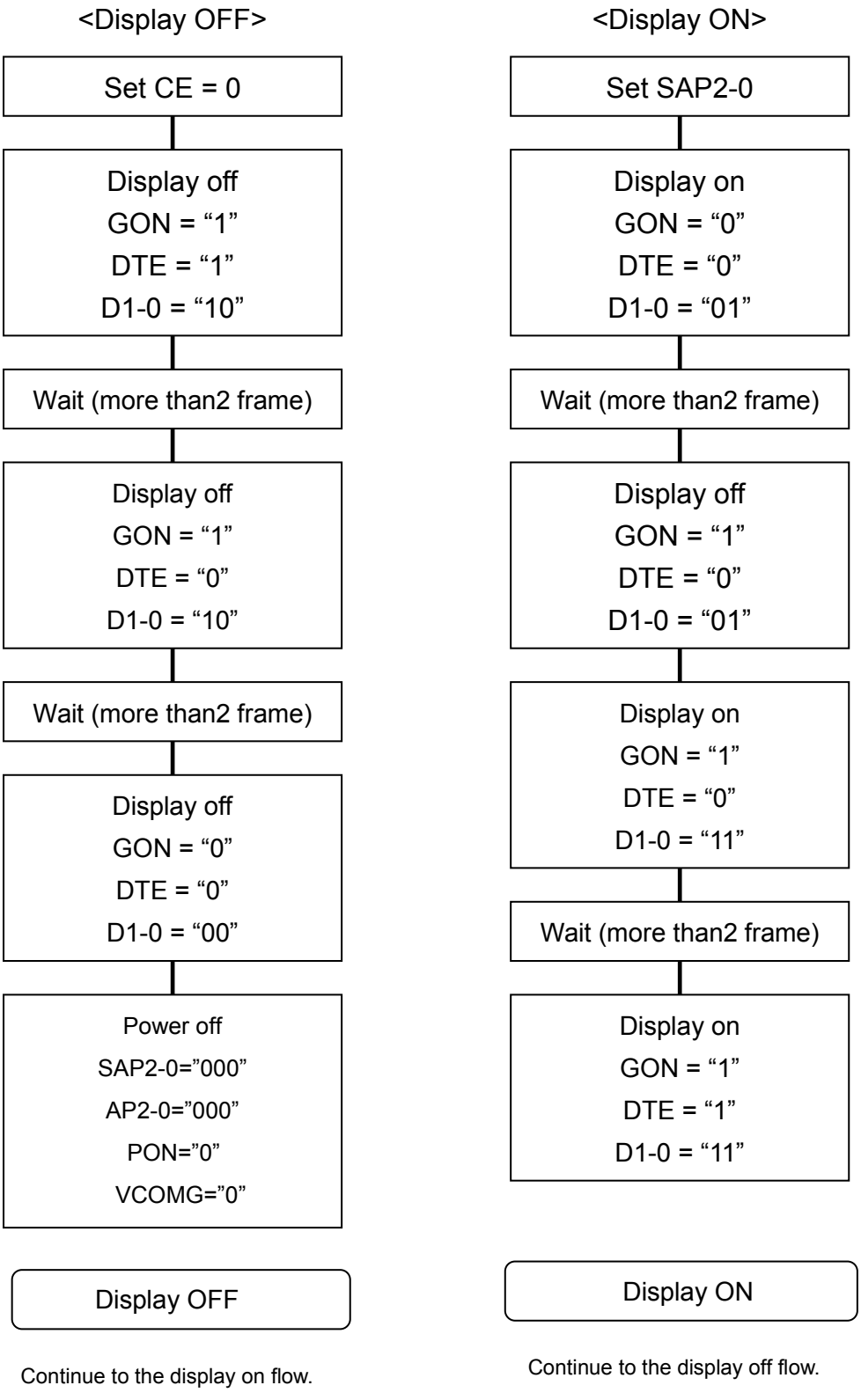


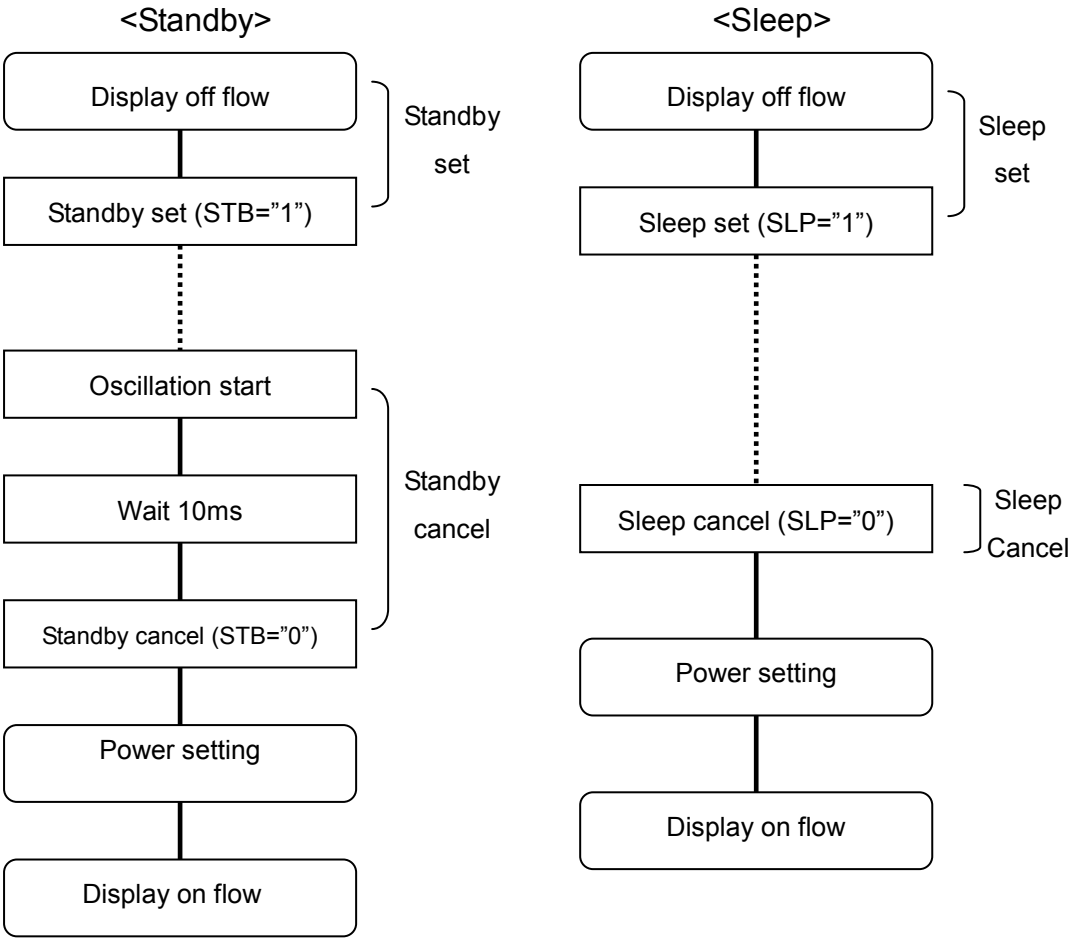
Display ON Sequence



Display OFF Sequence

10 INSTRUCTION SETUP FLOW




<Standby>
Display off flow
Standby set (STB="1")
Standby set
Oscillation start
Wait 10ms
Standby cancel (STB="0")
Standby cancel
Power setting
Display on flow
<Sleep>
Display off flow
Sleep set (SLP="1")
Sleep set
Sleep cancel (SLP="0")
Sleep Cancel
Power setting
Display on flow

11 QUALITY AND RELIABILITY

11.1 TEST CONDITIONS

Tests should be conducted under the following conditions :
Ambient temperature : 25 ± 5°C
Humidity : 60 ± 25% RH.

11.2 SAMPLING PLAN

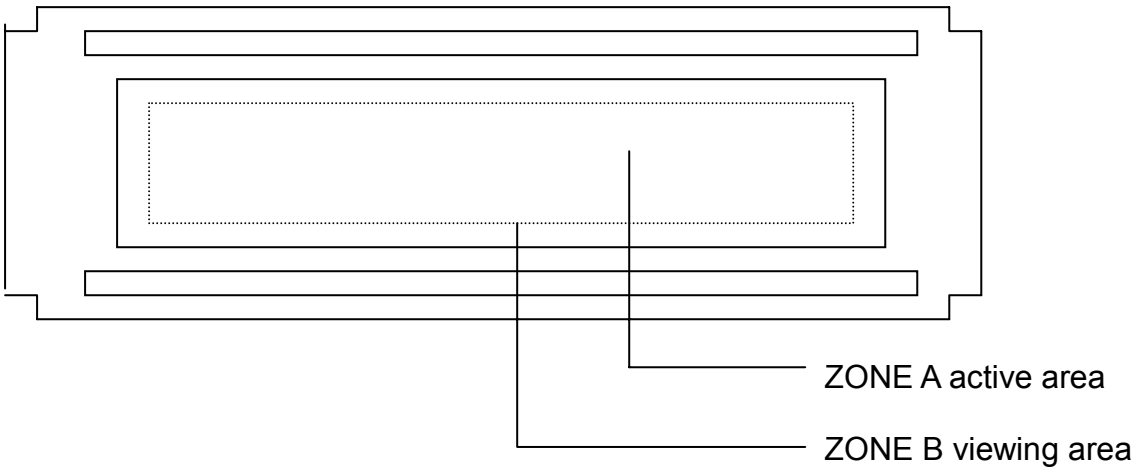
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

11.3 ACCEPTABLE QUALITY LEVEL

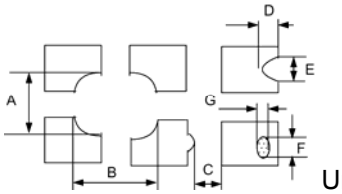
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

11.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



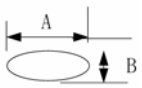
11.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Defect type</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>6</td><td>Black/White line (I)</td><td><table><tr><th>Length(mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>10 < L</td><td>0.03 < W ≤ 0.04</td><td>5</td></tr><tr><td>5.0 < L ≤10</td><td>0.04 < W ≤ 0.06</td><td>3</td></tr><tr><td>1.0 < L ≤ 5.0</td><td>0.06 < W ≤ 0.07</td><td>2</td></tr><tr><td>L ≤ 1.0</td><td>0.07 < W ≤ 0.09</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>7</td><td>Black/White sport (II)</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.30</td><td>Ignore</td></tr><tr><td>0.30 < D ≤ 0.50</td><td>5</td></tr><tr><td>0.50 < D ≤ 1.20</td><td>3</td></tr><tr><td>1.20 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>8</td><td>Black/White line (II)</td><td><table><tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>20 < L</td><td>0.05 < W ≤ 0.07</td><td>5</td></tr><tr><td>10 < L ≤ 20</td><td>0.07 < W ≤ 0.09</td><td>3</td></tr><tr><td>5.0 < L ≤ 10</td><td>0.09 < W ≤ 0.10</td><td>2</td></tr><tr><td>L ≤ 5.0</td><td>0.10 < W ≤ 0.15</td><td>1</td></tr></table></td><td>Minor</td></tr>
<tr><td>9</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable</td><td>Major</td></tr>
<tr><td>10</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there’re to two or more pinholes per dot</td><td>Minor</td></tr>
</table>

<table>
<tr><td>11</td><td>Blemish & Foreign matters

Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.15</td><td>Ignore</td></tr><tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr><tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr><tr><td>0.30 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>12</td><td>Scratch on Polarizer

  </td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>Ignore</td><td>Ignore</td></tr><tr><td>0.03<W≤0.05</td><td>L ≤ 2.0</td><td>Ignore</td></tr><tr><td></td><td>L > 2.0</td><td>1</td></tr><tr><td>0.05<W≤0.08</td><td>L > 1.0</td><td>1</td></tr><tr><td></td><td>L ≤ 1.0</td><td>Ignore</td></tr><tr><td>0.08<W</td><td>Note (1)</td><td>Note(1)</td></tr></table>Note(1) Regard as a blemish</td><td>Minor</td></tr>
<tr><td>13</td><td>Bubble in polarizer</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.20</td><td>Ignore</td></tr><tr><td>0.20 < D ≤ 0.50</td><td>3</td></tr><tr><td>0.50 < D ≤ 0.80</td><td>2</td></tr><tr><td>0.80 < D</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>14</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td></tr>
<tr><td>15</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td></tr>
<tr><td>16</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td></tr>
<tr><td>17</td><td>Parts mounting</td><td>1. Failure to mount parts
2. Parts not in the specifications are mounted
3. Polarity, for example, is reversed</td><td>Major
Major
Major</td></tr>
<tr><td>18</td><td>Parts alignment</td><td>1. LSI, IC lead width is more than 50% beyond pad outline.
2. Chip component is off center and more than 50% of the leads is off the pad outline.</td><td>Minor

Minor</td></tr>
<tr><td>19</td><td>Conductive foreign matter (Solder ball, Solder chips)</td><td>1. 0.45< φ ,N≧1
2. 0.30< φ ≤0.45 ,N≧1
φ :Average diameter of solder ball (unit: mm)
3. 0.50<L ,N≧1
L: Average length of solder chip (unit: mm)</td><td>Major
Minor

Minor</td></tr>
<tr><td>20</td><td>Faulty PCB correction</td><td>1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB.
2. Short circuited part is cut, and no resist coating has been performed.</td><td>Minor

Minor</td></tr>
</table>

11.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

12 USE PRECAUTIONS

12.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

12.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

12.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

12.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that

they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

12.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

13 MECHANIC DRAWING