A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

2.2-in COLOR TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A M - 2 4 0 3 2 0 J 1 T N Q W - 0 0 H
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2006/7/14	-	New Release	Tony
2007/3/21	6	Modify LED back light specification	Tony
2007/4/18	7,8,9	Modify LED back light specification and optical characteristics	Tony
200//6/8	37	Modify Mechanic Drawing	Tony
2007/7/6	30,31	Modify Inspection quality criteria	Tony
2007/7/17	30,31	Modify Inspection quality criteria	Tony

1 Features

This single-display module is suitable for cellphone application. The Main-LCD adopts one backlight with High brightness 3-lamps white LED.

(1) Main LCD : 1.1 Amorphous-TFT 2.2 inch display, transmissive, Normally white type, 12 o'clock.
1.2 240(RGB) X 320 dots Matrix,1/320 Duty.
1.3 Narrow-contact ledge technique.
1.4 Main LCD Driver IC: HX8312A
1.5 Real 262K colors display:
65K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)
262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)

(2) Low cross talk by frame rate modulation
(3) Direct data display with display RAM
(4) Partial display function: You can save power by limiting the display space.
(5) MPU interface: Serial interface.
(6) RGB interface:16bit parallel interface
(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*56.9 (W) x 40.1 (H) x 3.65 (D) Max.	mm
Main LCD	Pixel pitch	0.1395 (W) x 0.1395(H)	mm
	Active area	33.48 (W) x 44.64 (H)	mm
	Viewing area	35.24 (W) x 46.92 (H)	mm
Weight		15	g

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4.0	V	
Power voltage	LED A – LED K	-0.5	+12.8	V	
Input voltage	VIN	-0.5	VDD+0.5	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +70 °C Min. -20 °C	Note 1: Non-condensing
Operating temperature	Max. +60 °C Min. -10 °C	Note 1: Non-condensing

Note 1：Ta≦+40 °C・・・・Max.85%RH

Ta＞+40 °C・・・・The max. humidity should not exceed the humidity with 40 °C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 °C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
IC power voltage	V_{DD}		2.4	3.0	3.3	V	
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V	Note 1,2,3
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V	
Consumption current of VDD	I_{DD}	LED OFF	-	4		mA	
Consumption current of LED	I_{LED}	V_{LED}=9.6V	-	15	20	mA	

※ 1. 1/320 duty.

2. Electronic Volume value: (xxxxh) Decimal

3. Thermal Gradient: -0.05%/°C

4. Range of Electronic Volume control: (xxxxH±3) Decimal

***Reference only.**

(Note1) The Vci is the DC/DC converter power input. The limitation of the HX8312 are

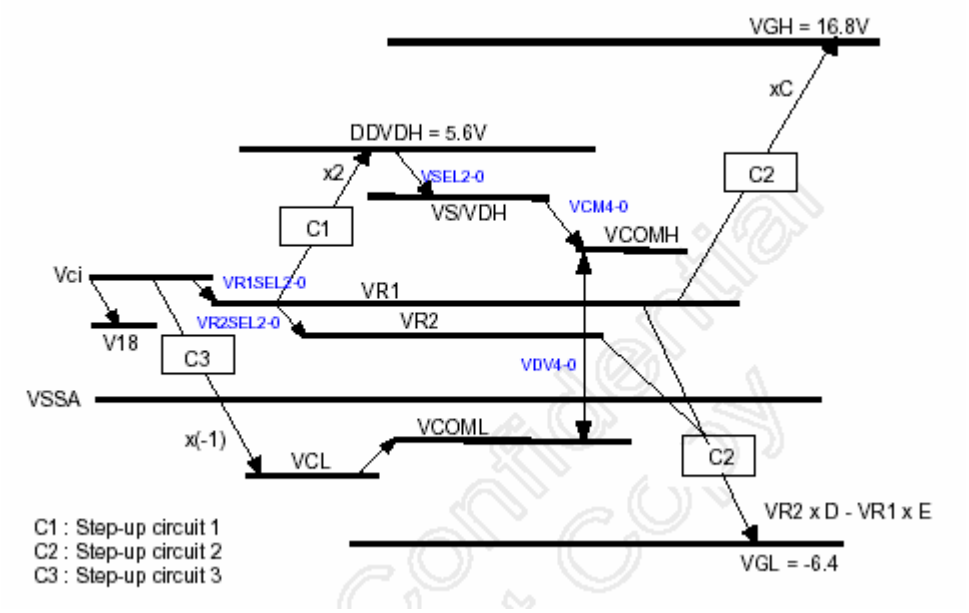
DDVDH<5.6V , VGH-VGL < 32V.

(Note2) When VCI > 3.16V,

R27 Register: VR1SEL2-0 can not be set to 000 or 001 or 010. Otherwise the DDVDH > 5.6V.

R25 Register : BT3-0 can not be set to 0000,0001,0010,0011,0100,0101,0110,0111. Otherwise the VGH-VGL > 32V.

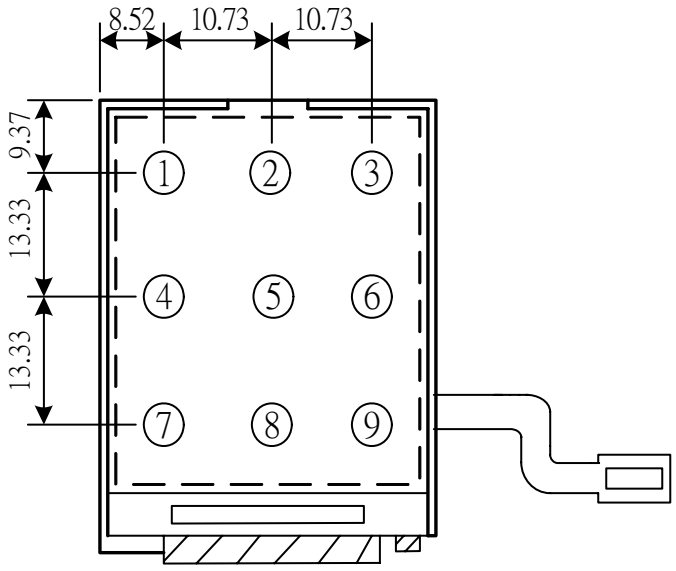
(Note 3) When VCI=3.4V .Recommend setting : VR1SEL2-0=100 , BT3-0=1000.


VGH = 16.8V
xC
DDVDH = 5.6V
x2
VSEL2-0
C2
VS/VDH
VCM4-0
C1
VCOMH
Vci
VR1SEL2-0
VR1
VR2SEL2-0
VR2
V18
C3
VDV4-0
VSSA
VCOML
x(-1)
VCL
C2
VR2 x D - VR1 x E
C1 : Step-up circuit 1
C2 : Step-up circuit 2
C3 : Step-up circuit 3
VGL = -6.4

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =15mA	9.3	9.8	-	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	3-chip serial	12	15	20	mA
Power Consumption	P_{BL}	I_f =15mA	-	147	-	mW
Uniformity (with L/G)	-	I_f=15mA	80%*1	-	-	
Luminous color	White					
Chip connection	3 chip serial connection					

Bare LED measure position:



*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	NA	10	25	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	NA	20	40		
Contrast ratio	CR	25°C	150	200	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	5.5	-	%	
Visual angle range front and rear	θ	25°C	(θf) 35 (θb) 15			De-gree	φ = 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 45 (θr) 45			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			160*			Cd/m2	V_{LED}=9.6V, 15mA Full White pattern

***This value is reference only, follow the limited samples.**

5.2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

Item	Symbol	Tranmissive R G B W Range				Conditions
		X_1Y_1	X_2Y_1	X_1Y_2	X_2Y_2	
Red	X_R	0.55	0.55	0.65	0.65	θ=0°, φ=0°
	Y_R	0.31	0.41	0.31	0.41	
Green	X_G	0.30	0.30	0.40	0.40	θ=0°, φ=0°
	Y_G	0.49	0.59	0.49	0.59	
Blue	X_B	0.09	0.09	0.19	0.19	θ=0°, φ=0°
	Y_B	0.06	0.16	0.06	0.16	
White	X_W	0.26	0.26	0.36	0.36	θ=0°, φ=0°
	Y_W	0.27	0.38	0.28	0.38	

※ **The R G B W ranges are for reference, follow the limited samples.**

LED Dice Bin Code

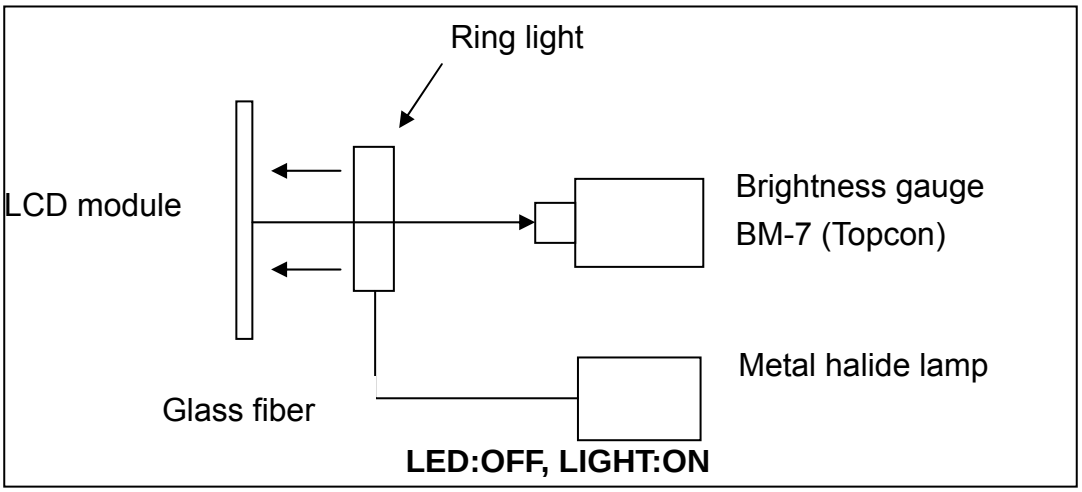
Color Coordinate @ I_f =20mA								
Bin Code	1		2		3		4	
	X	Y	X	Y	X	Y	X	Y
E	0.290	0.290	0.290	0.300	0.300	0.310	0.300	0.300
F	0.290	0.280	0.290	0.290	0.300	0.300	0.300	0.290
G	0.290	0.270	0.290	0.280	0.300	0.290	0.300	0.280

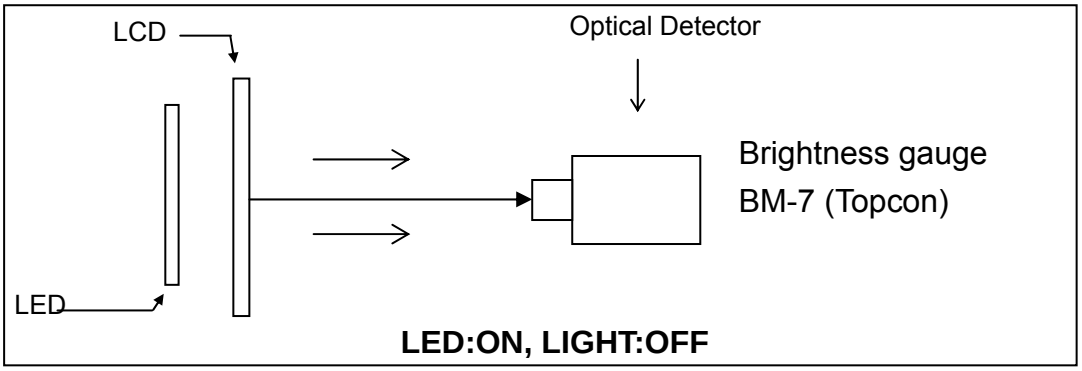
LED Part NO and IV Bin Code:

Unity Opto LED Dice MSL- 518ZW

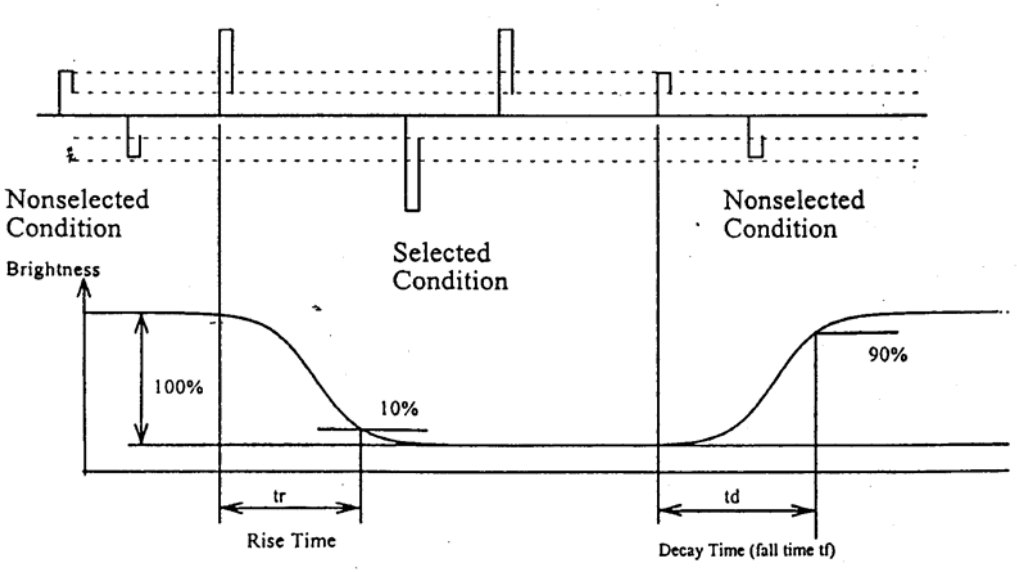
U1B,U2A,U2B

NOTE 1: Optical characteristic measurement system

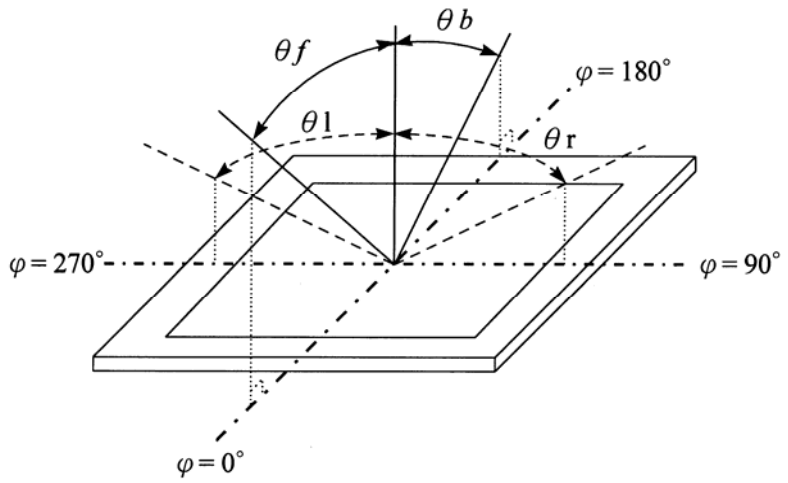




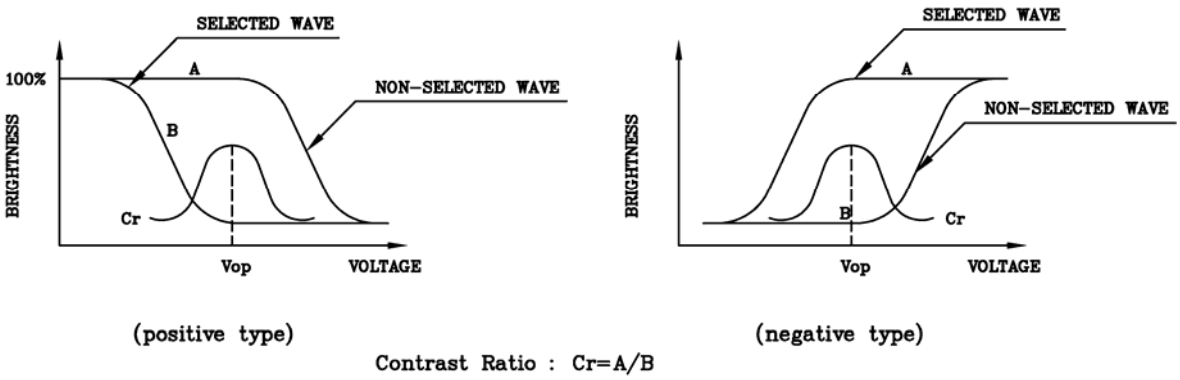
NOTE 2: Response tome definition



NOTE 3: φ 、θ definition

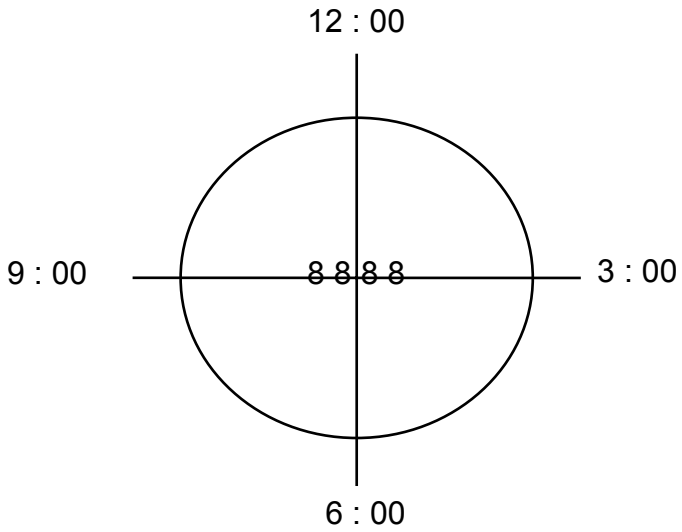


NOTE 4: Contrast definition



Contrast Ratio : Cr=A/B

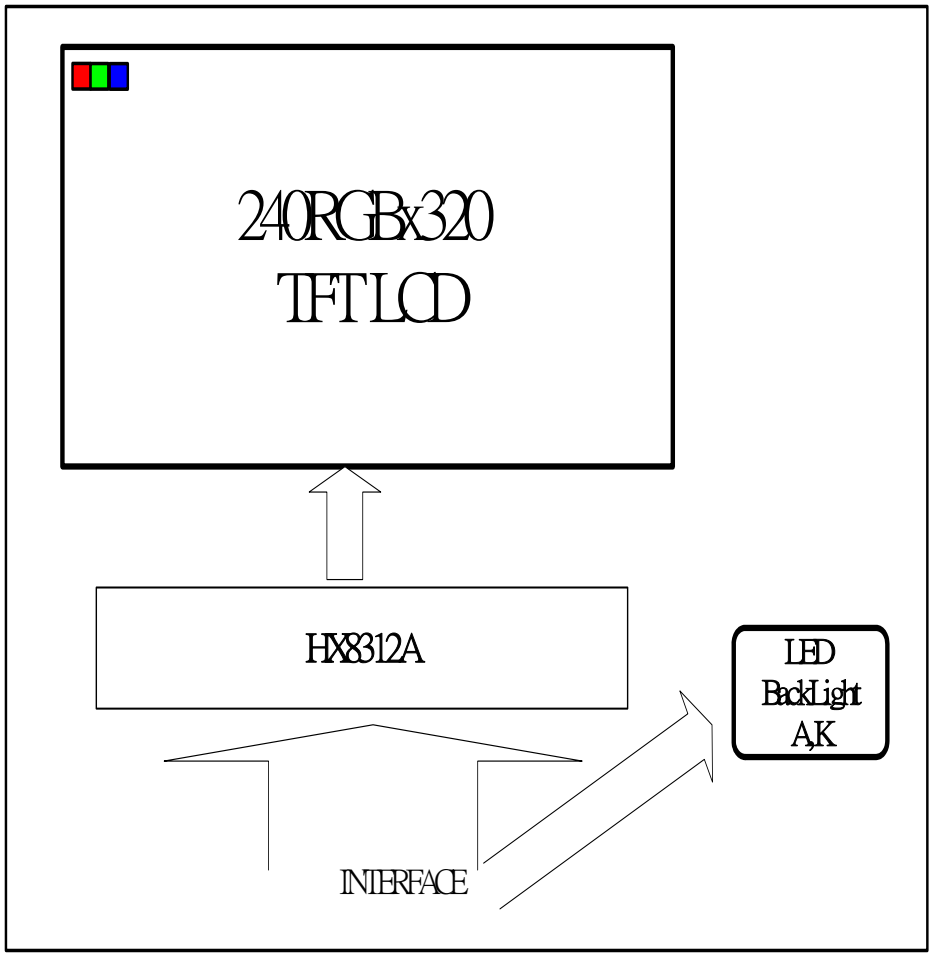
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format:	A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition:	240 RGB x 320 dots
LCD Driver :	HX8312A
Back light:	White LED x 3 (I_{LED}=15mA)



7 Interface specifications

Pin No.	Terminal	Functions
1	GND	Ground
2	GND	Ground
3	/CS	Chip Select Signal L : Select
4	/RS	Command/Display Data selection 0: Command , 1: Display Data
5	/WR	Serves As a Write Signal And Writes Data at The rising edge. M68 System:0:Write 1:Read.
6	/RD	I80 System:Serves as a Read Signal and Reads Data at the Low Level. M68 System:0:Write/Read Disable 1:Read.Write
7	RESET	Reset Signal L : Reset
8	D0	18-bit for Data Bus
9	D1	
10	D2	
11	D3	
12	D4	
13	D5	
14	D6	
15	D7	
16	D8	
17	D9	
18	D10	
19	D11	
20	D12	
21	D13	
22	D14	
23	D15	
24	D16	
25	D17	
26	PSX	The Parallel and Serial Bus Interface selection in system interface circuit 0: Parallel Bus Interface, 1: Serial Bus Bus Interface.
27	NC	No connection
28	LED_A	LED Back-light (+)
29	NC	No connection
30	LED_K	LED Back-light (-)
31	NC	No connection
32	SDI	Serial Data input Pin
33	VCL	Input for Serial Clock
34	VSYNC	Frame Synchronizing Signal
35	HSYNC	Line Synchronizing
36	DOTCLK	Dot Clock Signal

37	NC	No Connect
38	RGB/CPU	Gound Switching For Data Bus 0:System Interface can be accessed. 1:System Interface can Not be accessed.
39	VCC	Power Supply
40	VCI	DC/DC Converter Power

- **The Default FPC setting**

BWS1	VCC
BWS0	VCC
DTX2	VCC
DTX1	VCC
BWS2	VCC

- **Recommend Interface Type Setting :**

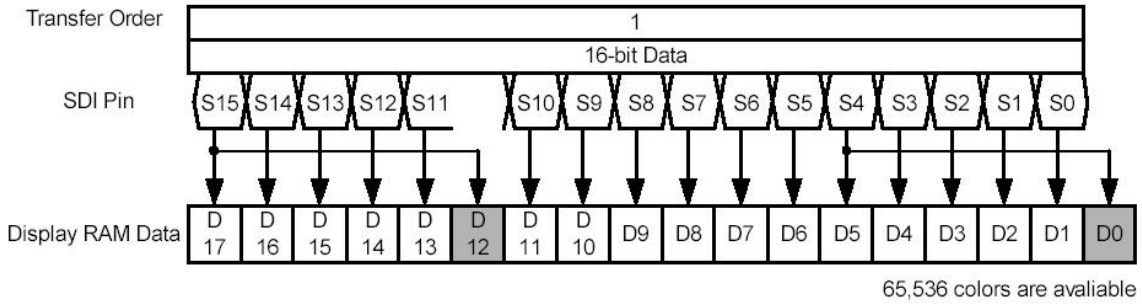
Interface Type	Pin					Bus Width	Bit number in a pixel	Transferring Method	Transferring Method of Command
	PSX	BWS1	BWS0	DTX2	DTX1				
MPU1	0	0	0	x	x	18-bit parallel	18-bits	18-bit collective	16-bit collective
MPU2	0	1	0	0	1	16-bit parallel	18-bits	9-bit twice	
MPU3	0	1	0	1	1			16-bit + 2-bit	
MPU4	0	1	0	0	0		16-bits	16-bit collective	
MPU5	0	1	1	0	1	8-bit parallel	18-bits	6-bit 3 times	8-bit twice
MPU6	0	1	1	1	1			8-bit+8-bit+2-bit	
MPU7	0	1	1	1	0		16-bits	8-bit twice	
MPU8	1	0	1	x	x	18-bit serial	18-bits	18-bit serial	18-bit serial
MPU9	1	1	1	x	x	16-bit serial	16-bits	16-bit serial	16-bit serial

Connect the pin26 PSX to VCC . MPU9 interface type is selected.

The serial bus interface mode is enabled through the chip select input (NCS), and accessed via a three-wire control pin consisting of the serial input data (SDI), serial output data (SDO), and the serial transfer clock (SCL). The selection of read / write operation is made by R/W_nWR pin, and the RS pin specifies whether the access is to the register command or to the display data RAM.

7.1 Data format for 8-bit interface

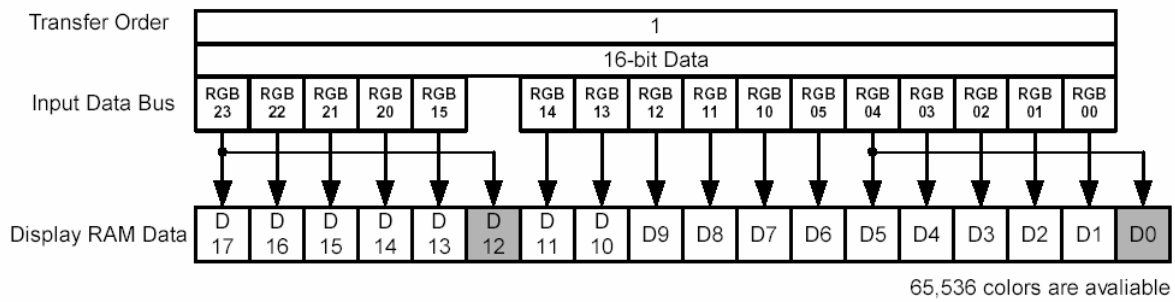
Data format for 16-bit SDI interface



Data format for SDI interface

7.2 RGB interface

16-bit RGB interface



7.3 Instruction Explanation

Input Parts				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
BWS2	I	1	MPU	The bus width selection in RGB interface circuit. 0: 18-bit, 1: 16-bit
BWS1-0		2	MPU	The bus width selection in system interface circuit. (see Table 2.1)
PSX	I	1	MPU	The parallel and serial bus interface selection in system interface circuit. 0: Parallel bus interface, 1: Serial bus interface
NCS	I	1	MPU	Chip select signal. 0: chip can be accessed; 1: chip cannot be accessed.
NRESET	I	1	MPU	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
NRD (E)	I	1	MPU	I80 system: Serves as a read signal and reads data at the low level. M68 system: 0: Read/Write disable ; 1: Read/Write enable Fix it to IOVCC or VSSD level when using serial buss interface.
NWR (RnW)	I	1	MPU	Serves as a write signal and writes data at the rising edge. M68 system: 0: Write ; 1: Read Fix it to IOVCC or VSSD level when using serial bus interface.
C86	I	1	MPU	MPU selection 0: i80 series MPU ; 1: M68 series MPU. Fix it to IOVCC or VSSD level when using serial bus interface.
SI	I	1	MPU	Serial bus interface data input pin. Fix it to IOVCC or VSSD level when using parallel bus interface.
SCL	I	1	MPU	Serial bus interface clock input pin Fix it to IOVCC or VSSD level when using parallel bus interface.
RGB_nCPU	I	1	MPU	0: System interface can be accessed. 1: System interface can not be accessed.
RS	I	1	MPU	Command/display Data Selection 0: Command, 1: Display data Connect to IOVCC or VSSD level when serial bus interface is selected.
DTX2-1	I	2	MPU	Speciy the transferring method of one pixel data in system interface. (see Table 2.3)
SCLEG1-0	I	1	MPU	Determine the effective edge operation of SCLK for SDI data latch and SDO data output. (see Table 2.6)
VSYNC	I	1	MPU	Vertical synchronization signal input pin. Must be connected to IOVCC if not in use.
HSYNC	I	1	MPU	Horizontal synchronization signal input pin. Must be connected to IOVCC if not in use.
DOTCLK	I	1	MPU	Dot clock signal input used in the RGB interface circuit. Must be connected to IOVCC if not in use.
ENABLE	I	1	MPU	Enable signal pin used in RGB interface circuit. 0: disable, 1: enable when EPL (D1 bit of R157) = 0. 0: enable, 1: disable when EPL (D1 bit of R157) = 1. Must be connected to IOVCC if not in use.
VSEG	I	1	MPU	Valid VSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level
HSEG	I	1	MPU	Valid HSYNC polarity selection pin 0: Start in the low level, 1: Start in the high level.
DCKEG	I	1	MPU	Valid DOTCLK polarity selection pin 0: falling edge latch, 1: rising edge latch
DDS	I	1	MPU	Selection the position of dummy line (321th line). 0: the end of the frame, 1: the beginning of the frame

Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
SO	O	1	MPU	Serial bus interface data output pin. Keep it open while using parallel bus interface
CSTB	O	1	MPU	Frame synchronization signal output pin. Keep it open if not in use.
S1~S720	O	720	LCD	Source driver output pin. Output voltages to the liquid crystal.
G1~G321	O	321	LCD	Output signals to panel gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM1~4	O	4	LCD	VCOM output pin. They are short-circuited inside HX8312A.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
DB17-0	I/O	18	MPU	Operates liked an 18-bit bi-directional data bus. Fix it to IOVCC or VSSD level when using serial bus interface. Don't set MPU output as Hi-Z when MPU has no output.
OSC2-1	I/O	2	Oscillation Resistor	Connect an external resistor for generating internal clock by internal R-C oscillation. Or an external clock signal is supplied through OSC1 with OSC2 open.
C11A , C11B CX11A , CX11B	I/O	4	Step up Capacitor	Connect to the step-up capacitors for step up circuit 1 operation. Leave this pin open if the internal step-up circuit is not used.
C21A , C21B C22A , C22B C23A , C23B	I/O	6	Step up Capacitor	Connect to the step-up capacitors for step up circuit 2 operation. Leave this pin open if the internal step-up circuit is not used.
C12A , C12B	I/O	2	Step up Capacitor	Connect to the step-up capacitors for step up circuit 3 operation. Leave this pin open if the internal step-up circuit is not used.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
VCC	I	1	Power supply	A power supply for the internal logic circuit. VCC = 2.2 ~ 3.3V
VCI	I	1	Power supply	A Power supply for step-up circuit and power supply circuit. VCI = 2.5 ~ 3.3V
IOVCC	I	1	Power supply	Power supply for I/O circuit. IOVCC = 1.65 ~ 3.3V
V18	O	1	Bypass capacitor and VDDD, RVCC	1.8V regulator output. V18, VDDD and RVCC must have the same voltage level. Connect to VDDD and RVCC on the FPC.
RVCC	I	1	V18 and VDDD	Power supply for RAM circuit.
VDDD	I	1	V18 and RVCC	Power supply for logic circuit.
VSSD	I	1	Power supply	Ground for digital circuit.
VSSA	I	1	Power supply	Ground for analog circuit.
VGH	O	1	Bypass Capacitor	A positive power supply for the gate line drive circuit.
VGL	O	1	Bypass Capacitor Schottky Diode	A negative power supply for the gate line drive circuit. Insert a schottky diode in a forward direction to VSSA.
ADDVDH	I	1	DDVDH	Power supply pins for VS and COMH regulators. Connected to DDVDH on FPC
DDVDH	O	1	ADDVDH and Bypass Capacitor	Output supply pin. Connected to ADVDDH on FPC.
VDH	O	1	Bypass Capacitor	Power supply for the source drive unit.
VCL	O	1	Bypass Capacitor	The voltage of Vci x (-1) output
VR2-1	O	2	Bypass Capacitor	Reference voltage output for the step-up circuit 2.
VS	O	1	Bypass Capacitor	Power supply for the source drive unit.
VGLDMY	O	1	---	A negative power supply for the gate line drive circuit.

7.4 Register Description

Register	Bit	Symbol	Function	Configuration
	Control register 1			
R0 (R00h) default "A0"h	D7	DISP1	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
	D6	DISP0	Source output data selection.	All source output as "0" or "1" selection Refer to "10.2 " All "0" or "1" Source Output Display "
	D5	ADC	Specifies source output and display RAM address mapping .	Refer to 4.1 "Relation between the Display RAM Address and the Source Output Channel"
	D4	DTY	Specifies partial display mode.	"0" : Normal display mode. "1" : Partial display mode. Refer to "5. Partial Display Mode".
	D3	STBY	Specifies stand-by mode.	"0" : Normal operation. "1" : Stand-by mode.
	D2	COLOR	Specifies color mode.	"0" : 262,144 color mode. "1" : 8 color mode. Refer to "9 8-color Display Mode".
	D1	-	-	-
	D0	GSM	Gate scan selection in partial-off display areas.	"0" : Normal scan in non-display area "1" : Configures the scanning cycle in non-display area by the number of the R52 register.
	Control register 2			
R1 (R01h) default "00"h	D7	ADX	RAM X address increment direction after one write or read operation .	"0" : From X0 to X239 Refer to "4.2. Display RAM Access" "1" : From X239 to X0 *Note : ADX = "1" setting is prohibited when RGB interface circuit is in use.
	D6	ADR	RAM Y address increment direction after one write or read operation .	"0" : Y0 to Y319 Refer to "4.2. Display RAM Access" "1" : Y319 to Y0 *Note : ADR = "1" setting is prohibited when RGB interface circuit is in use.
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	LTS	Specifies setting period of calibration.	"0" : 1line period = tcal "1" : 1 line period = tcal x 2 Refer to "3.3 Internal Clock Mode".
	D0	OSCSTBY	Oscillation control.	"0" : Starts oscillation. "1" : Stops oscillation.
	RGB interface register 2			
R2 (R02h) default "00"h	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	VMODE	Vsync interface selection.	"0" : Normal Refer to "Table 9-1". "1" : Uses Vsync interface.
	D3	WNRGB	RGB interface writing mode selection.	"0" : Requires 1 frame data. "1" : Requires data only for the window area. Refer to "9.1.6 Restriction when using the RGB interface circuit".
	D2	RGBS	RGB interface writing mode selection.	"0" : Capture mode. Refer to "Table 9-1". "1" : Through mode.
	D1	DISPCK	Specifies display timing at RGB interface circuit.	"0" : Internally synchronized display mode by SYSCLK. "1" : Externally synchronized display mode by Vsync and Hsync. Refer to "Table 9-1".
	D0	NWRGB	RGB interface pin control.	"0" : Writes to the display data RAM via the system interface circuit. "1" : Writes to the display data RAM via the RGB interface circuit. Refer to "Table 9-1".

	Reset register 1			
R3 (R03h)	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	RES	Reset command for the HX8312A	"0" : Normal operation. "1" : Reset Operation.
	RAM access control register			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
R5 (R05h)	D4	WAS	Specifies window area access mode.	"0" : Normal writing mode. "1" : Window area access mode. Refer to "4.3. Window Area Access Mode".
	D3	-		
default "00"h	D2	AM	Specifies the address increment direction.	"0" : X address increment, then Y address increment. "1" : Y address increment, then X address increment, *Note: This setting is invalid when RGB interface circuit is in use. Refer to "4.2. Access to the Display Data RAM".
	D1	-	-	-
	D0	-	-	-
	Data reverse register			
	D7	-	-	-
R6 (R06h)	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	REV	Reverse the source output data voltage	"0": Data "0000"h; Source output: V63 at VCOML "1": Data "0000"h; Source output V0 at VCOML
	Display size control register			
	D7	-	-	-
R13 (R0Dh)	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	NSO1	Specify source output size.	Refer to "4.1 Relation between the Display RAM Address and the Source Output Channel".
	D1	NSO0		
	D0	-	-	-
	Partial non-display area color register 1			
	D7	-	-	-
	D6	-	-	-
R14 (R0Eh)	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
default "00"h	D1	-	-	-
	D0	PSEL	Specifies the color of the partial non-display area	"0" : Displays the color specified in the R15 register. "1" : Displays the most significant bit of the display RAM data. Refer to "5.2 Display Color Selection and Gate Scan Method in Partial Non-Display Areas".

R15 (“0F“h) default “00“h	Partial non-display area color register 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	PGR	Specifies display data for pixel R.	"0" : Displays "0". "1" : Displays "1".
	D1	PGG	Specifies display data for pixel G.	"0" : Displays "0". "1" : Displays "1".
	D0	PGB	Specifies display data for pixel B.	"0" : Displays "0". "1" : Displays "1".
R16 (R10h) default “00“h	First display window area starting register 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1SL8	Specify the starting line number of the first display window area.	Set within the range of "000"h - "13F"h.
R17 (R11h) default “00“h	D7	P1SL7		
	D6	P1SL6		
	D5	P1SL5		
	D4	P1SL4		
	D3	P1SL3		
	D2	P1SL2		
	D1	P1SL1		
	D0	P1SL0		
R18 (R12h) default “00“h	Second display window area starting register 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2SL8	Specify the starting line number of the second display window area.	Set within the range of "000"h - "13F"h.
R19 (R13h) default “00“h	D7	P2SL7		
	D6	P2SL6		
	D5	P2SL5		
	D4	P2SL4		
	D3	P2SL3		
	D2	P2SL2		
	D1	P2SL1		
	D0	P2SL0		
R20 (R14h) default “00“h	First display window area display line number 1 , 2			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P1AW8	Specify the display line number of the first display window area.	Set within the range of "001"h - "140"h.
R21 (R15h) default “00“h	D7	P1AW7		
	D6	P1AW6		
	D5	P1AW5		
	D4	P1AW4		
	D3	P1AW3		
	D2	P1AW2		
	D1	P1AW1		
	D0	P1AW0		

R22 (R16h) default "00"h	**Second display window area display line number 1 , 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	P2AW8	Specify the display line number of the second display window area.	Set within the range of 000"h - "13F"h.
R23 (R17h) default "00"h	D7	P2AW7		
	D6	P2AW6		
	D5	P2AW5		
	D4	P2AW4		
	D3	P2AW3		
	D2	P2AW2		
	D1	P2AW1		
	D0	P2AW0		
R24 (R18h) default "00"h	**Power Supply System Control Register 1**			
	D7	VR2ON	Controls the VR2 regulator.	"0" : VR2 regulator off. "1" : VR2 regulator on.
	D6	VR1ON	Controls the VR1 regulator.	"0" : VR1 regulator off. "1" : VR1 regulator on.
	D5	VCLON	Controls the step-up circuit 3 for VCL..	"0" : VCL step-up circuit off. "1" : VCL step-up circuit on.
	D4	VGON	Controls the step-up circuit 2.	"0" : Step-up circuit 2 off. "1" : Step up circuit 2 on.
	D3			
	D2	DDVDHON	Controls the step-up circuit 1 for DDVDH.	"0" : DDVDH step-up circuit off. "1" : DDVDH step-up circuit on.
	D1			
	D0	DCON	Controls the DC/DC converter.	"0" : DC/DC converter off. "1" : DC/DC converter on.
R25 (R19h) default "00"h	**Power Supply System Control Register 2**			
	D7	VR2SEL2	Specify the output voltage of the VR2 regulator.	-
	D6	VR2SEL1		
	D5	VR2SEL0		
	D4	VR1SEL2	Specify the output voltage of the VR1 regulator.	-
	D3	VR1SEL1		
	D2	VR1SEL0		
	D1	-	-	-
	D0	-	-	-
R26 (R1Ah) default "05"h	**Power Supply System Control Register 3**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	FS3	Specify the step-up circuit 2and 3 frequency	-
	D2	FS2		
	D1	FS1	Specify the step-up circuit 1 frequency	-
	D0	FS0		
R27 (R1Bh) default "0A"h	**Power Supply System Control Register 4**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	VSEL2	Specify the output voltage of the VS and VDH regulator.	-
	D2	VSEL1		
	D1	VSEL0		
	D0	RGON	Controls the VS and VDH regulator.	"0" : VS and VDH regulator off. "1" : VS and VDH regulator on.

R28 (R1Ch) default "33"h	Power Supply System Control Register 5			
	D7	-	-	-
	D6	SAP2	Source driver circuit operating current control	(SAP2, SAP1, SAP0) = "000": Halt (SAP2, SAP1, SAP0) = "001": 0.5(fixed) (SAP2, SAP1, SAP0) = "010": 0.75(fixed) (SAP2, SAP1, SAP0) = "011": 1.0(fixed) (SAP2, SAP1, SAP0) = "100": 1.25(fixed) (SAP2, SAP1, SAP0) = "101": 1.5(fixed) (SAP2, SAP1, SAP0) = "110": 1.5(fixed) (SAP2, SAP1, SAP0) = "111": Setting disable
	D5	SAP1		
	D4	SAP0		
	D3	-	-	-
	D2	AP2	Step-up circuit operating current control	(AP2, AP1, AP0) = "000": Halt (AP2, AP1, AP0) = "001": Setting disable (AP2, AP1, AP0) = "010": 0.5(fixed) (AP2, AP1, AP0) = "011": 0.75(fixed) (AP2, AP1, AP0) = "100": 1.0(fixed) (AP2, AP1, AP0) = "101": 1.25(fixed) (AP2, AP1, AP0) = "110": 1.5(fixed) (AP2, AP1, AP0) = "111": Setting disable
	D1	AP1		
	D0	AP0		
R29 (R1Dh) default "03"h	Power Supply System Control Register 6			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	R/L	Specifies the gate scan direction.	-
	D2	SCN2	Specify gate scan mode.	(SCN2, SCN1, SCN0) = "XX0" : MODE5 (SCN2, SCN1, SCN0) = "011" : MODE2
	D1	SCN1		
	D0	SCN0		
R30 (R1Eh) default "00"h	Power Supply System Control Register 8			
	D7	VCOMEN	Specify the VCOM1 operation.	-
	D6			
	D5	VCOMFX		
	D4	VCOMHI		
	D3	XVCOMG	VCOML output control	"0": VCOML = GND "1": VCOML is setting with VDV and VCM
	D2	-	-	-
	D1	-	-	-
	D0	DDVDHXON	Specifies whether to use or not to use the extra step-up circuit 1 for DDVDH.	"0" : Doesn't use the extra step-up circuit 1. "1" : Uses the extra step-up circuit 1.
R31 (R1Fh) default "00"h	Power Supply System Control Register 9			
	D7	-	Specify the VCOM amplitude.	-
	D6	-		
	D5	-		
	D4	VDV4		
	D3	VDV3		
	D2	VDV2		
	D1	VDV1		
	D0	VDV0		
R32 (R20h) default "00"h	Power Supply System Control Register 10			
	D7	-	Specify the VCOMH voltage level	-
	D6	-		
	D5	-		
	D4	VCM4		
	D3	VCM3		
	D2	VCM2		
	D1	VCM1		
	D0	VCM0		

R49 (R31h)	**ID code register 1**			
	D7	MCOD3	Manufacturer code.	-
	D6	MCOD2		
	D5	MCOD1		
	D4	MCOD0		
default "10"h	D3	VCOD3	The version of this LSI.	Depends on the version of the product.
	D2	VCOD2		
	D1	VCOD1		
	D0	VCOD0		
R50 (R32h)	-	-	-	**ID code register 2**
	D7	DCOD7	Device code of this LSI.	-
	D6	DCOD6		
	D5	DCOD5		
	D4	DCOD4		
default "03"h	D3	DCOD3		
	D2	DCOD2		
	D1	DCOD1		
	D0	DCOD0		
R51 (R33h)	D7	**N line inversion register**		
	D6	NLINE6	Specify the number of lines for N line inversion.	Set within the range of "01"h - "78"h. Refer to "7 Gate Line Driving Function".
	D5	NLINE5		
	D4	NLINE4		
	D3	NLINE3		
default "01"h	D2	NLINE2		
	D1	NLINE1		
	D0	NLINE0		
R52 (R34h)	**Partial gate register 1**			
	D7	GSMLN7	Specify the gate scanning cycle of the non-display area	"00"h : Doesn't scan the partial non-display area. "01"h : Scans the partial non-display area every frame. "02"h : Scans the partial non-display area every two frames.
	D6	GSMLN6		
	D5	GSMLN5		
	D4	GSMLN4		
default "01"h	D3	GSMLN3		
	D2	GSMLN2		
	D1	GSMLN1		
	D0	GSMLN0		
R53 (R35h)	**Partial gate register 2**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	PNFRM	Configures the driving method of the partial non-display area.	"0" : The partial non-display area is driven as that in the partial display area. "1" : The partial non-display area is driven by the frame inversion.
R55 (R37h)	**Gate scan selection register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	
default "00"h	D2	GSCAN2	Select the method of gate scanning.	-
	D1	GSCAN1		
	D0	GSCAN0		
R59 (R3Bh)	**Gate output control register**			
	D7	-	-	-
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
default "00"h	D2	-	-	-
	D1	-	-	-
	D0	DISPTMG	Controls the gate output	"0" : Fix all gate outputs to VGL level. "1" : Gate scanning normal operation.

Gamma control register 12				
R154 (R9Ah) default “00“h	D7	-	Gamma adjustment register	-
	D6	-		
	D5	-		
	D4	ON14		
	D3	ON13		
	D2	ON12		
	D1	ON11		
	D0	ON10		
Extend mode register				
R157 (R9Dh) default “00“h	D7	-	-	-
	D6	-	-	-
	D5	MON_EN	Specify the V0 and V63 monitor function	“0”: V0 and V63 output monitor is disable. “1”: V0 and V63 output monitor is enable.
	D4	MON_SEL	V0 and V63 monitor selection	“0”: V0 outputs at DS1 pin. “1”: V63 outputs at DS1 pin
	D3	-	-	-
	D2	BPEN	Specify the Enable operation	“0”: Enable control is available. “1”: VBP/HBP control is enable
	D1	EPL	Specify the Enable polarity	“0”: High active “1”: Low active
	D0	MSBF	NWRGB (R2:D0)="1"	"0" : 18-bit x 1transfer (BWS2="L"). RGB interface type "0" : 16-bit x 1transfer (BWS2="H"). RGB interface type "1" : 6-bit x 3 transfer (BWS2=x). RGB interface type
			NWRGB (R2:D0)="0"	"0" : MPU5 mode A (use lower 6bits). MPU interface type "1" : MPU5 mode B (use upper 6bits). MPU interface type This bit is invalid in other modes.
Off mode register				
R192 (“C0“h) default “00“h	D7	OFFMOD	Specify the Off mode	“0”: Normal mode “1”: Off mode In off mode, only OFFMOD bit can be updated. Other register and the display RAM can not be updated. The display RAM data may not be retained in off mode, and need to rewrite after off mode canceling.
	D6	-	-	-
	D5	-	-	-
	D4	-	-	-
	D3	-	-	-
	D2	-	-	-
	D1	-	-	-
	D0	-	-	-

8 Timing Characteristics

8.1Timing Characteristics

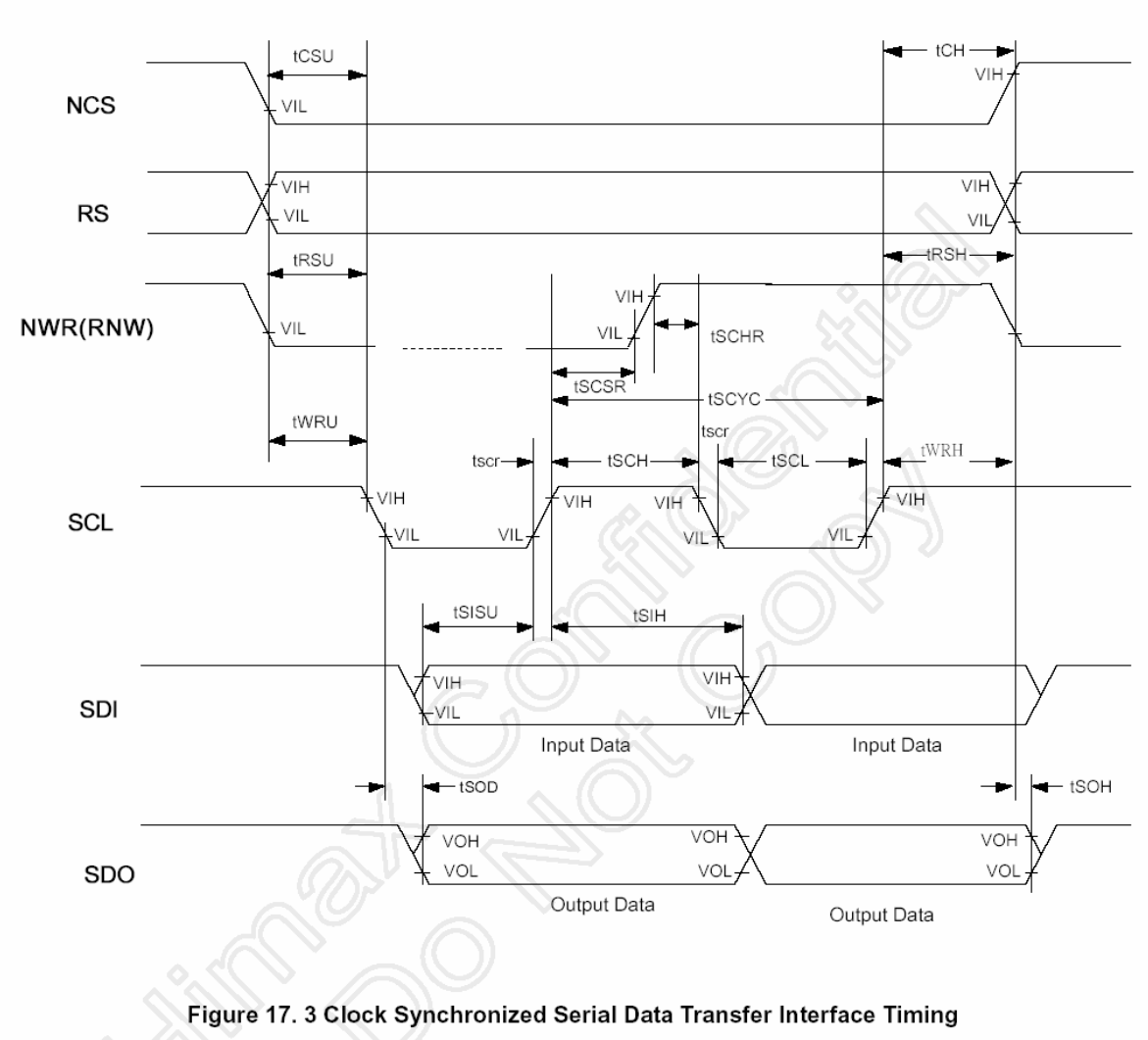
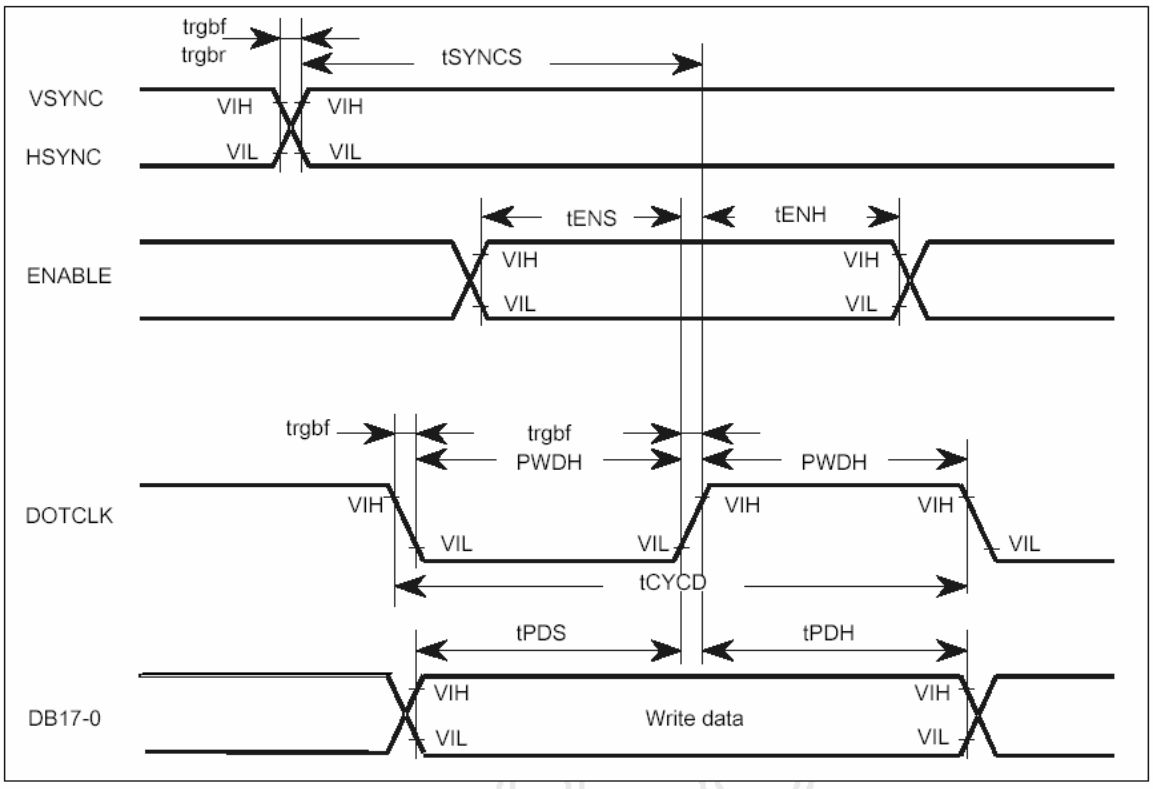


Figure 17. 3 Clock Synchronized Serial Data Transfer Interface Timing

Serial Data Transfer Interface Timing Characteristics

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	-	Figure 17.3
	Read (transmitted)	t_{SCYC}	ns	200	-	-	Figure 17.3
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCH}	ns	150	-	-	Figure 17.3
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	-	Figure 17.3
	Read (transmitted)	t_{SCL}	ns	150	-	-	Figure 17.3
Serial clock rise / fall time		t_{scr} , t_{scf}	ns	-	-	20	Figure 17.3
Chip select (NCS) set up time		t_{CSU}	ns	20	-	-	Figure 17.3
Chip select (NCS) hold time		t_{CH}	ns	60	-	-	Figure 17.3
RS set up time		t_{RSU}	ns	10			Figure 17.3
RS hold time		t_{RSH}	ns	10			Figure 17.3
Read/write select (RNW) set up time		t_{WRU}	ns	10			Figure 17.3
Read/write select (RNW) hold time		t_{WRH}	ns	10			Figure 17.3
Read clock set up time		t_{SCSR}	ns	10			Figure 17.3
Read clock hold time		t_{SCHR}	ns	10			Figure 17.3
Serial input data set up time		t_{SISU}	ns	30	-	-	Figure 17.3
Serial input data hold time		t_{SIH}	ns	30	-	-	Figure 17.3
Serial output data delay time		t_{SOD}	ns	-	-	100	Figure 17.3
Serial output data hold time		t_{SOH}	ns	5	-	-	Figure 17.3

Table 17. 6 (IOVCC=1.65~3.3V) / (VCC = 2.4V~3.3V)



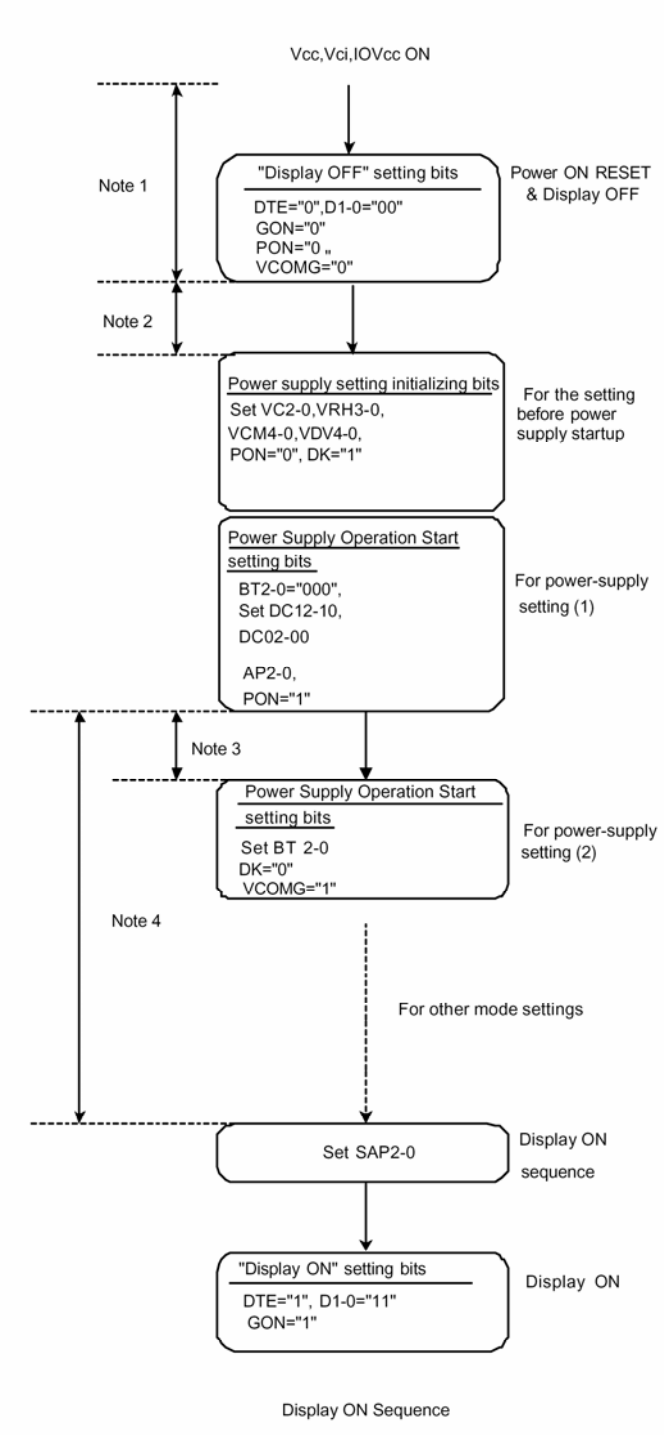
Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC / HSYNC set up time	t_{SYNCS}	ns	10	-	-	Figure 17.4
ENABLE set up time	t_{ENS}	ns	10	-	-	Figure 17.4
ENABLE hold time	t_{ENH}	ns	10	-	-	Figure 17.4
DOTCLK “low” level pulse width	PW_{DL}	ns	40	-	-	Figure 17.4
DOTCLK “high” level pulse width	PW_{DH}	ns	40	-	-	Figure 17.4
DOTCLK cycle time	t_{CYCD}	ns	150	-	-	Figure 17.4
DATA set up time	t_{PDS}	ns	20	-	-	Figure 17.4
DATA hold time	t_{PDH}	ns	20	-	-	Figure 17.4
DOTCLK , VSYNC , HSYNC rising and falling time	t_{rgbr} , t_{rgbf}	ns	-	-	25	Figure 17.4

Table 17. 8 RGB interface mode, Normal Write Mode (IOVCC=2.4~3.3V) / (VCC = 2.4V~3.3V)

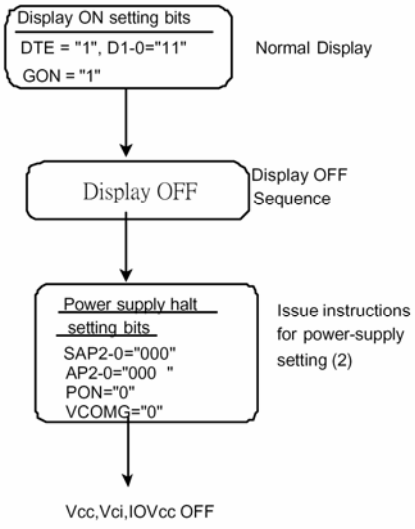
Reset Timing Characteristics

Item	Symbol	Unit	Min	Typ	Max
Reset”low”level width	tRES	ms	(1)	-	-
Reset rise time	trRES	us	-	-	(10)

9 SETUP FLOW OF POWER SUPPLY



Display ON Sequence



Display OFF Sequence

10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

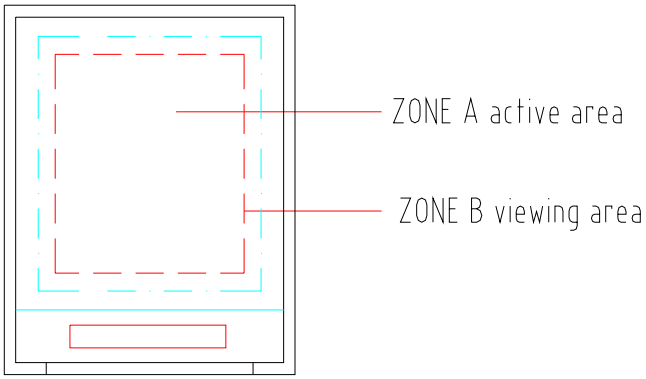
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

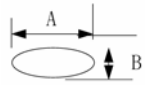
10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



10.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defect</th><th>Acceptable level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>2</td><td>Irregular operation</td><td>No irregular operation is allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>3</td><td>Short</td><td>No short are allowed</td><td>Major</td><td>0.4</td></tr>
<tr><td>4</td><td>Open</td><td>Any segments or common patterns that don’t activate are rejectable.</td><td>Major</td><td>0.4</td></tr>
<tr><td>5</td><td>Black/White spot (I)</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Ignore</td></tr>
<tr><td>0.1 < D ≤ 0.15</td><td>2 ※1</td></tr>
<tr><td>0.15 < D</td><td>0</td></tr>
</table>
※ 1: The distance of two defects must be more than 20mm.
Note: The phenomenon should follow the limit sample.
</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Dot Defect</td><td>
<table>
<tr><td>Bright dot</td><td>0</td></tr>
<tr><td>Dark dot</td><td>N≦2</td></tr>
<tr><td>Total dot defect
(Bright dot + Dark dot)</td><td>N≦2</td></tr>
<tr><td>Minimum distance between dark dot and dark dot</td><td>0.1＜D≦0.3mm,N≦2</td></tr>
</table>
Note: The phenomenon should follow the limit sample.
</td><td>Minor</td><td>1.5</td></tr>
<tr><td>7</td><td>Back Light</td><td>1. No Lighting is rejectable
2. Flickering and abnormal lighting are rejectable
Note: The phenomenon should follow the limit sample.</td><td>Major</td><td>0.4</td></tr>
<tr><td>8</td><td>Blemish & Foreign matters
Size:
$D = \frac{A+B}{2}$</td><td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.15</td><td>Ignore</td></tr>
<tr><td>0.15 < D ≤ 0.20</td><td>3</td></tr>
<tr><td>0.20 < D ≤ 0.30</td><td>2</td></tr>
<tr><td>0.30 < D</td><td>0</td></tr>
</table>
Note1: With 30cm from the LCD surface as testing distance, no scratch should be visible in 10secs as LCM was turned on.
Note2: The phenomenon should follow the limit sample.
</td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr><td>9</td><td>Scratch on Polarizer</td><td><table><tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr><tr><td>W≤0.03</td><td>L ≤ 2.0</td><td>2</td></tr></table>Note1: The distance of two defects must be more than 20mm.
Note2: With 30cm from the LCD surface as testing distance, no scratch should be visible in 10secs as LCM was turned on</td><td>Minor</td><td>1.5</td></tr>
<tr><td>10</td><td>Bubble in polarizer
  </td><td>D ≤0.5 ,N≤ 1
Note: Only one bubble with diameter smaller than 0.5mm is allowed.
The phenomenon should follow the limit sample.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>11</td><td>Stains on LCD panel surface</td><td>Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>12</td><td>Rust in Bezel</td><td>Rust which is visible in the bezel is rejectable.</td><td>Minor</td><td>1.5</td></tr>
<tr><td>13</td><td>Defect of land surface contact (poor soldering)</td><td>Evident crevices which is visible are rejectable.</td><td>Minor</td><td>1.5</td></tr>
</table>

Note: Please follow the above acceptable criteria before the limit samples collect completely.

RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge 150pF 330 ohm ±4kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions

(15-35°C , 45-65%RH).

Definitions of life end point :

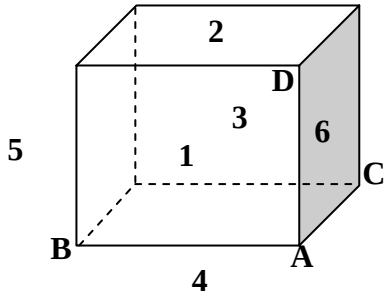
- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

Box Drop Test:

The module test on packing:

Falling body Height and Weight:

Totally Weight	Falling body Height
0 ~ 9 Kg	92 cm
9 ~ 25 Kg	76 cm
25 ~ 45 Kg	53 cm
45 ~ 68 Kg	46 cm
Over68 Kg	41 cm



The dropping test in turns：

1. Conner A
2. Edges of the planes：1-4，1-6， 4-6
3. Planes： 1，2，3，4，5，6

11 USE PRECAUTIONS

11.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light

emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

12 Mechanic Drawing