晶采光電科技股份有限公司
AMPIRE CO., LTD

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	**AM-240320LDTNQW-00H**
APPROVED BY	
DATE	

☑ **Approved For Specifications**
☐**Approved For Specifications & Sample**

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APPROVED BY	CHECKED BY	ORGANIZED BY

A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

2.4-IN COLOR TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A M - 2 4 0 3 2 0 L D T N Q W - 0 0 H
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

9856 SIXTH STREET RANCHO CUCAMONGA CA 91730

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2008/12/31	-	New Release	Emil
2009/01/06	4	Correction the External shape dimensions	Emil
2009/02/13	3	Remove “Touch Panel” in Features	Edward
2009/03/24		Modify Features (6)	Kokai
2009/04/27	24	Correction the Figure 7-19. 16 bit RGB I/F: DB1-DB11, DB13-DB17.	Emil

1 Features

LCD 2.4 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments.

(1) Construction: 2.4" a-Si color TFT-LCD, White LED Backlight and FPCB.
(2) Main LCD : 2.1 Amorphous-TFT 2.4 inch display, transmissive, Normally white type, 12 o'clock.
2.2 240(RGB)X320 dots Matrix,1/320 Duty.
2.3 Narrow-contact ledge technique.
2.4 Main LCD Driver IC: SPFD5408B
2.5 262K: Red-6bit, Green-6bit, Blue-6bit(18-bit interface)
(3) Low cross talk by frame rate modulation
(4) Direct data display with display RAM
(5) Partial display function: You can save power by limiting the display space.
(6) Interface: MPU and RGB Interface. (Select by H/W Jumper). Default : SPI

	JP0(IM0)		JP1(IM1)		JP2(IM2)		JP3(IM3)		Remark
Interface mode	R1(H)	R2(L)	R3(H)	R4(L)	R5(H)	R6(L)	R7(H)	R8(L)	
80-18BIT	NC	0R	0R	NC	NC	0R	0R	NC	
80-9BIT	0R	NC	0R	NC	NC	0R	0R	NC	
80-16BIT	NC	0R	0R	NC	NC	0R	NC	0R	
80-8BIT	0R	NC	0R	NC	NC	0R	NC	0R	
SPI	NC	0R	NC	0R	0R	NC	NC	0R	Default

(7) Abundant command functions:
Area scroll function
Display direction switching function
Power saving function
Electric volume control function: you are able to program the temperature compensation function.

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 43.6 (W) x 85.5 (H) x2.8(T)	mm
Main LCD	Pixel size	0.153 (W) x 0.153 (H)	mm
	Active area	36.72 (W) x 48.96 (H)	mm
	Number of Pixels	240(H)x320(V) pixels	mm
Weight		18.75	g

*1. This specification is about External shape on shipment from AMP DISPLAY

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+3.3	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	Parallel
Input voltage	VIN	-0.5	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80°C Min. -30°C	Note 1: Non-condensing
Operating temperature	Max. +70°C Min. -10°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25 ^{o}C)

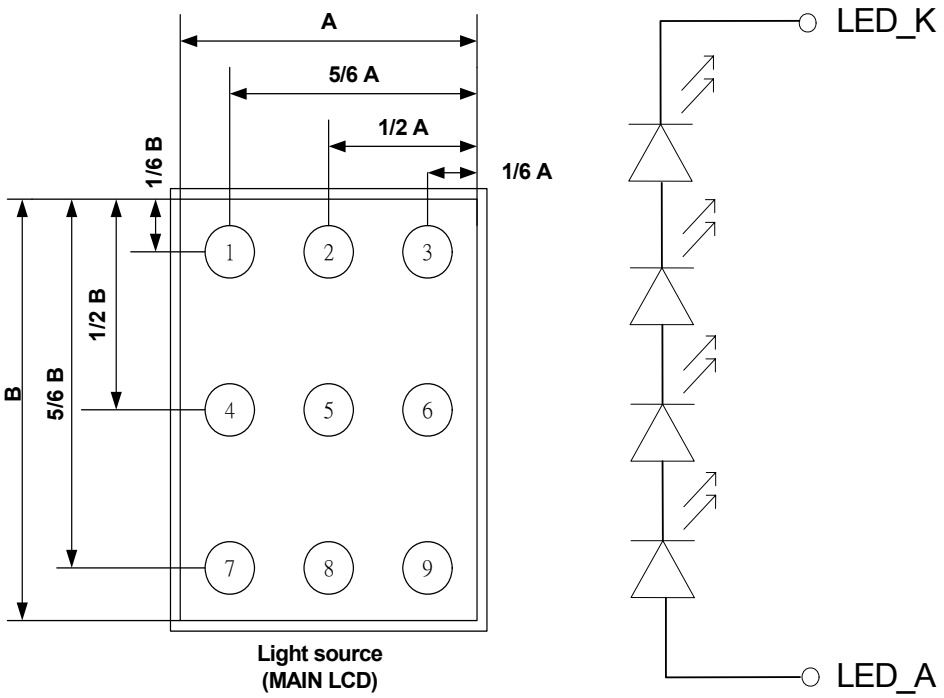
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.6	2.8	3.3	V
High-level input voltage	V_{IHC}		0.8		V_{DD}	V
Low-level input voltage	V_{ILC}		-0.3		0.2V_{DD}	V
Consumption current of VDD	I_{DD}	LED OFF	-	6	10	mA
Consumption current of LED	I_{LED_ON}	V_{LED}=12.8V	-	20	-	mA

※ 1. 1/320 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =20mA	12.3	12.8	13.8	V
Reverse voltage	V_r		-	-	12	V
Forward current	I_f	4-chip serial	-	18	20	mA
Power Consumption	P_{BL}	I_f =20mA	-	256	276	mW
Uniformity (with L/G)	-	I_f=20mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	13.2V 20mA	3700	-	-	cd/m^2
Luminous color	White					
Chip connection	4 chip serial connection					

Bare LED measure position:



*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

5 Main LCD

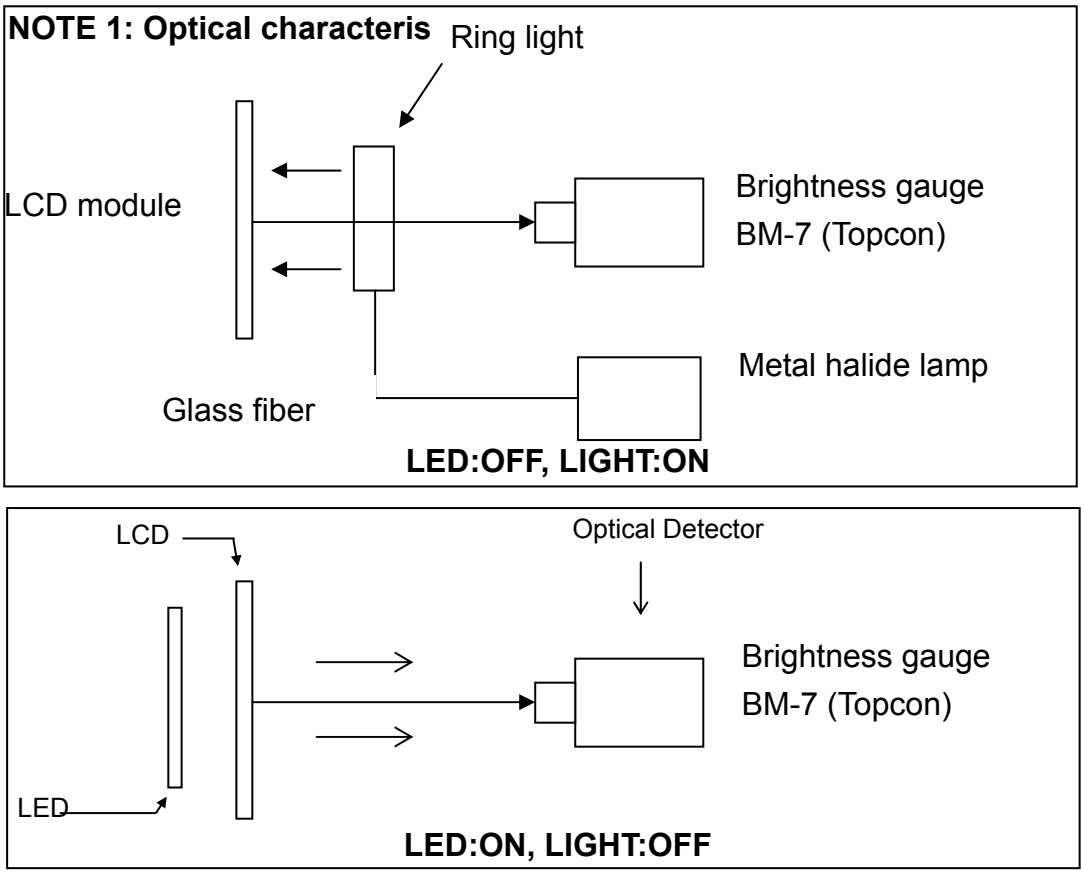
5-1 Optical characteristics

(1/320 Duty in case except as specified elsewhere Ta = 25°C)

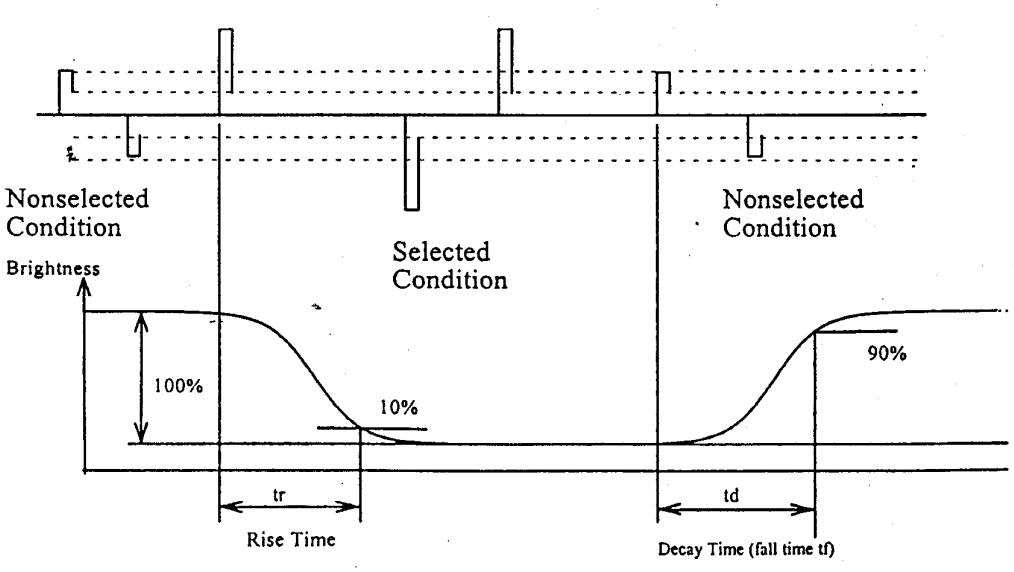
Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	--	15	25	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	--	20	30		
Contrast ratio	CR	25°C	-	200	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	-	4.7	-	%	
Visual angle range front and rear	θ	25°C	(θf) 35 (θb) 65			De-gree	φ= 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) 70 (θr) 70			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			170	220	--	Cd/ m2	I_F=20mA, Full White pattern

5-2 CIE (x, y) chromaticity (1/320 Duty Ta = 25°C)

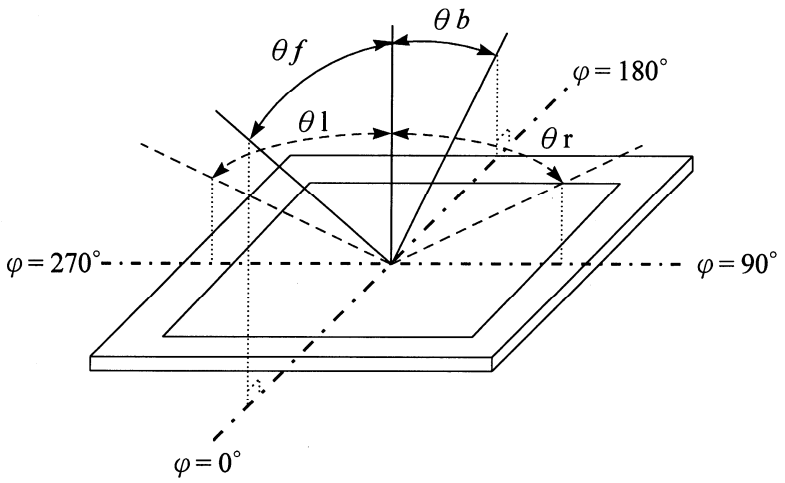
Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	0.5789	0.6289	0.6789	θ=0° ,φ=0°
	Y	0.2946	0.3446	0.3946	
Green	X	0.2968	0.3468	0.3968	θ=0° ,φ=0°
	Y	0.5293	0.5793	0.6293	
Blue	X	0.1095	0.1595	0.2095	θ=0° ,φ=0°
	Y	0.0975	0.1475	0.1975	
White	X	0.261	0.311	0.361	θ=0° ,φ=0°
	Y	0.2971	0.3471	0.3971	



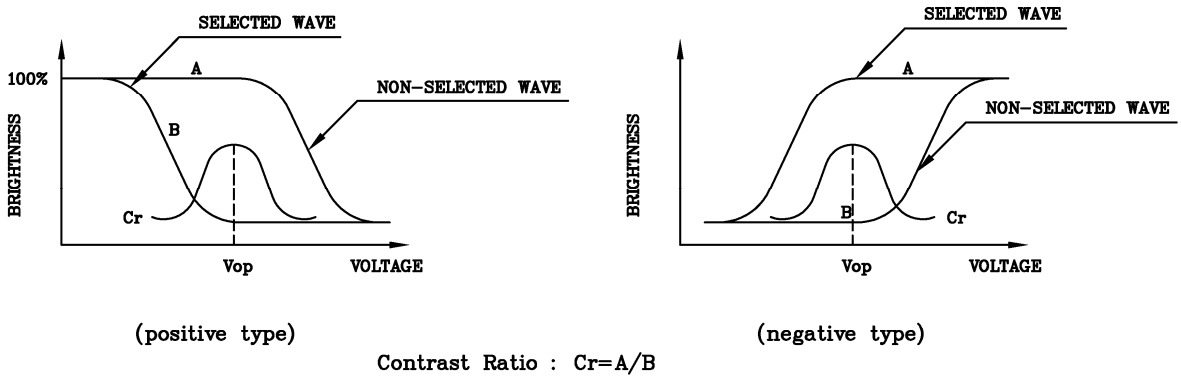
NOTE 2: Response tome definition



NOTE 3: φ、θ definition

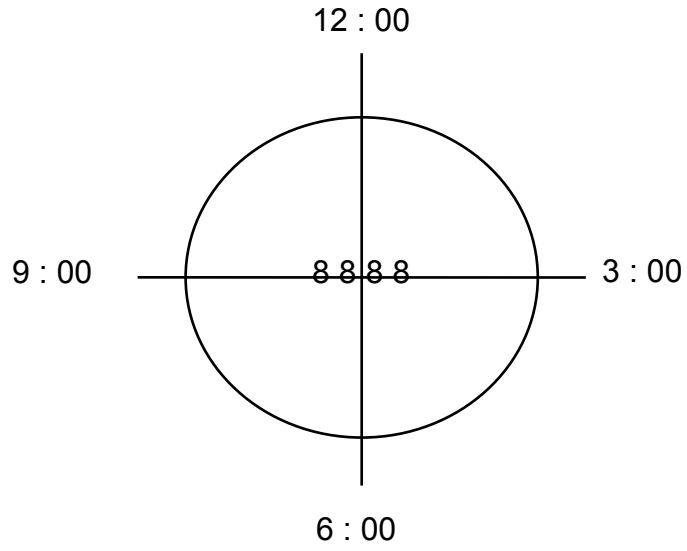


NOTE 4: Contrast definition



Contrast Ratio : Cr=A/B

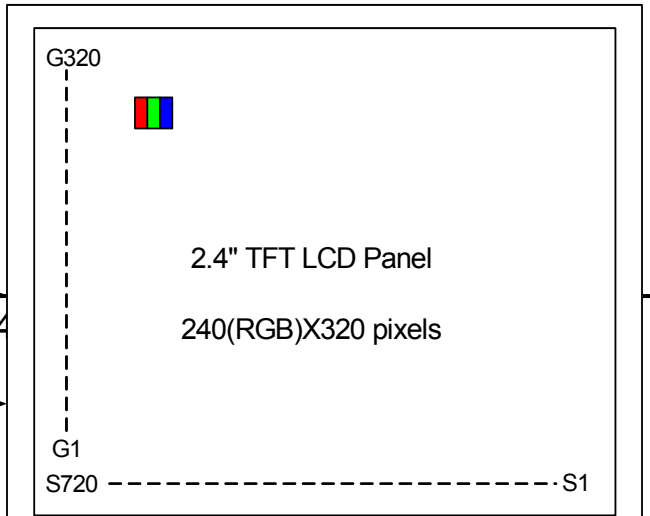
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 240 x RGB x 320 dots
LCD Driver : SPFD5408B



7 Interface specifications

Pin No.	Terminal	Functions
1	ENABLE	A data ENABLE signal in RGB I/F mode.
2	DOTCLK	Dot clock signal in RGB I/F mode.
3	HSYNC	Frame synchronizing signal in RGB I/F mode.
4	VSYNC	Frame synchronizing signal in RGB I/F mode.
5	/CS	Chip select signal.
6	WR/SCL	Write enable signal/Serial bus interface clock input pin.
7	SDI	Serial bus interface data input pin.
8	RS	Command/display Data Selection.
9	NC	NC
10	/RD	Read enable signal.
11	/RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
12	PD0	**Mode** / **DB Pin in use** **MCU 18-bit** / **PD [17:0]**
13	PD1	

14	PD2
15	PD3
16	PD4
17	PD5
18	PD6
19	PD7
20	PD8
21	PD9
22	PD10
23	PD11
24	PD12
25	PD13
26	PD14
27	PD15
28	PD16
29	PD17

MCU 16-bit	**PD [17:10], DB[8:1]**
MCU 9-bit	**PD [17:9]**
MCU 8-bit	**PD [17:10]**
Serial Mode/Digital RGB Interface Mode	**SDI, SDO/ PD [17:0]** **R[5:0]=PD[17:12]** **G[5:0]=PD[11:6]** **B[5:0]=PD[5:0]**

(To be continued)

30	VDD	Power supply for the internal logic circuit. (VDD=2.2~3.3V)
31	VCI	Power supply for Step-up circuit. (VCI=2.5~3.3V)
32	VCI	
33	NC	NC
34	NC	
35	NC	
36	NC	
37	NC	
38	NC	
39	NC	
40	GND	GND-terminal
41	NC	NC
42	NC	
43	NC	
44	NC	
45	GND	GND-terminal
46	SDO	Serial bus interface data output pin.
47	NC	NC
48	NC	
49	NC	
50	GND	GND-terminal
51	GND	

7-1 80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in Figure 7-1 and Figure 7-2, respectively.

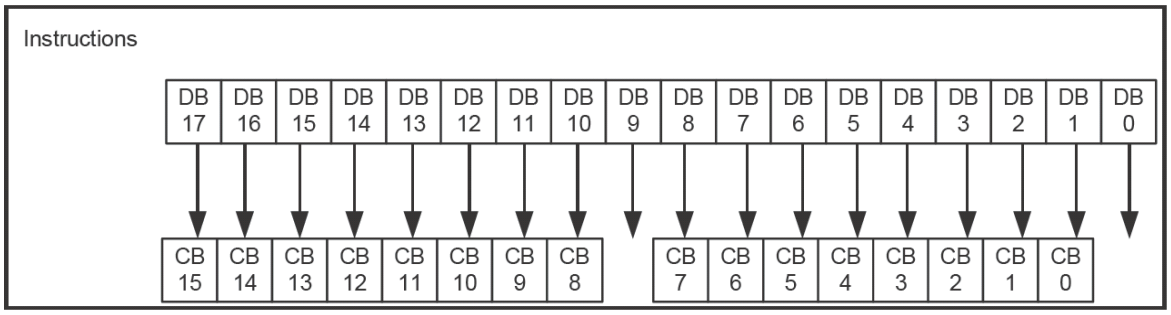


Figure 7-1

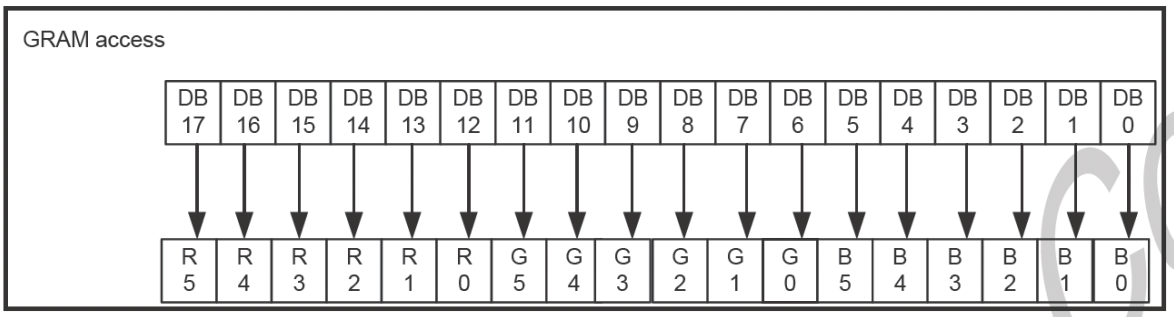


Figure 7-2

7-2 80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in Figure 7-3 and Figure 7-4, respectively.

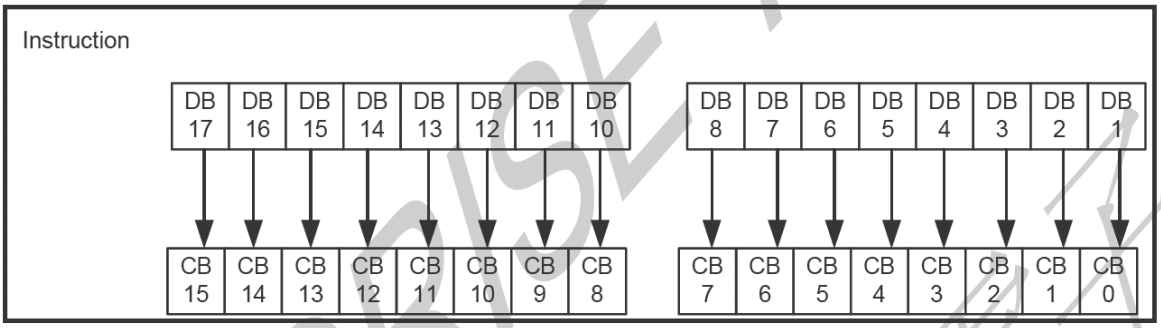


Figure 7-3

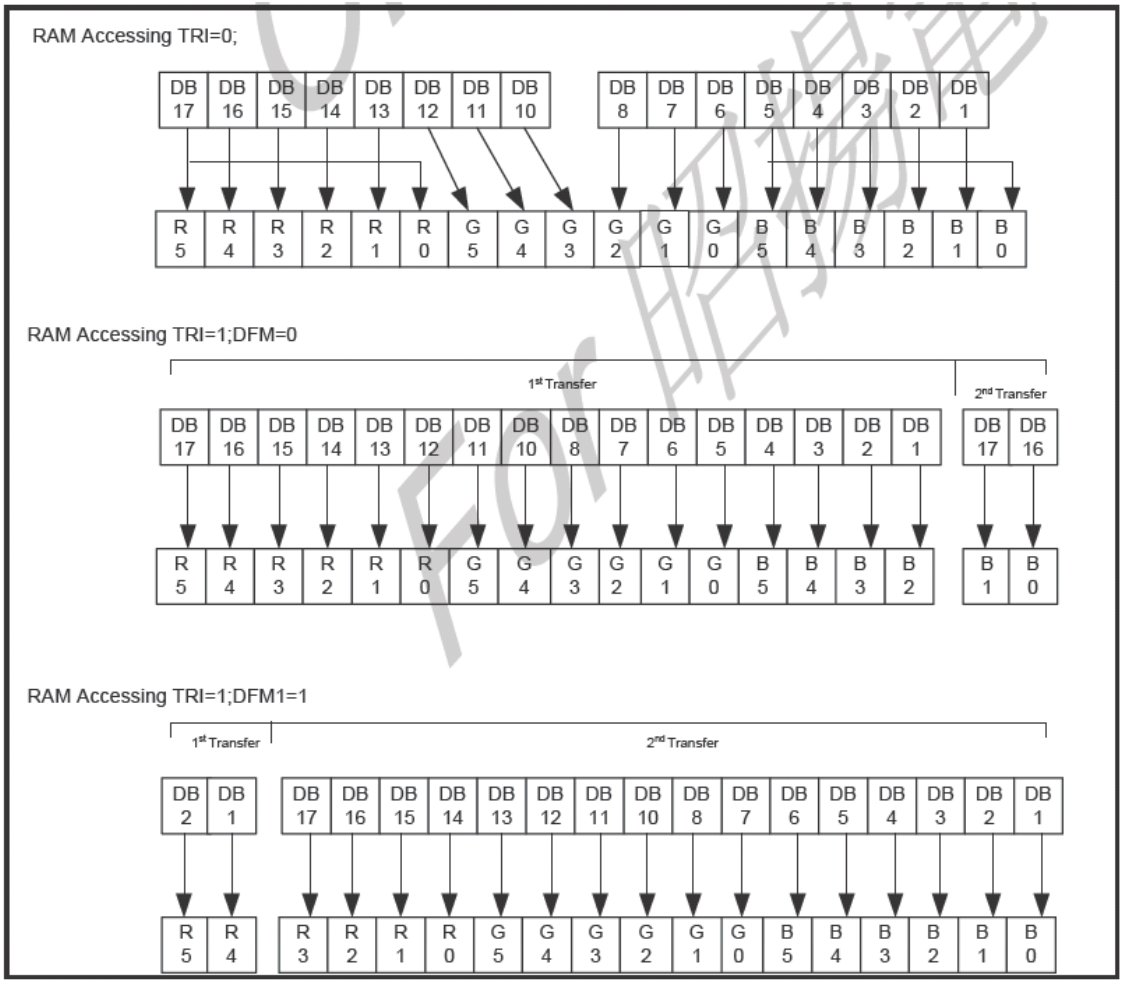


Figure 7-4

7-3 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in Figure 7-5 and Figure 7-6, respectively.

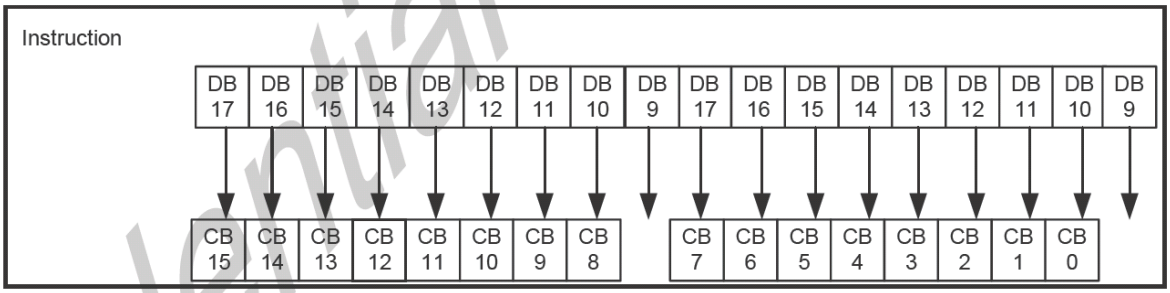


Figure 7-5

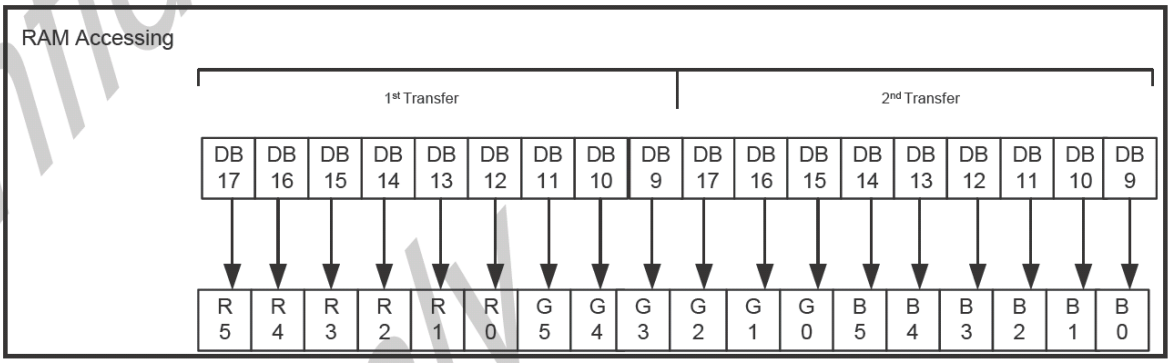


Figure 7-6

7-4 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in Figure 7-7 and Figure 7-8, respectively.

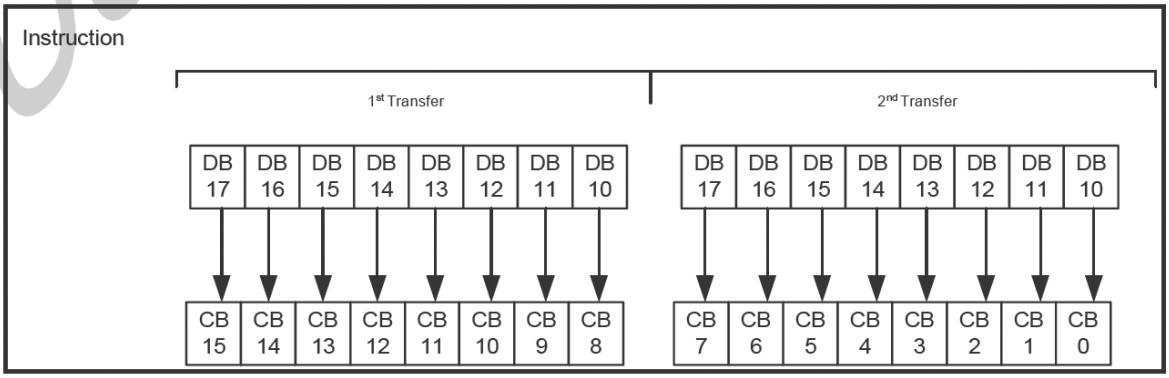


Figure 7-7

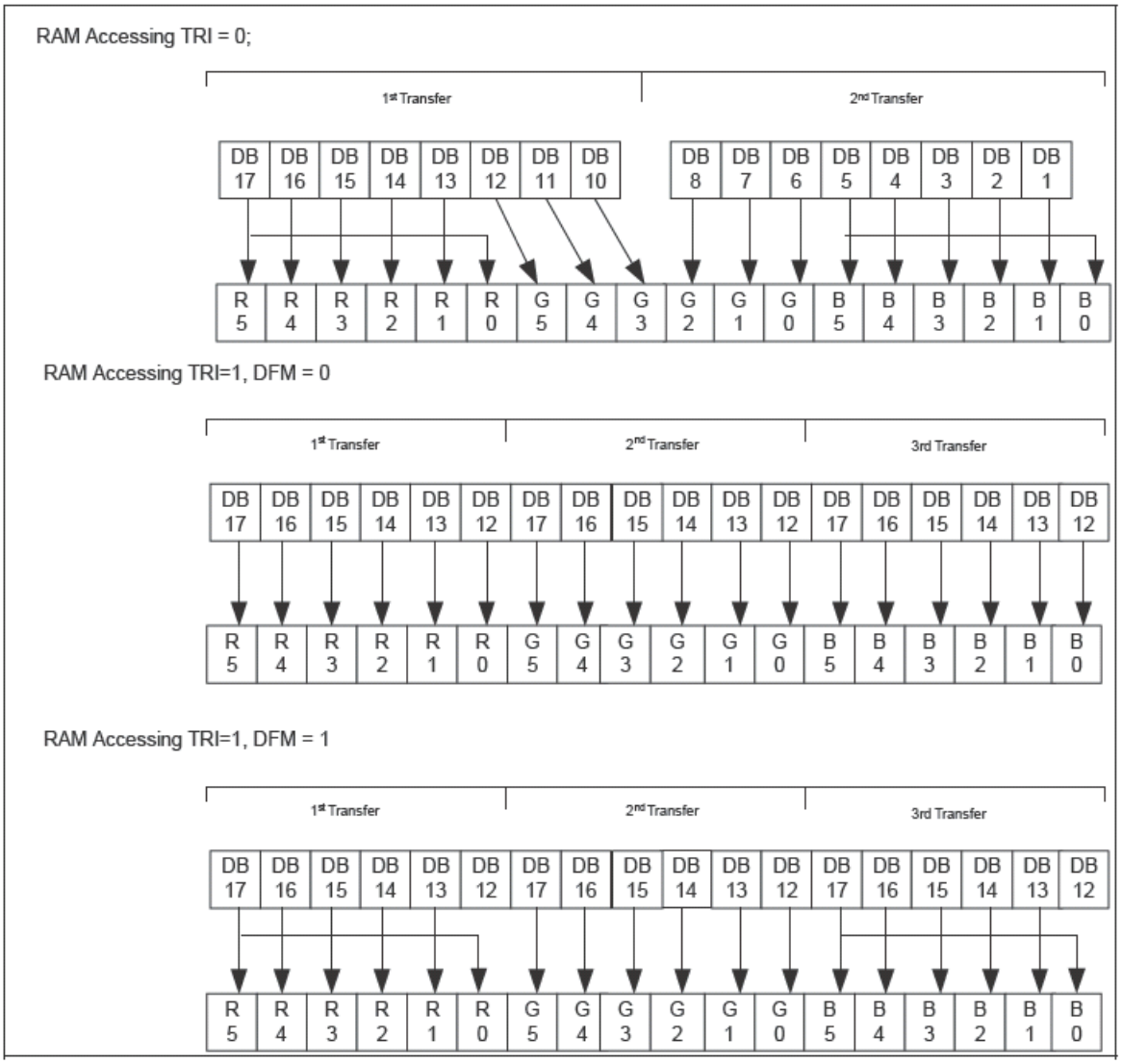


Figure 7-8

7-5 Serial Peripheral interface (SPI)

The system interface of SPFD5408B also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and SPFD5408B. IM0/ID pin served as the ID pin. Figure 7-9 illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

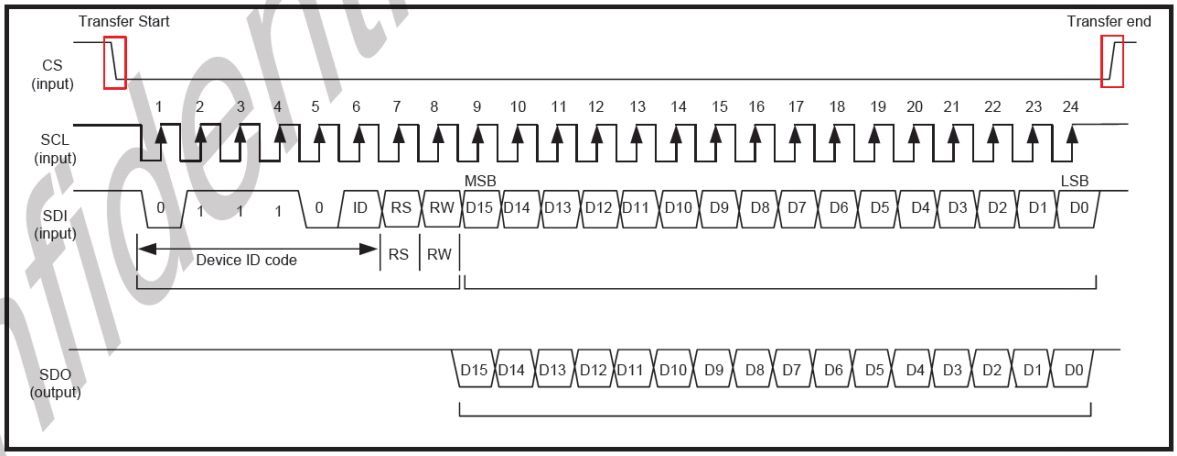


Figure 7-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

The instruction and GRAM accessing format o Serial Peripheral interface are shown in Figure 7-10 and Figure 7-11 respectively.

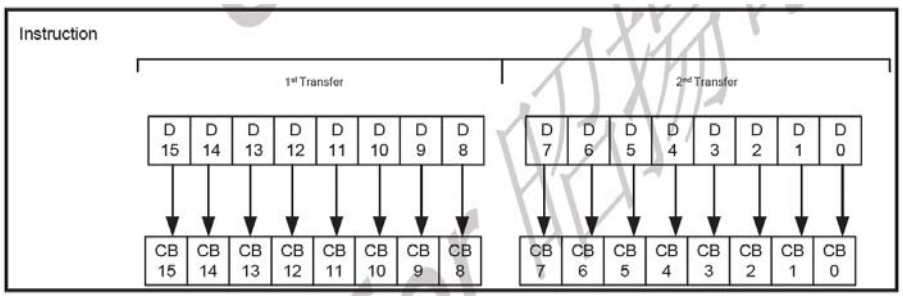


Figure 7-10

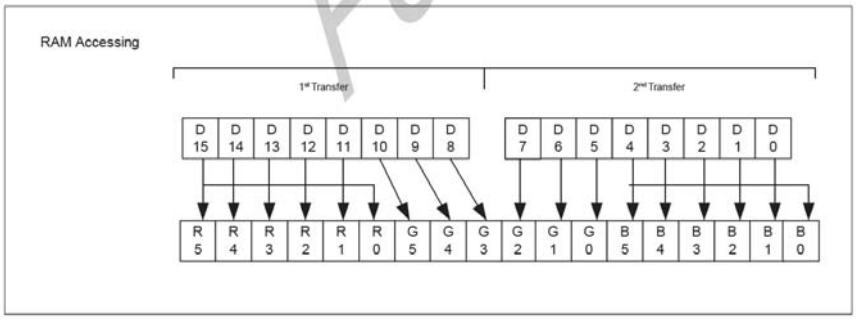


Figure 7-11

When read operation is desired In SPI mode, valid data are read out as the SPFD5408B reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with status read are illustrated in Figure 7-12,, respectively.

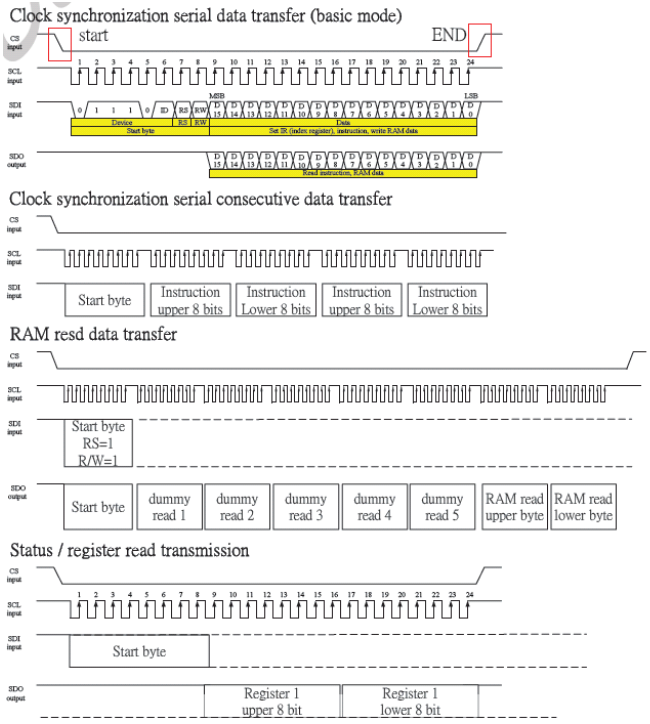


Figure 7-12

7-6 RGB Interface

AM-240320LDTNQW-00H also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. Table 7-1summarized the corresponding types of RGB interface with RIM1-0 setting.

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-10, 8-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

Table 7-1

RGB interface cab access SPFD5408B by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. Figure 7-13 illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

(a) Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface.

(b) In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.

(c) The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.

(d) In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

(e) In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

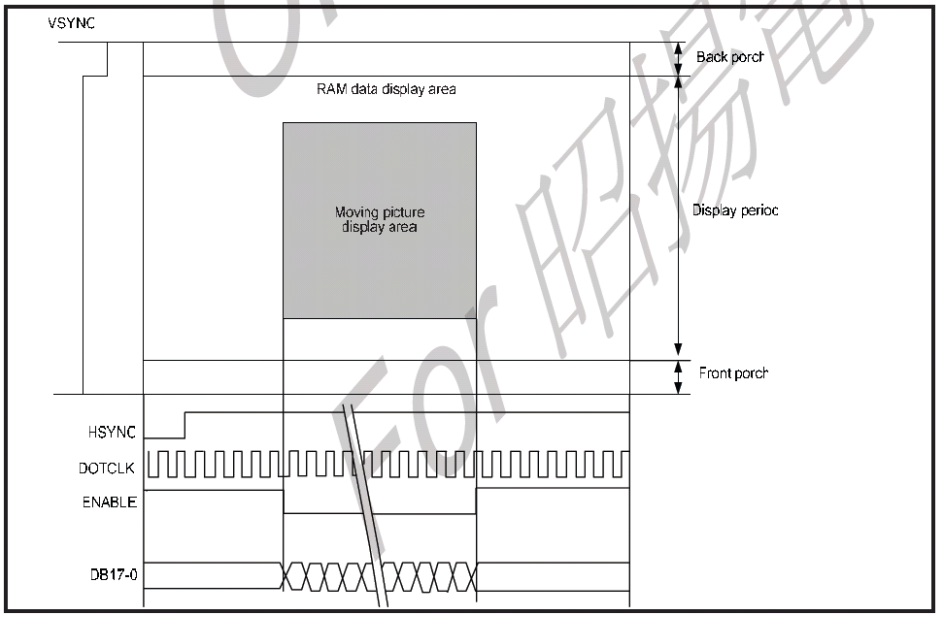


Figure 7-13

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. Table 7-2 summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disenabled	Retained
1	0	Disenabled	Retained
1	1	Enabled	Updated

Table 7-2

SPFD5408B can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in Figure7-14 and Figure 7-15respectively.

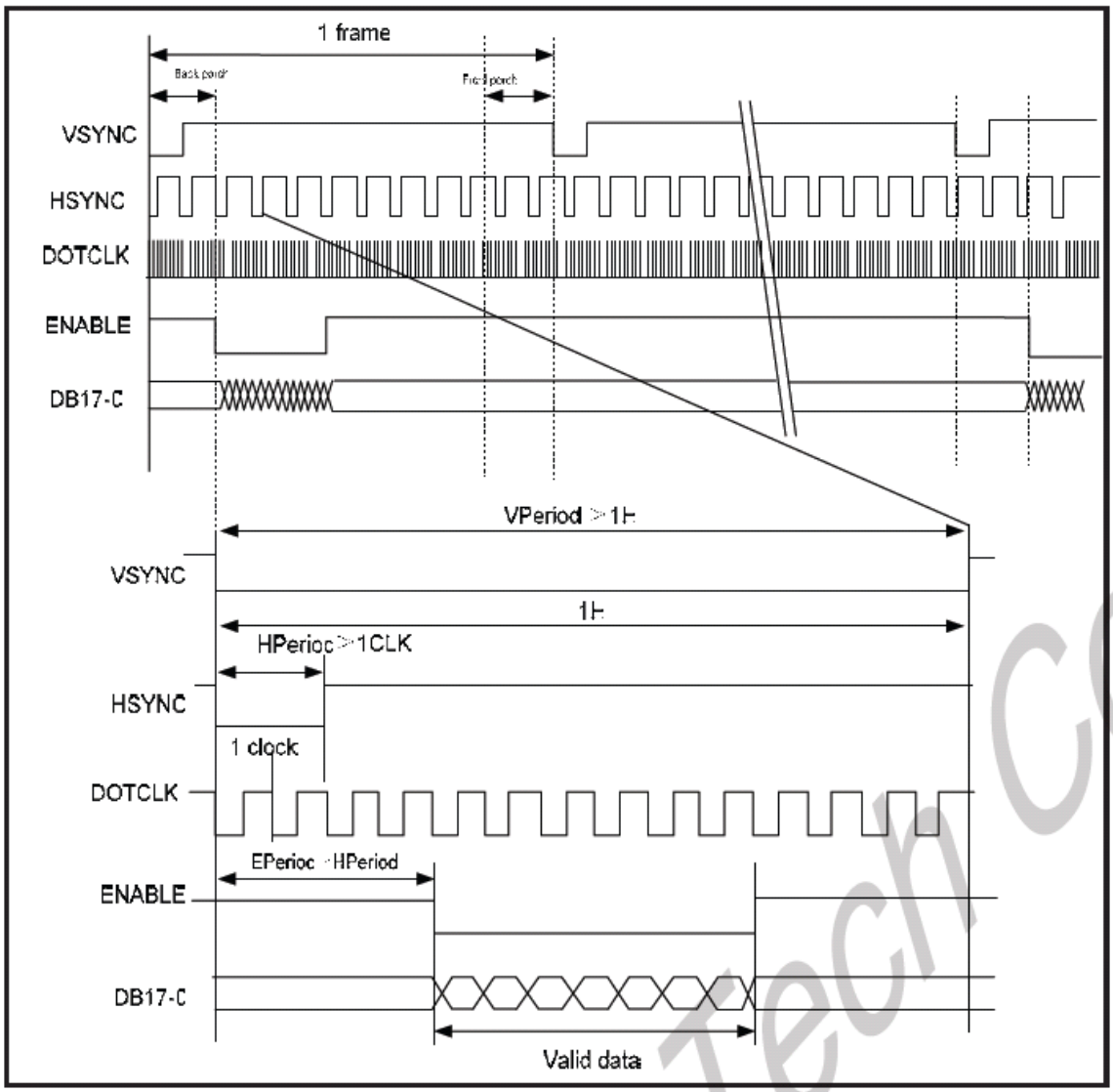


Figure 7-14

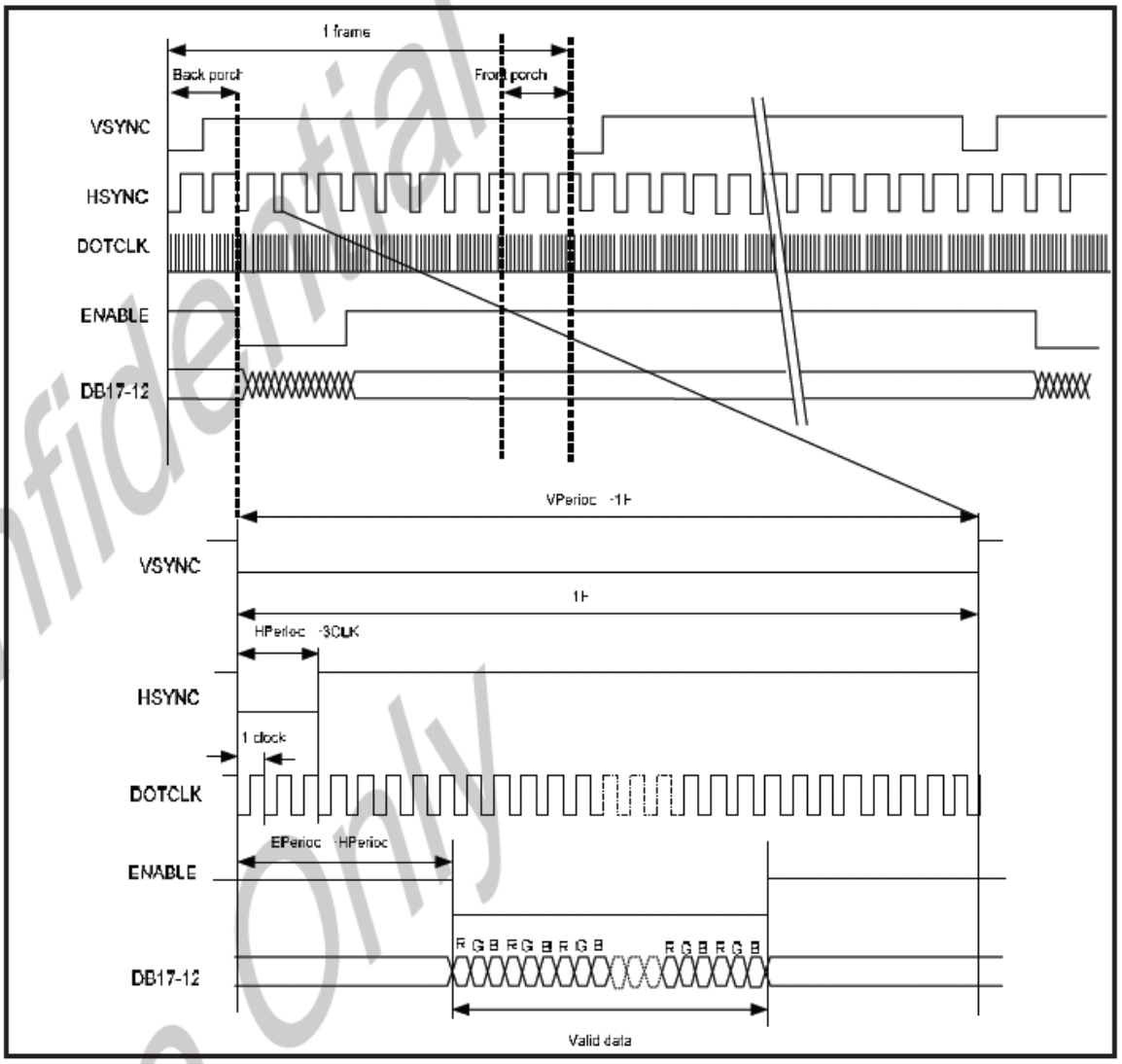

1 frame
Back porch
Front porch
VSYNC
HSYNC
DOTCLK
ENABLE
DB17-12
VPeriod -1H
VSYNC
1H
HPeriod -3CLK
HSYNC
1 clock
DOTCLK
EPeriod HPeriod
ENABLE
R G B R G B R G B
R G B R G B
DB17-12
Valid data

Figure 7-15

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM access through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting. Figure 7-16 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

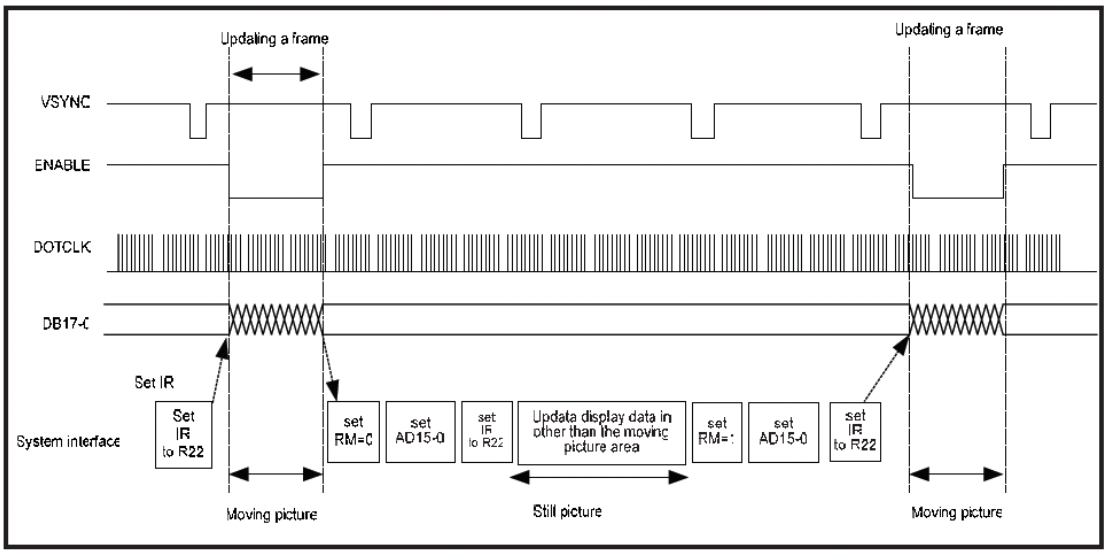


Figure 7-16

* 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in Figure 7-17 and Figure 7-18, respectively.

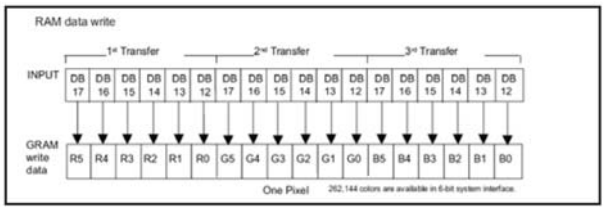


Figure 7-176

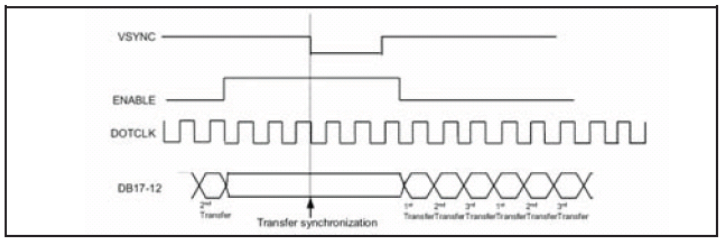


Figure 7-18

* 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in Figure 7-19.

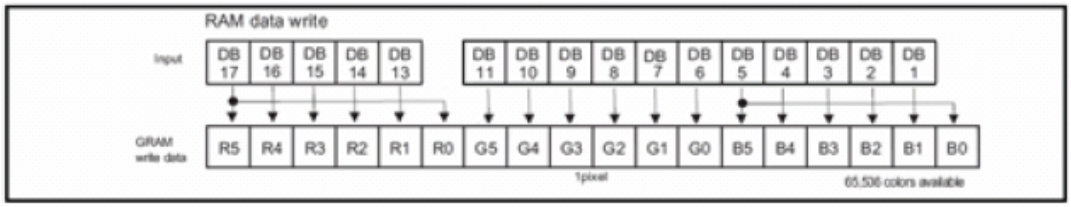


Figure 7-19

* 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in Figure 8-21.

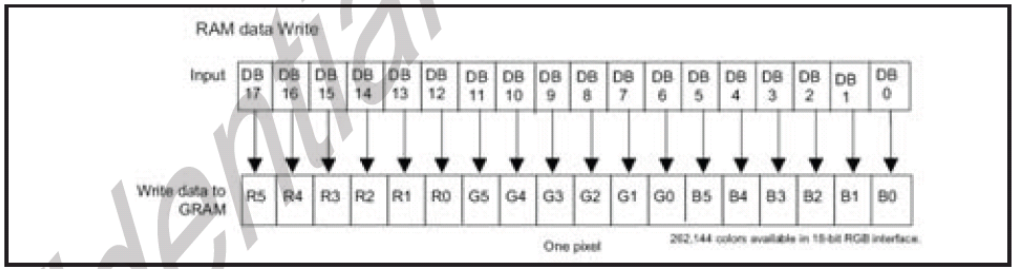


Figure 7-20

7-7 Instruction List

Main LCD Driver IC:SPFD5408B

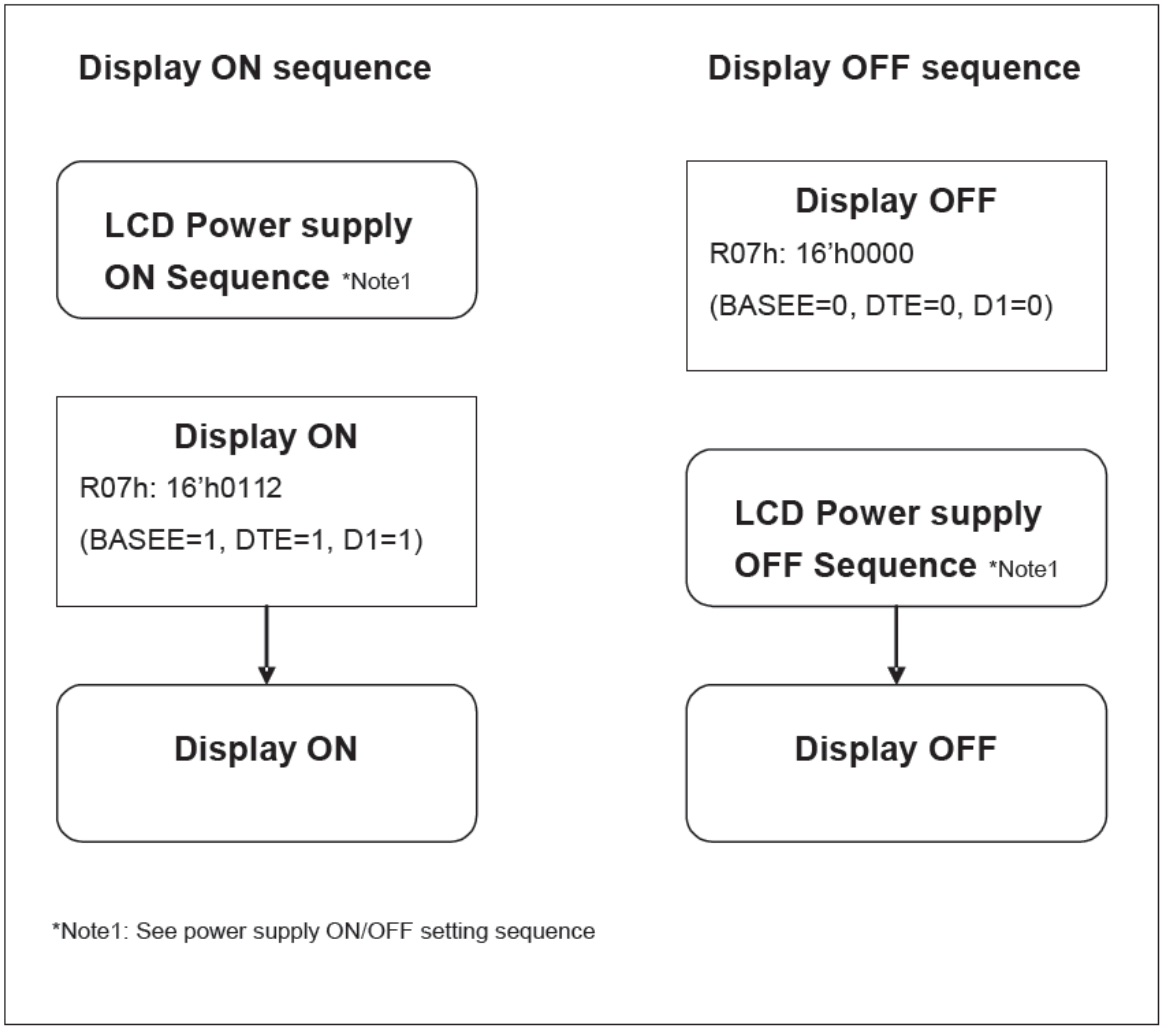
Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
00h	ID Read	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
02h	LCD Drive Waveform Control	0	0	0	0	0	1	B/C (0)	0	0	0	0	0	0	0	0	0
03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	0
04h	Scaling Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)
07h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	0	DTE (0)	COL (0)	0	D1 (0)	0
08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
09h	Display Control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
0Ah	Frame Cycle Control	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)
0Ch	External Display interface control (1)	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
0Fh	External Display interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
10h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
12h	Power Control (3)	0	0	0	0	0	0	0	VCMR0 (0)	VREG1R (0)	0	0	0	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
22h	Write Data to GRAM Read Data from GRAM																
28h	NVM read data (1)	0	0	0	0	0							0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
29h	NVM read data (2)	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
2Ah	NVM read data (3)	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
30h	γ Control (1)	0	0	0	V1RP4	V1RP3	V1RP2	V1RP1	V1RP0	0	0	0	V6RN4	V6RN3	V6RN2	V6RN1	V6RN0
31h	γ Control (2)	0	0	V2RP5	V2RP4	V2RP3	V2RP2	V2RP1	V2RP0	0	0	V5RN5	V5RN4	V5RN3	V5RN2	V5RN1	V5RN0
32h	γ Control (3)	0	0	V3RP5	V3RP4	V3RP3	V3RP2	V3RP1	V3RP0	0	0	V4RN5	V4RN4	V4RN3	V4RN2	V4RN1	V4RN0
33h	γ Control (4)	0	0	V4RP5	V4RP4	V4RP3	V4RP2	V4RP1	V4RP0	0	0	V3RN5	V3RN4	V3RN3	V3RN2	V3RN1	V3RN0
34h	γ Control (5)	0	0	V5RP5	V5RP4	V5RP3	V5RP2	V5RP1	V5RP0	0	0	V2RN5	V2RN4	V2RN3	V2RN2	V2RN1	V2RN0
35h	γ Control (6)	0	0	0	V6RP4	V6RP3	V6RP2	V6RP1	V6RP0	0	0	0	V1RN4	V1RN3	V1RN2	V1RN1	V1RN0
36h	γ Control (7)	0	0	0	V7RP4	V7RP3	V7RP2	V7RP1	V7RP0	0	0	0	V8RN4	V8RN3	V8RN2	V8RN1	V8RN0
37h	γ Control (8)	0	0	0	V8RP4	V8RP3	V8RP2	V8RP1	V8RP0	0	0	0	V7RN4	V7RN3	V7RN2	V7RN1	V7RN0
38h	γ Control (9)	0	0	0	0	V9RP3	V9RP2	V9RP1	V9RP0	0	0	0	0	V16RN3	V16RN2	V16RN1	V16RN0
39h	γ Control (10)	0	0	0	0	V10RP3	V10RP2	V10RP1	V10RP0	0	0	0	0	V15RN3	V15RN2	V15RN1	V15RN0
3Ah	γ Control (11)	0	0	0	0	V11RP3	V11RP2	V11RP1	V11RP0	0	0	0	0	V14RN3	V14RN2	V14RN1	V14RN0
3Bh	γ Control (12)	0	0	0	0	V12RP3	V12RP2	V12RP1	V12RP0	0	0	0	0	V13RN3	V13RN2	V13RN1	V13RN0
3Ch	γ Control (13)	0	0	0	0	V13RP3	V13RP2	V13RP1	V13RP0	0	0	0	0	V12RN3	V12RN2	V12RN1	V12RN0
3Dh	γ Control (14)	0	0	0	0	V14RP3	V14RP2	V14RP1	V14RP0	0	0	0	0	V11RN3	V11RN2	V11RN1	V11RN0
3Eh	γ Control (15)	0	0	0	0	V15RP3	V15RP2	V15RP1	V15RP0	0	0	0	0	V10RN3	V10RN2	V10RN1	V10RN0
3Fh	γ Control (16)	0	0	0	0	V16RP3	V16RP2	V16RP1	V16RP0	0	0	0	0	V9RN3	V9RN2	V9RN1	V9RN0
50h	Window Horizontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
51h	Window Horizontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
52h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
53h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
60h	Driver Output Control	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)

61h	Driver Output Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scroll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
80h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
81h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
82h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
83h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)
84h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
85h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
92h	Panel Interface Control 2	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	0	0	0
93h	Panel Interface Control 3	0	0	0	0	0	0	VEQW11 (0)	VEQW10 (0)	0	0	0	0	0	MCPI2 (0)	MCPI1 (0)	MCPI0 (0)
95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
97h	Panel Interface Control 5	0	0	0	0	NOWE3 (0)	NOWE2 (0)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	0	0	0	0
98h	Panel Interface Control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE2 (0)	MCPE1 (0)	MCPE0 (0)
A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB (0)

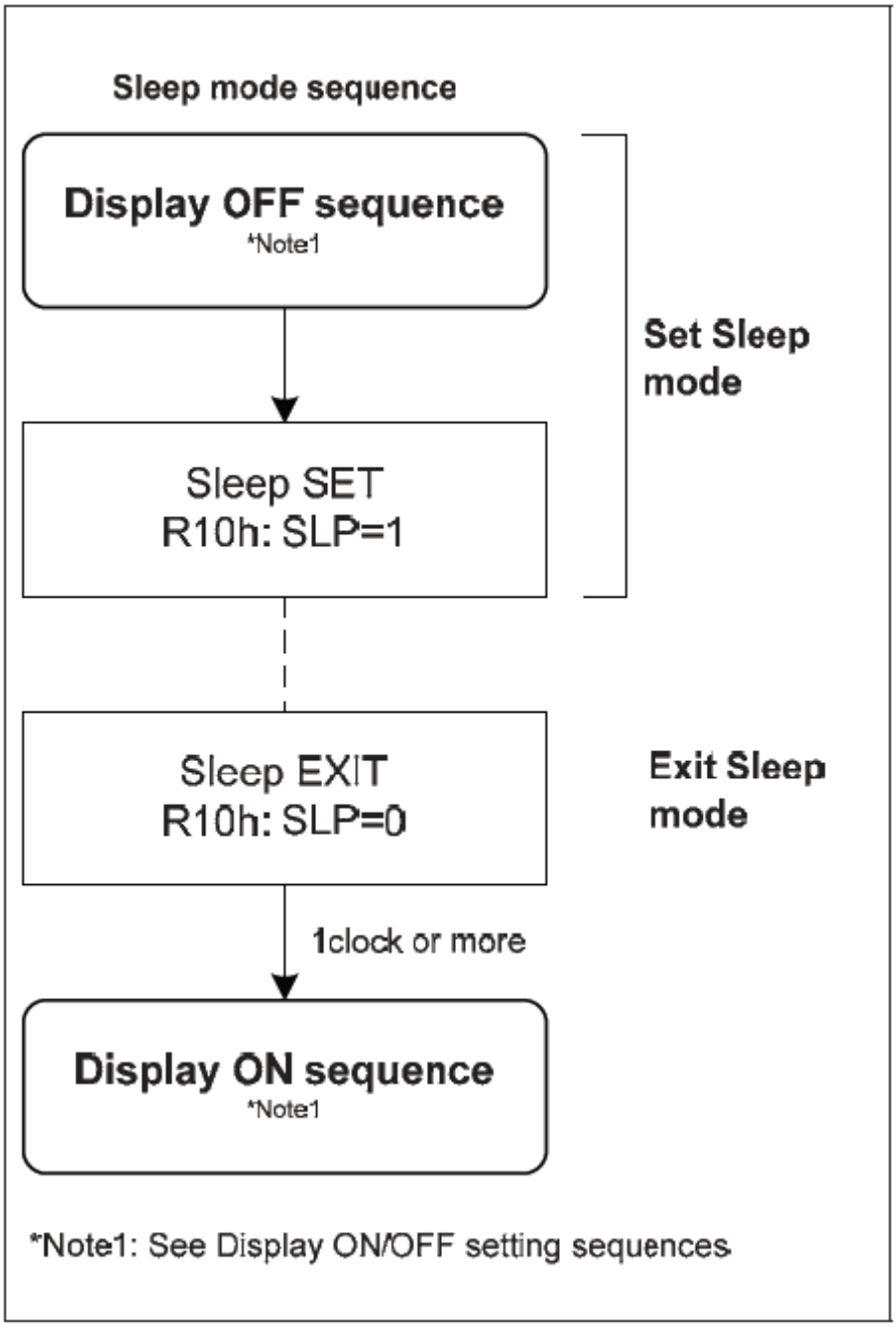
~

8 Application

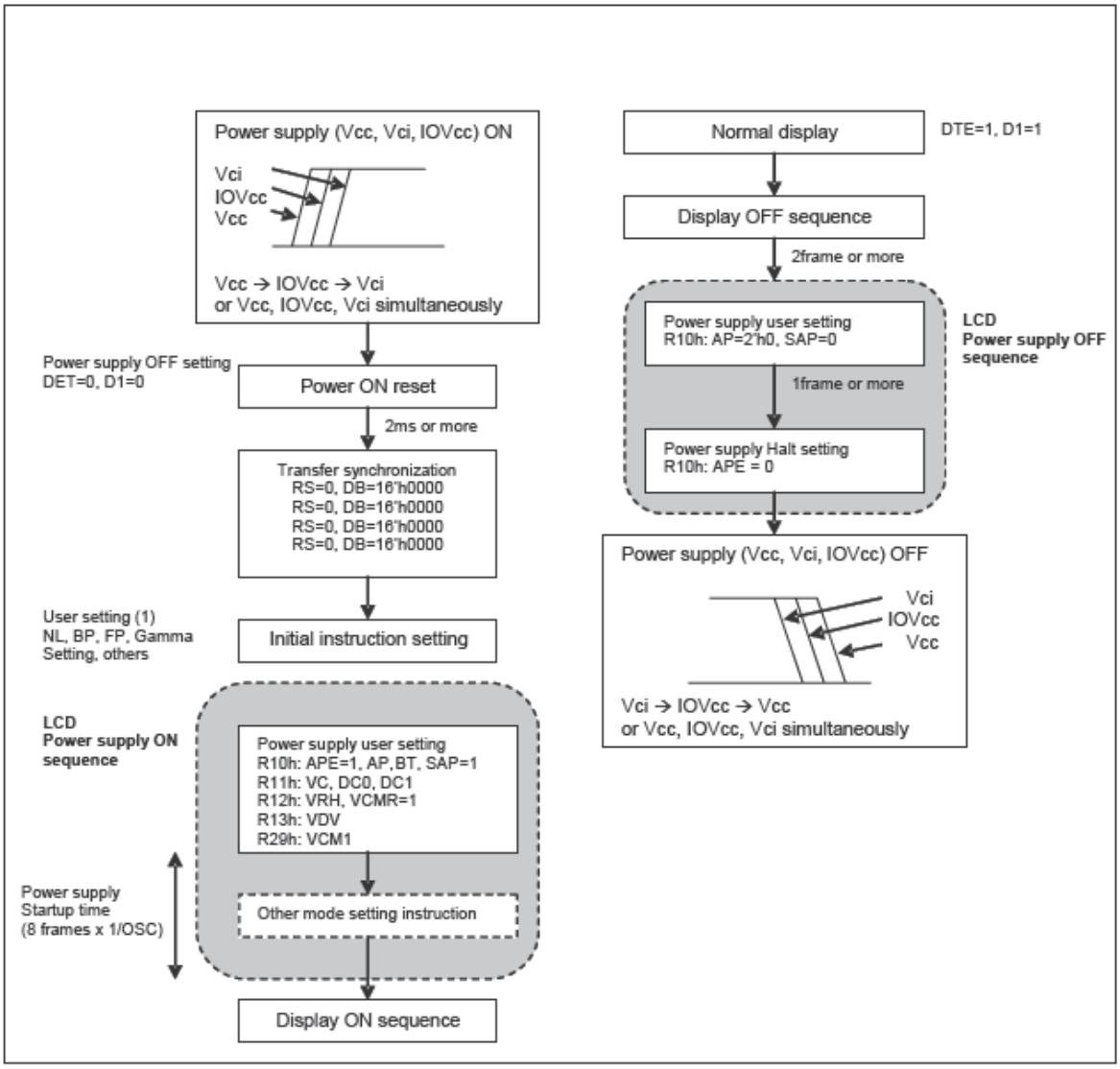
8-1 Display ON / OFF



8-2 Sequence to exit sleep mode



8-3 Power Supply Configuration



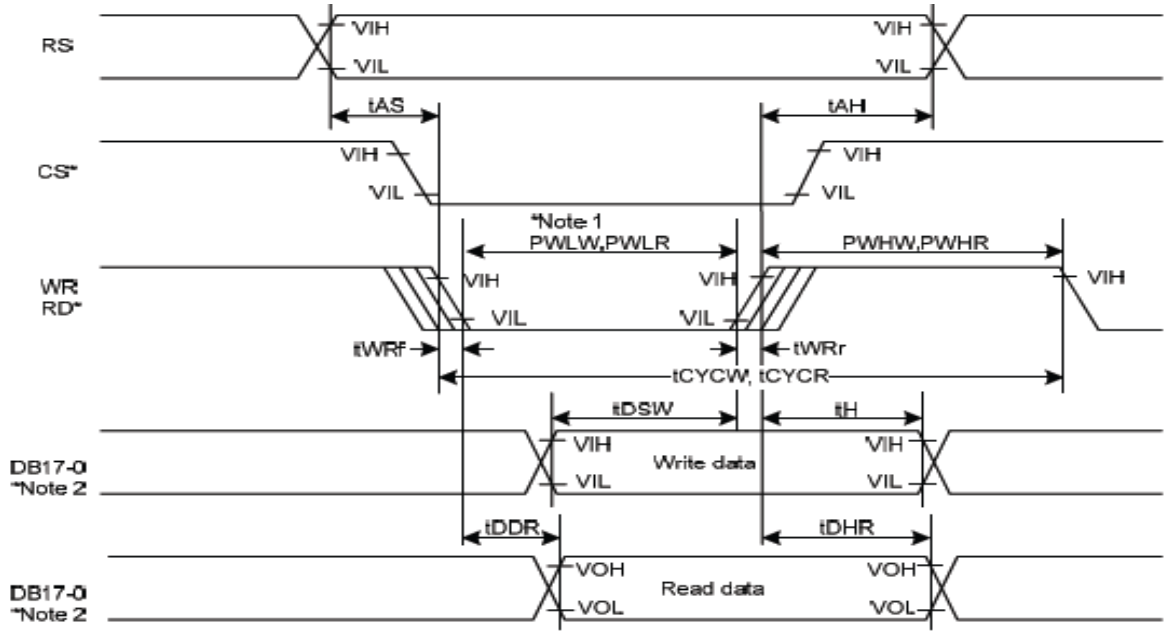
Power Supply ON/OFF Sequence

9 Electrical Characteristics

9-1 AC Characteristics (i80 – system Interface Timing Characteristics)

Normal write operation, IOVCC=1.65V~3.30V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	125	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	45	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	25
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-



***Note1: PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".**

***Note2: Unused DB pins must be fixed at "IOVcc 1" "IOGND 1".**

Figure 9-1 80-System Bus Interface

Figure 9-2 Reset Operation

10 QUALITY AND RELIABILITY

10-1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10-2 SAMPLING PLAN

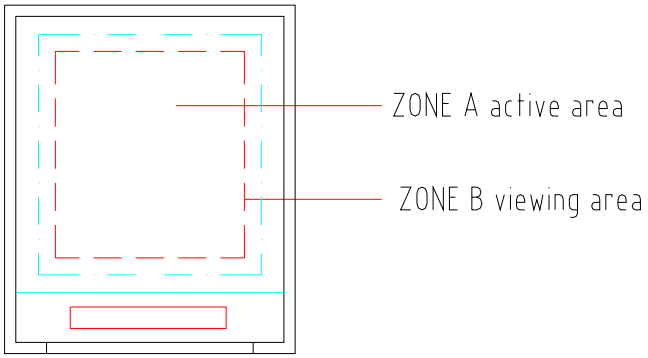
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10-3 ACCEPTABLE QUALITY LEVEL

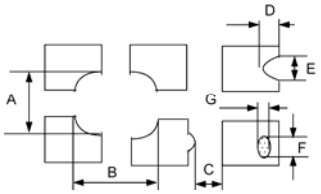
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10-4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



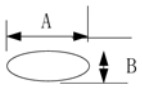
10-5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defec</th><th>Acceptable level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>2</td><td>Scratch,Dent of Plastic Mold</td><td>Serious one is not allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>3</td><td>Scratch on FPC</td><td>By limited sample</td><td>Major</td><td>0.65</td></tr>
<tr><td>4</td><td>Dot Defect</td><td><table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>N ≦ 0</td></tr><tr><td>Black dot defect</td><td>N ≦ 2</td></tr><tr><td>Total</td><td>N ≦ 2</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>5</td><td>Line Defect</td><td>None</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Uneven Brightness : Line Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>7</td><td>Uneven Brightness : Dot Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>8</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Scratch of Polarizer :Dot Shape s
Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1
0.1 < D ≤ 0.3
0.3 < D</td><td>Ignore
3
0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr>
<td>10</td>
<td>Scratch of Polarizer :

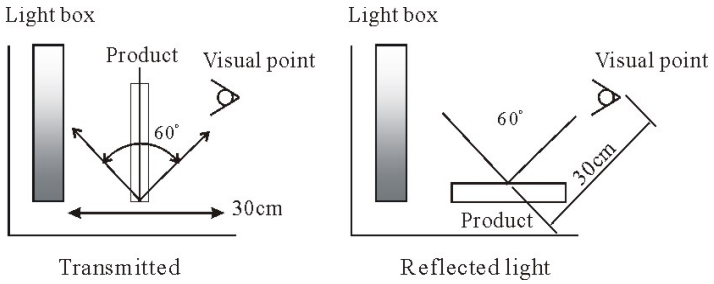
Line Shape

  </td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.05</td><td>L ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.1<W≤0.05</td><td>0.3 < L ≤ 2.0</td><td>N≦3.</td></tr>
<tr><td>0.1<W</td><td>-</td><td>See dot shape</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>11</td>
<td>Bubble in polarizer</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.30 < D ≤ 0.50</td><td>1</td></tr>
<tr><td>0.50 < D</td><td>0</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>12</td>
<td>Stains inclusion : Line shape</td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.04</td><td>Ignore</td><td>Not Allowed</td></tr>
<tr><td>0.04<W≤0.06</td><td>L ≤ 0.8</td><td>Not Allowed</td></tr>
<tr><td>0.06<W</td><td>-</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>13</td>
<td>Stains inclusion : dot shape</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Not Allowed</td></tr>
<tr><td>0.1 < D ≤ 0.2</td><td>Not Allowed</td></tr>
<tr><td>0.25< D</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>14</td>
<td>Newton Ring</td>
<td>(A). The lightness of environment is 500 Lux

(B). The distance between product and eye is about 30cm

(C). The angle of 60° between eye

(D). Please find data below for your reference

Not Allowed Newton Ring</td>
<td>Major</td>
<td>0.65</td>
</tr>
</table>

10-6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=72 hrs	
Low Temperature Operation	-10±3°C , t=72 hrs	
High Temperature Storage	80±3°C , t=72hrs	1,2
Low Temperature Storage	-30±3°C , t=72 hrs	1,2
Temperature /Humidity Storage Test	60°C, Humidity 90%, 72 hrs	1,2
Temperature /Humidity Operation Test	40°C, Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-20°C ~ 70°C 60 min 60 min. (1 cycle) Total 20 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2
Static Electricity	150pF 330 ohm ±8kV, 10times air discharge ±5kV, 10times contact discharge	

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11-1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11-2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11-3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11-4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11-5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one years warrantee for all products and three months warrantee for all repairing products.

12 MECHANICAL DRAWING