A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

2.8-IN WVGA COLOR TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	AM-240400ATNQW-T00H W/ TOUCH
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2007/12/18	-	New Release	Edward
2008/2/1	--	Rename to AM-240400ATNQW-T00H	Edward
	--	Modify the arrangement of Chapter	Edward
	3	Modify Features	Edward
		(From 18bit-80 change to 8bit-80 of default setting)	
	--	Revise all T.B.D value	Edward
	7	Modify the brightness of LCM to 230 cd/m2(typ)	Edward
	10	Modify Block Diagram	Edward

1 Features

LCD 2.81 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments. The LCD adopts one backlight with High brightness 5-lamps white LED.

(1) Construction: 2.81” a-Si color TFT-LCD with White LED Backlight, and FPC.
(2) LCD : 2.1 Amorphous-TFT 2.81” inch display, transmissive, Normally white type, 12 o’clock.
2.2 240(RGB)X400 dots Matrix,1/400 Duty.
2.3 LCD controller is SPFD5420A.
2.4 Real 262K colors display:
262K: Red-6bit, Green-6bit, Blue-6bit (9/18-bit interface)
Dithering 262K: Red-5bit, Green-6bit, Blue-5bit (8/16-bit interface)
(3) Direct data display with display RAM.
Built-in 233,280 bytes internal RAM.
(4) MPU interface: 8/9/16/18-bit 80 system parallel interface selectable.
<Default>8-bit 80 system interface.
(5) VSYNC interface mode : for moving picture display

2 Mechanical specifications

Dimensions and weight

Item		Specifications	Unit
External shape dimensions		*1 43.22 (W) x 74.8 (H)	mm
Main LCD	Pixel size	0.153 (W) x 0.153 (H)	mm
	Active area	36.72 (W) x 61.2 (H)	mm
	Number of Pixels	240(H)x400(V) pixels	mm
Weight		23	g

*1. This specification is about External shape on shipment from AMPIRE.

3 Absolute max. ratings and environment

3-1 Absolute max. ratings

Ta=25°C GND=0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power voltage	VDD – GND	-0.3	+4.0	V	
Power voltage	LED A – LED K	-0.5	+4.0	V	Parallel
Input voltage	VIN	-0.3	VDD	V	

3-2 Environment

Item	Specifications	Remarks
Storage temperature	Max. +80°C Min. -30°C	Note 1: Non-condensing
Operating temperature	Max. +70°C Min. -20°C	Note 1: Non-condensing

Note 1：Ta≦+40°C・・・・Max.85%RH

Ta＞+40°C・・・・The max. humidity should not exceed the humidity with 40°C 85%RH.

4 Electrical specifications

4-1 Electrical characteristics of LCM

(V_{DD}=3.0V, Ta=25°C)

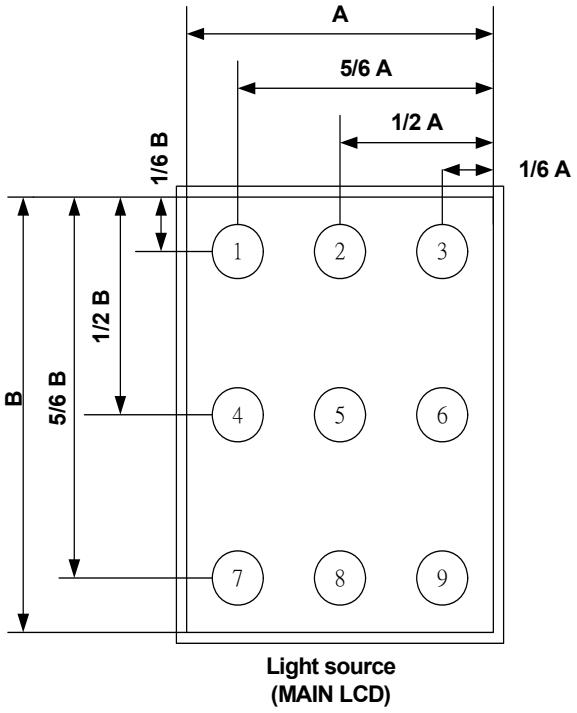
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage	V_{DD}		2.5	2.8	3.6	V
High-level input voltage	V_{IHC}		$0.8V_{DD}$		V_{DD}	V
Low-level input voltage	V_{ILC}		0		$0.2V_{DD}$	V
Consumption current of VDD	I_{DD}	LED OFF	-	6.6	-	mA
Consumption current of LED	I_{LED}	V_{LED}=3.3V	-	100	-	mA

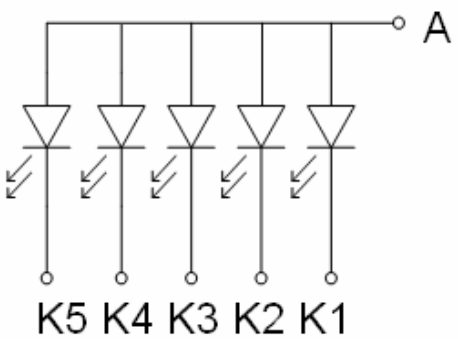
※ 1. 1/400 duty.

4-2 LED back light specification

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f =100mA	3.1	3.3	3.7	V
Reverse voltage	V_r		-	-	(12)	V
Forward current	I_f	5-chip Parallel		100	105	mA
Power Consumption	P_{BL}	I_f =100mA	-	(330)	-	mW
Uniformity (with L/G)	-	I_f=100mA	80%*1	-	-	
Bare LED Luminous intensity	V_f I_f	3.3V 100mA	5000	-	-	cd/m^2
Luminous color	White					
Chip connection	5 chip parallel connection					

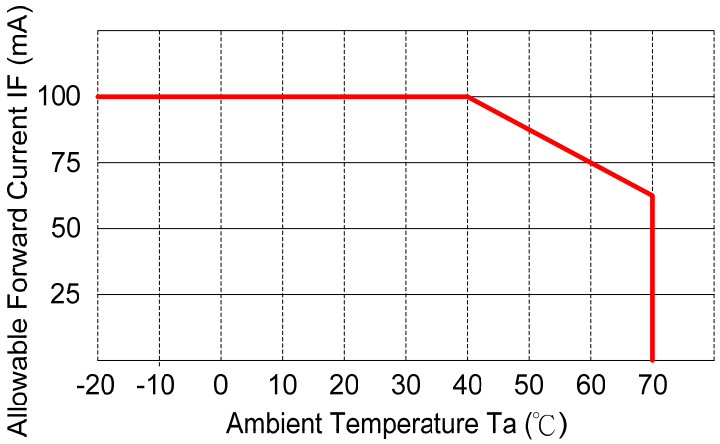
Bare LED measure position:





*1 Uniformity (LT): $\frac{Min(P1 \sim P9)}{Max(P1 \sim P9)} \times 100 \geq 80\%$

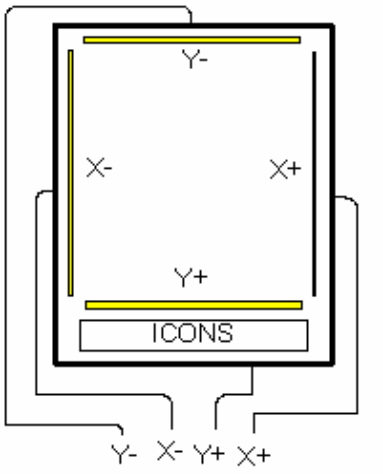
When LCM is operated over 40℃ ambient temperature, the ILED of the LED back-light should be follow :



4-3 Touch Panel Electrical Specification

Parameter	Condition	Standard Value
Terminal Resistance	X Axis	(200) ~ (900) Ω
	Y Axis	(200) ~ (900) Ω
Insulating Resistance	DC 25 V	More than (20)MΩ
Linearity	--	±1.5 %
Notes life by Pen	Note a	(100,000) times(min)
Input life by finger	Note b	(1,000,000) times (min)

	Symbol	Function
1	X+	Touch Panel Right Signal in X Axis
2	Y+	Touch Panel Bottom Signal in Y Axis
3	X-	Touch Panel Left Signal in X Axis
4	Y-	Touch Panel Top Signal in Y Axis



5 Optical characteristics

Main LCD

5.1 Optical characteristics

(1/400 Duty in case except as specified elsewhere Ta = 25°C)

LED backlight transmissive module:

Item	Symbol	Temp.	Min.	Std.	Max.	Unit	Conditions
Response time	Tr	25°C	--	12	--	ms	θ=0°, φ=0° (Note 2)
	Tf	25°C	--	18	--		
Contrast ratio	CR	25°C	250	400	-	-	θ=0°, φ=0° LED:ON, LIGHT:OFF (Note 4)
Transmittance	T	25°C	(5.0)	(5.4)	-	%	
Visual angle range front and rear	θ	25°C	(θf) (70) (θb) (50)			De-gree	φ= 0°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle range left and right	θ	25°C	(θl) (70) (θr) (70)			De-gree	φ=90°, CR≧10 LED:ON LIGHT:OFF (Note 3)
Visual angle direction priority			12:00				(Note 5)
Brightness			(200)	(230)	--	Cd/m2	V_{LED}=3.3V, 100mA Full White pattern

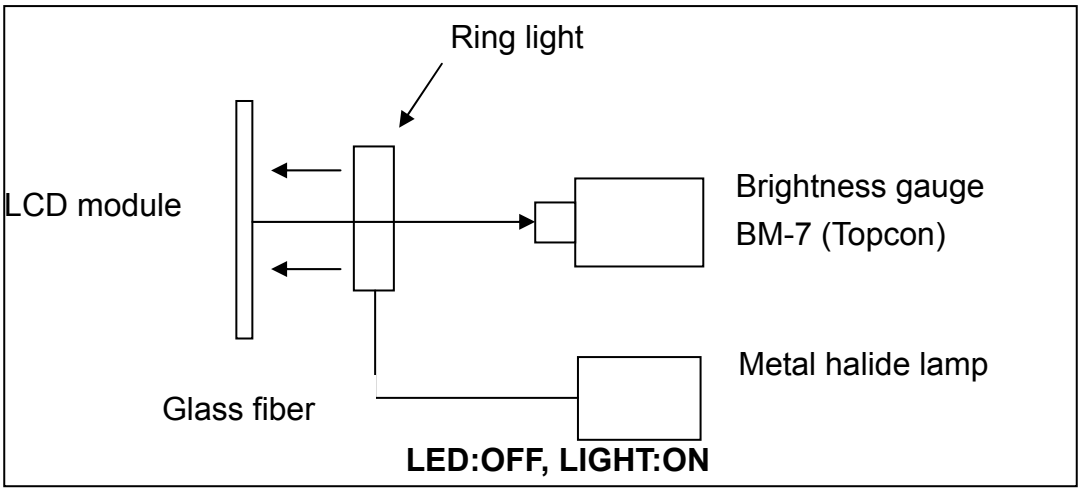
( ) is a default

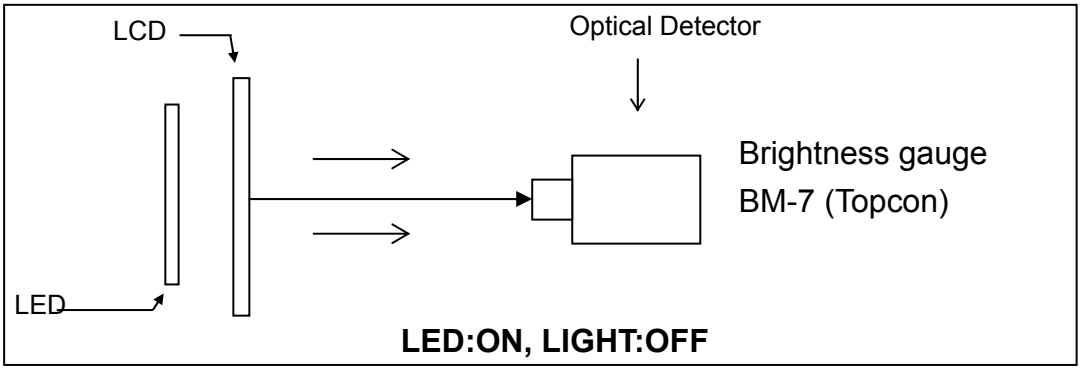
5.2 CIE (x, y) chromaticity (1/400 Duty Ta = 25°C)

Item	Symbol	Transmissive			Conditions
		Min.	Typ.	Max.	
Red	X	--	(0.623)	--	θ=0°, φ=0°
	Y	--	(0.332)	--	
Green	X	--	(0.2843)	--	θ=0°, φ=0°
	Y	--	(0.554)	--	
Blue	X	--	(0.149)	--	θ=0°, φ=0°
	Y	--	(0.128)	--	
White	X	--	(0.308)	--	θ=0°, φ=0°
	Y	--	(0.333)	--	

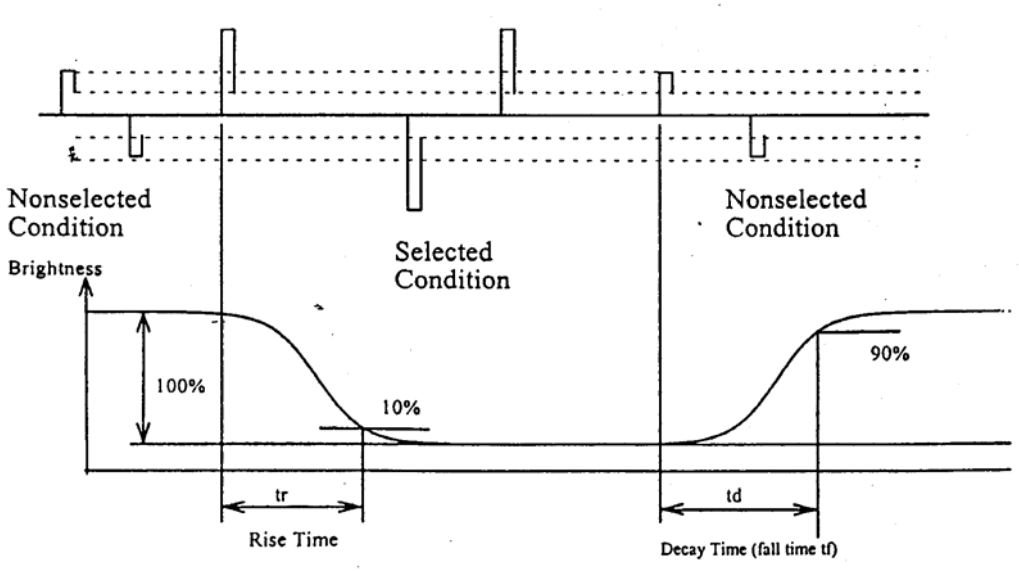
( ) is a default

NOTE 1: Optical characteristic measurement system

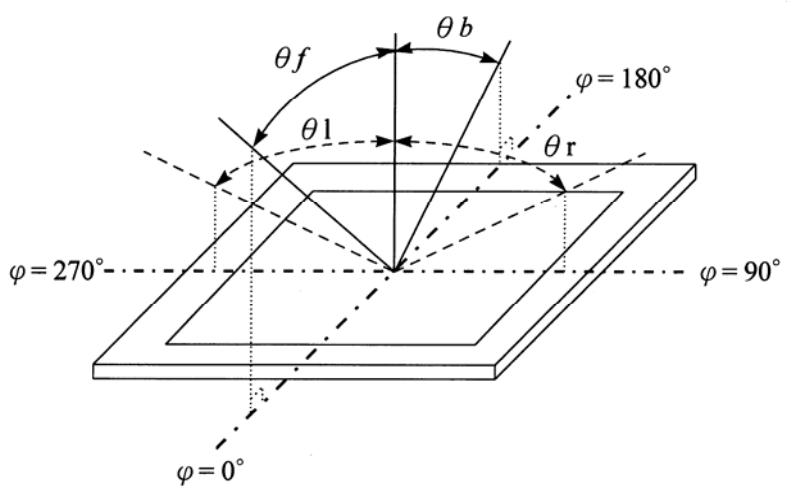




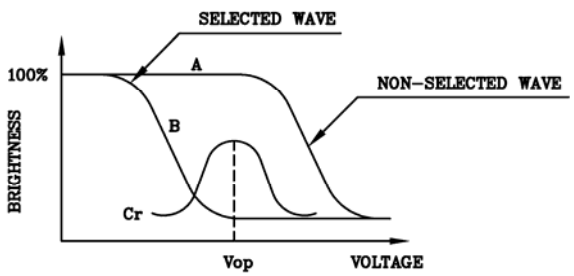
NOTE 2: Response tome definition



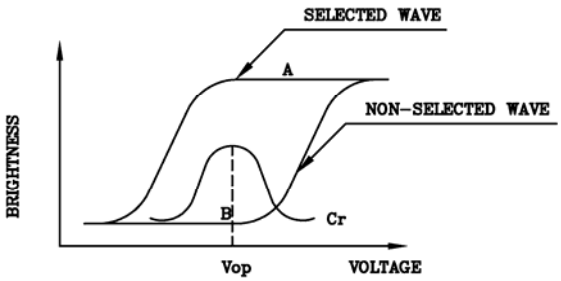
NOTE 3: φ、θ definition



NOTE 4: Contrast definition



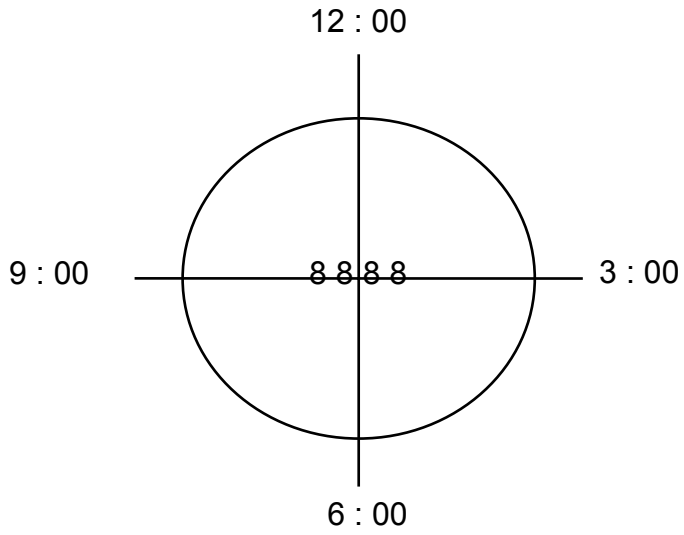
(positive type)



(negative type)

Contrast Ratio : Cr=A/B

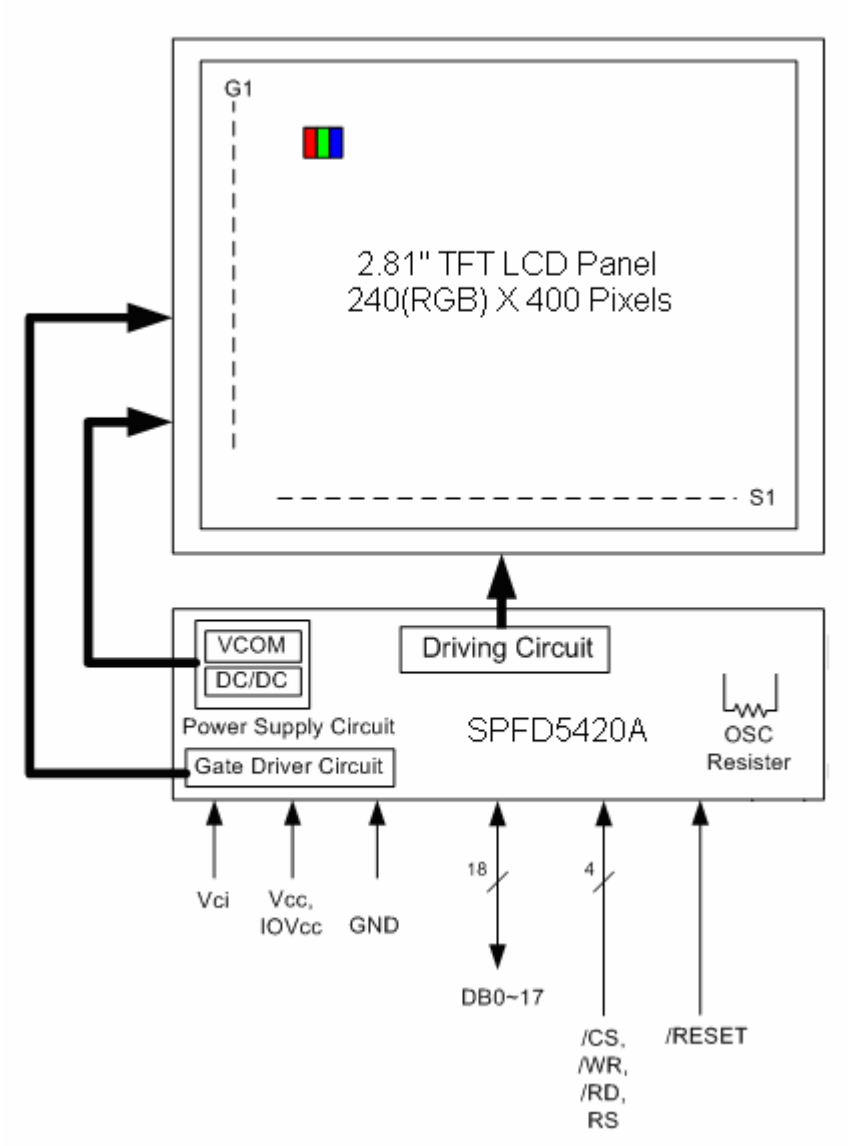
NOTE 5: Visual angle direction priority



6 Block Diagram

Block diagram (Main LCD)

Display format: A-Si TFT transmissive, Normally white type, 12 o'clock.
Display composition: 240 x RGB x 400 dots
LCD Driver : SPFD5420A
Back light: White LED x 5 (I_{LED}=100mA)



7 Interface specifications

Pin No.	Terminal	Functions
1	NC	No Connection
2	NC	No Connection
3	NC	No Connection
4	FLM	Frame head pulse signal, which is used when writing data to the internal RAM.
5	/RESET	Reset pin.
6	DB17	Data Bus Pin
7	DB16	Data Bus Pin
8	DB15	Data Bus Pin
9	DB14	Data Bus Pin
10	DB13	Data Bus Pin
11	DB12	Data Bus Pin
12	DB11	Data Bus Pin
13	DB10	Data Bus Pin
14	DB9	Data Bus Pin
15	DB8	Data Bus Pin
16	DB7	Data Bus Pin
17	DB6	Data Bus Pin
18	DB5	Data Bus Pin
19	DB4	Data Bus Pin
20	DB3	Data Bus Pin
21	DB2	Data Bus Pin
22	DB1	Data Bus Pin
23	DB0	Data Bus Pin
24	/RD	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low
25	/WR	In 80-system interface mode, a write strobe signal can be input via this pin
26	RS	Register select signal.
27	/CS	Chip select signal.
28	VSYNC	In external interface mode, served as a vertical synchronize signal input
29	IOVCC	Power supply to the interface pins
30	VCC	Internal logic power
31	VCI	Reference voltage of step-up circuit
32	GND	Internal logic GND
33	GND	Internal logic GND
34	XL	Touch panel X axis (Left)
35	YD	Touch panel Y axis (Bottom)
36	XR	Touch panel X axis (Right)

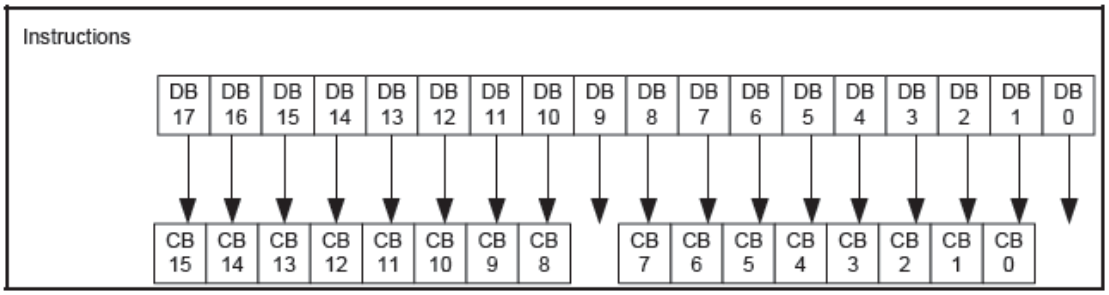
37	YU	Touch panel Y axis (Top)
38	NC	No Connection
39	LEDA	LED Backlight A terminal
40	LEDA	LED Backlight A terminal
41	LEDK1	LED Backlight K1 terminal
42	LEDK2	LED Backlight K2 terminal
43	LEDK3	LED Backlight K3 terminal
44	LEDK4	LED Backlight K4 terminal
45	LEDK5	LED Backlight K5 terminal

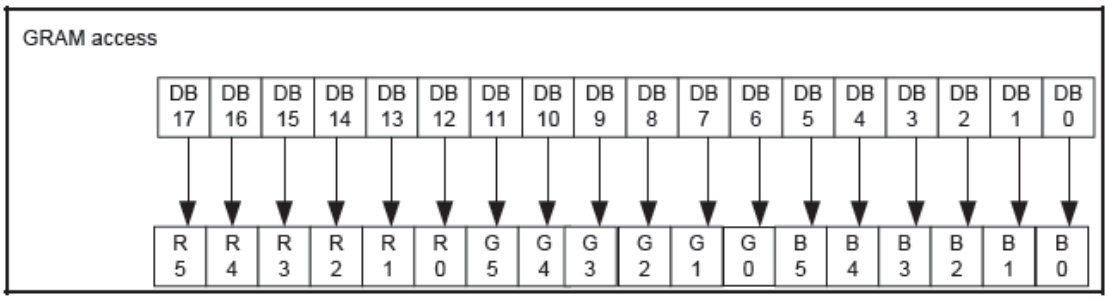
7.1 MPU interface

The system interfaces of SPFD5420A can support 8-bit, 9-bit,16-bit, 18-bit 80-system Interface. <Default>8-bit 80 system interface.

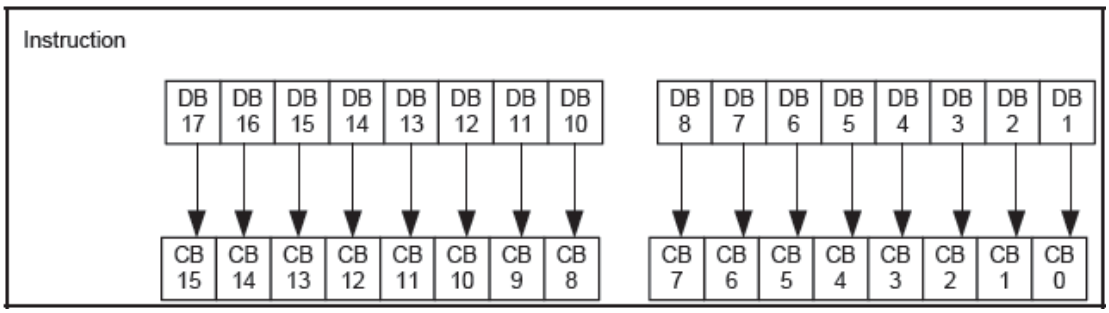
MPU-Interface Mode	DB Pin in use	JP1(IM0) 1:H 2:IM0 3:L	JP2 (IM1) 1:H 2:IM1 3:L	Remark
80-system 18-bit interface	DB17 to 0	1,2 Open 2,3 Short **L**	1,2 Open 2,3 Short **L**	
80-system 9-bit interface	DB17 to 9	1,2 Open 2,3 Short **L**	1,2 short 2,3 open **H**	
80-system 16-bit interface	DB17 to 10 and 8 to 1	1,2 short 2,3 open **H**	1,2 Open 2,3 Short **L**	
80-system 8-bit interface	DB17 to 10	1,2 short 2,3 open **H**	1,2 short 2,3 open **H**	**Default**

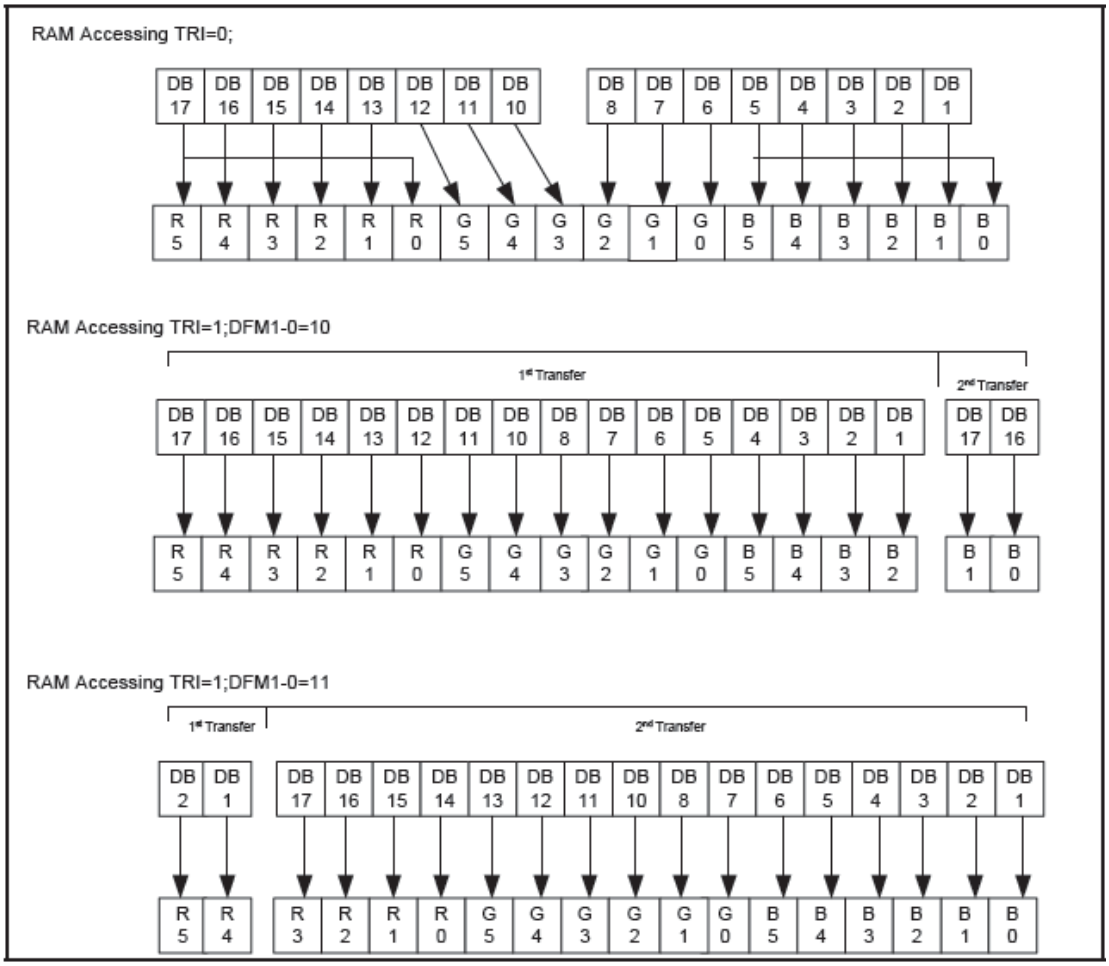
7.1.1 80-system 18-bit interface



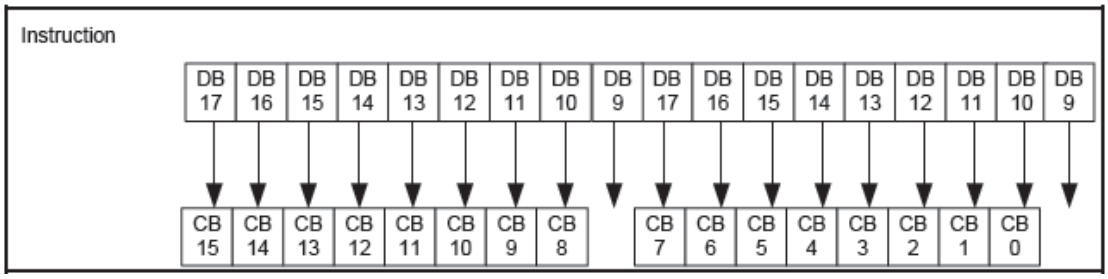


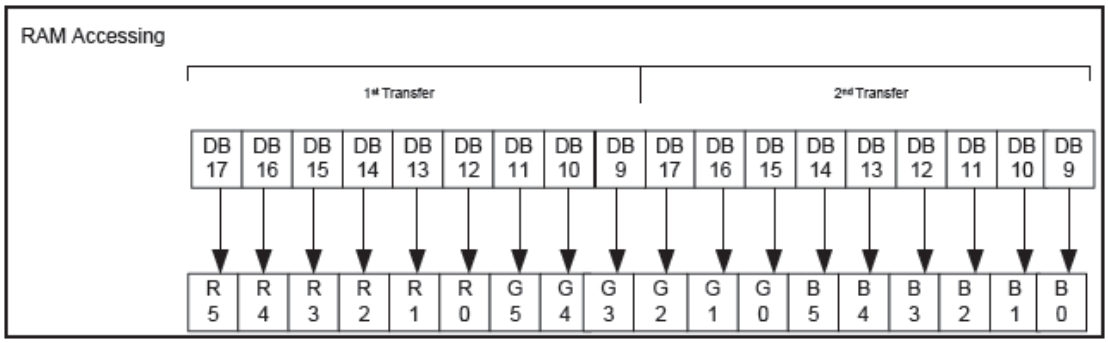
7.1.2 80-system 16-bit interface



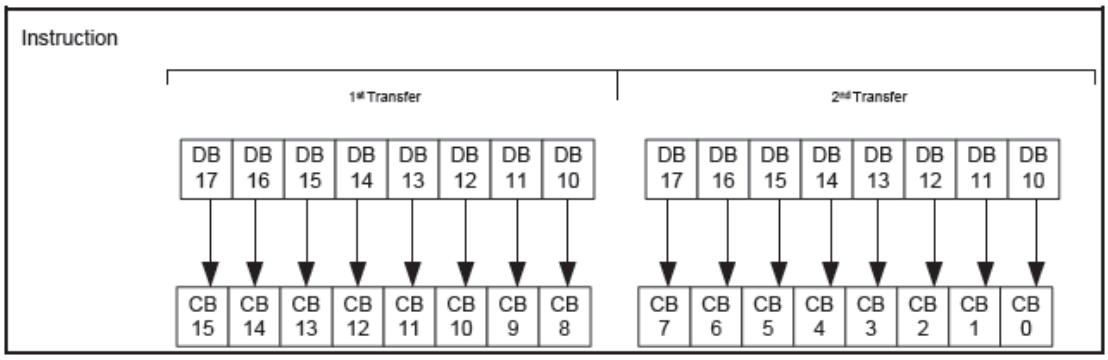


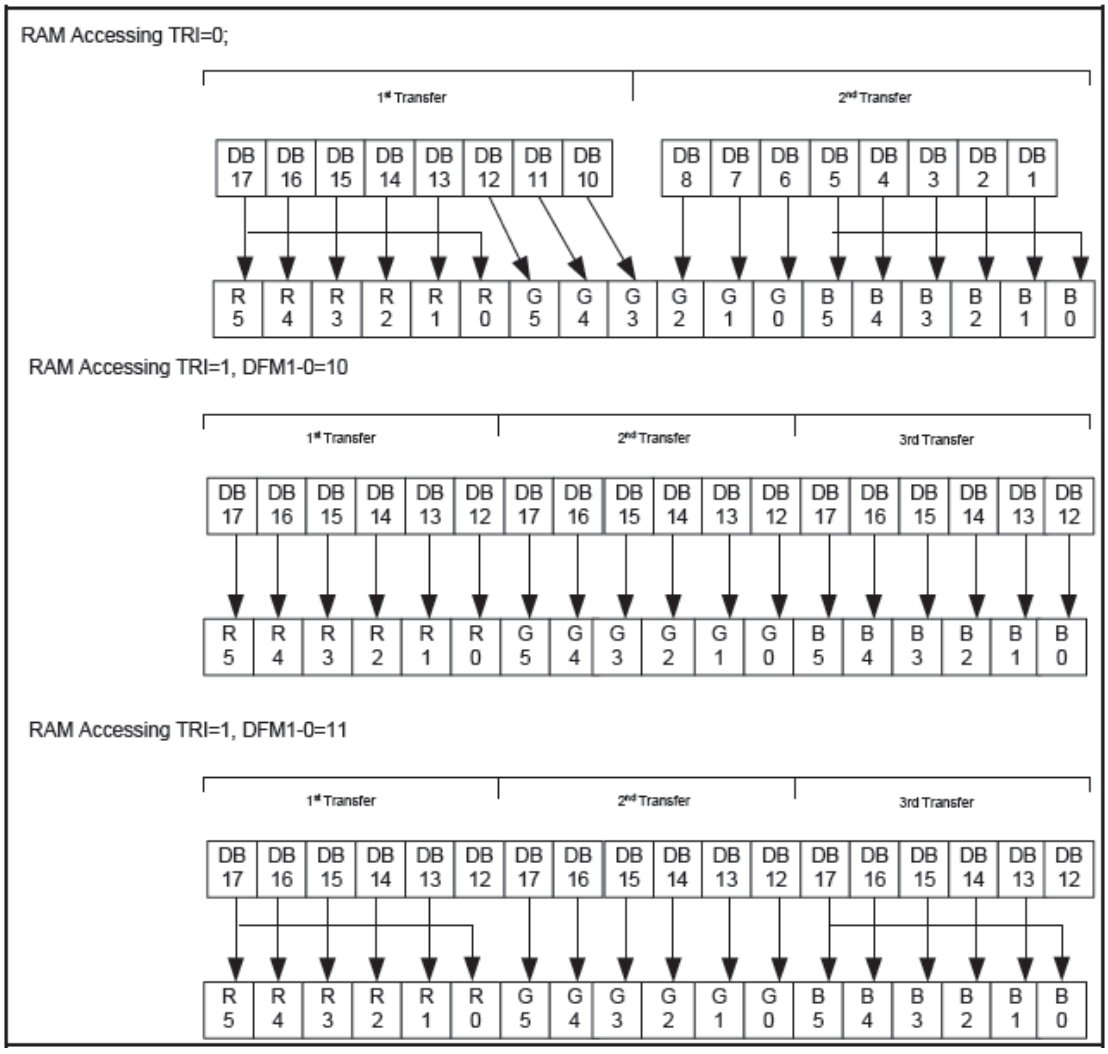
7.1.3 80-system 9-bit interface





7.1.4 80-system 8-bit interface



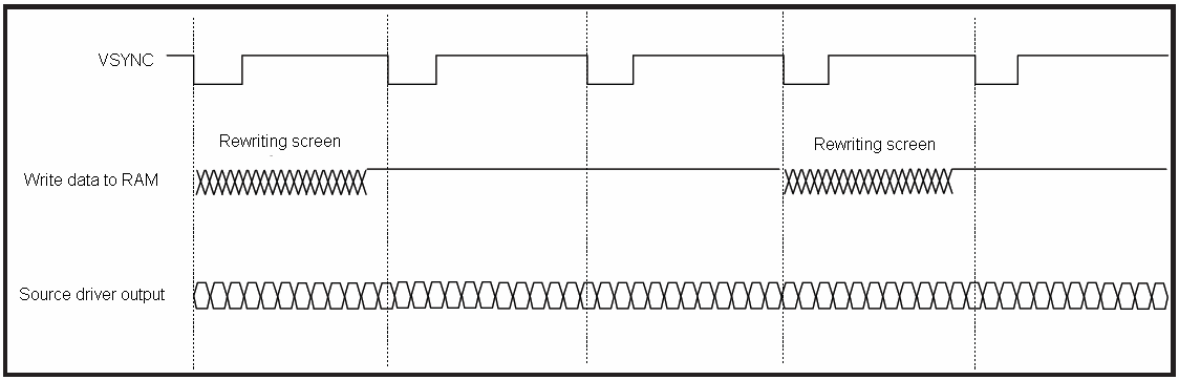


7.2 VSYNC interface

The SPFD5420A also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. The below figure illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. SPFD5420A can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode.



In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

$$Input\ clock\ frequency = FrameRate\ x\ (DisplayLines + FrontPorch + BackPorch)\ x\ 16\ x\ variance$$

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

7.3 Instruction List

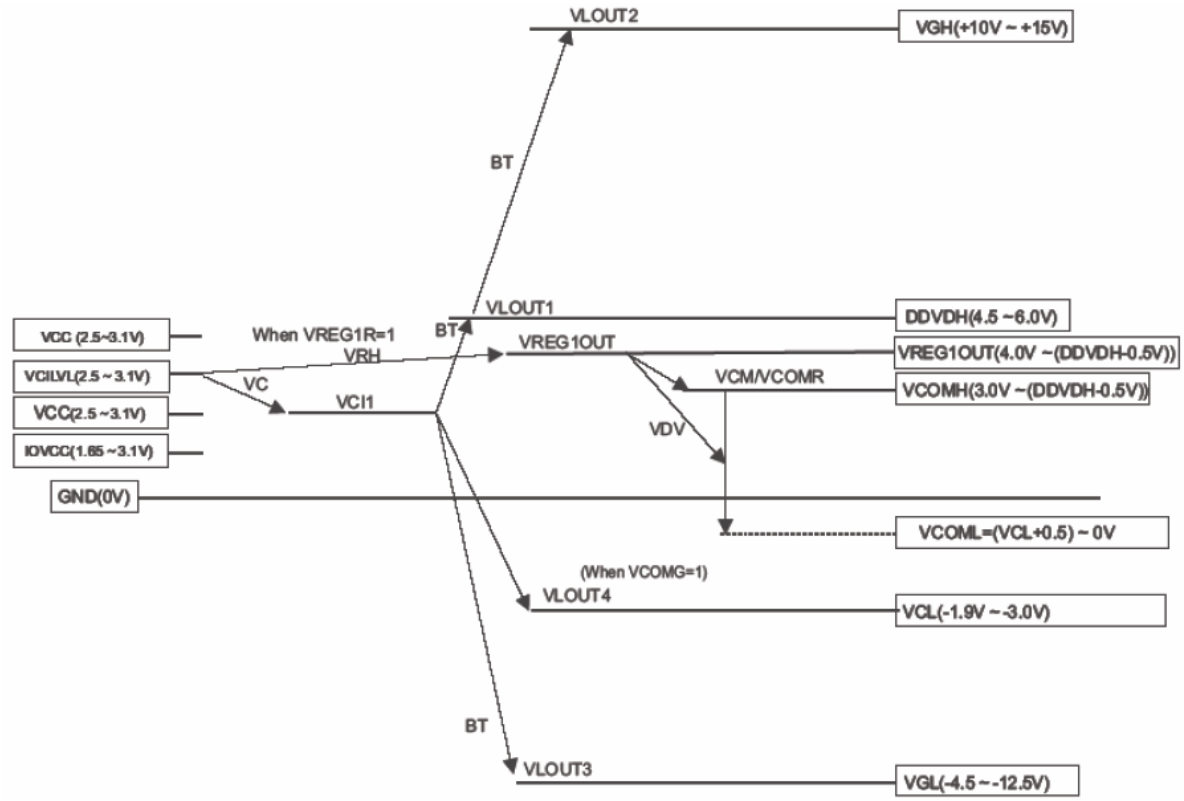
Main LCD Driver IC: SPFD5420A

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
000h	ID Read	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0
001h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	0
002h	LCD Drive Waveform Control	0	0	0	0	0	0	0	B/C (0)	0	0	0	0	0	0	NW1 (0)	NW0 (0)
003h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	EPF1 (0)	EPF0 (0)
004h-006h	Setting disabled																
007h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	VON (0)	GON (0)	DTE (0)	0	0	D1 (0)	D0 (0)
008h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
009h	Low Power Control (1)	0	0	0	0	PTV (0)	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)
00Ah	Setting Disabled																
00Bh	Low Power Control (2)	0	0	0	0	0	0	0	0	0	0	0	VEM0 (0)	0	0	0	COL (0)
0Ch	External Display Controll (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
00Dh-00Eh	Setting Disabled																
00Fh	External Display Controll (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)
010h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (1)	RTNI1 (1)	RTNI0 (1)
011h	Panel interface Control 2	0	0	0	0	0	NOWI2 (0)	NOWI1 (0)	NOWI0 (0)	0	0	0	0	0	SDTI2 (0)	SDTI1 (0)	SDTI0 (0)
012h	Panel interface Control 3	0	0	0	0	0	0	VEQW11 (0)	VEQW10 (0)	0	0	0	0	0	0	0	0
013-01Fh	Setting Disabled																
020h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (0)	DIVE0 (0)	0	RTNE6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
021h	Panel Interface Control 5	0	0	0	0	NOWE3 (0)	NOWE2 (0)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	SDTE3 (0)	SDTE2 (0)	SDTE1 (0)	SDTE0 (0)
022h	Panel Interface Control 6	0	0	0	0	0	VEQWE2 (0)	VEQWE1 (0)	VEQWE0 (0)	0	0	0	0	0	0	0	0
023h-08Fh	Setting Disabled																
090h	Frame Marker Control	FMKM (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)
091h-0FFh	Setting disabled																
100h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	0	AP1 (0)	AP0 (0)	0	DSTB (0)	SLP (0)	0
101h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)
102h	Power Control (3)	0	0	0	0	0	0	0	VCMR0 (0)	VREG1R (0)	0	PSON (0)	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
103h	Power Control (4)	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0
104h-106h	Setting disabled																
107h	Power Control (5)	0	0	0	0	0	0	0	0	0	0	0	DCM0 (0)	DCT3 (0)	DCT2 (0)	DCT1 (0)	DCT0 (0)
108-10Fh	Setting disabled																
110h	Power Control(6)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE (0)
111-1ffh	Setting disabled																
200h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
201h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
202h	Write Data to GRAM Read Data from GRAM	Data format is varied according to "interface".															
203-20Fh	Setting disabled																
210h	Window Horzontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
211h	Window Horzontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
212h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
213h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
214-27Fh	Setting Disabled																
280h	NVM Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	UID3 (0)	UID2 (0)	UID1 (0)	UID0 (0)
281h	VCom high voltage 1	0	0	0	0	0	0	0	0	0	0	0	VCM14 (0)	VCM13 (0)	VCM12 (0)	VCM11 (0)	VCM10 (0)
282h	VCom high voltage 2	0	0	0	0	0	0	0	0	VCMSEL (0)	0	0	VCM24 (0)	VCM23 (0)	VCM22 (0)	VCM21 (0)	VCM20 (0)
283-2FFh	Setting disabled																
300h	γ Control (1)																
301h	γ Control (2)																

302h	γ Control (3)																
303h	γ Control (4)																
304h	γ Control (5)																
305h	γ Control (6)																
306h	γ Control (7)																
307h	γ Control (8)																
308h	γ Control (9)																
309h	γ Control (10)																
30Ah	γ Control (11)																
30Bh	γ Control (12)																
30Ch	γ Control (13)																
30Dh	γ Control (14)																
30Eh	γ Control (15)																
30Fh	γ Control (16)																
310-3FFh	Setting disabled																
400h	Size of base image	GS (0)	0	NL5 (0)	NL4 (0)	NL3 (0)	NL2 (0)	NL1 (0)	NL0 (0)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
401h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)
402-403h	Setting disabled																
404h	Vertical Scoll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
405-4FFh	Setting disabled																
500h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
501h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
502h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
503h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)
504h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
505h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
506-605h	Setting Disabled																
606h	i80-I/F Endian Control	0	0	0	0	0	0	0	TCREV1 (0)	0	0	0	0	0	0	0	TCREV0 (0)
607-6EFh	Setting disabled																
6F0h	NVM access control	0	0	0	0	0	0	0	0	TE (0)	0	EOP1 (0)	EOP0 (0)	0	0	EAD1 (0)	EAD0 (0)
6F1-FFFh	Setting disabled																

8. Power Management System

Voltage Generation Diagram



9. Timing Characteristics

9.1 80-System Bus Interface Timing Characteristics

Normal write operation (HWM=0), IOVCC=1.65V~3.10V

Item		Symbol	Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	150	-	-
	Read	tCYCR	ns	450	-	-
Write low-level pulse width		PWLW	ns	55	-	-
Read low-level pulse width		PWLR	ns	170	-	-
Write high-level pulse width		PWHW	ns	70	-	-
Read high-level pulse width		PWHR	ns	250	-	-
Write/Read rise/ fall time		tWRr, WRf	ns	-	-	10
Setup time	Write (RS to CS*,WR*)	tAS	ns	0	-	-
	Read (RS to CS*, RD*)		ns	10	-	-
Address Hold Time		tAH	ns	2	-	-
Write data setup time		tDSW	ns	25	-	-
Write data hold time		tH	ns	10	-	-
Read data delay time		tDDR	ns	-	-	150
Read data hold time		tDHR	ns	5	-	-

9.2 Reset Timing Characteristics (IOVCC=1.65~3.10V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—
Reset rise time	trRES	μs	—	—	10

10.QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :
Ambient temperature : 25 ± 5°C
Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

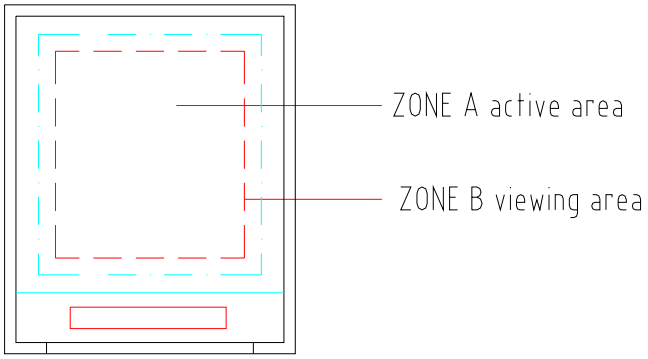
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

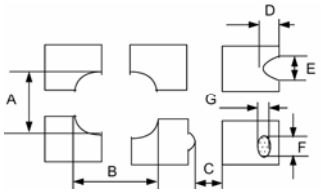
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under florescent light. The inspection area of LCD panel shall be within the range of following limits.



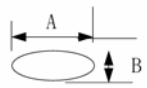
10.5 INSPECTION QUALITY CRITERIA

<table>
<tr><th>No.</th><th>Item</th><th>Criterion for defects</th><th>Class of Defec</th><th>Acceptable level</th></tr>
<tr><td>1</td><td>Non display</td><td>No non display is allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>2</td><td>Scratch,Dent of Plastic Mold</td><td>Serious one is not allowed</td><td>Major</td><td>0.65</td></tr>
<tr><td>3</td><td>Scratch on FPC</td><td>By limited sample</td><td>Major</td><td>0.65</td></tr>
<tr><td>4</td><td>Dot Defect</td><td><table><tr><th>Item</th><th>Number</th></tr><tr><td>Bright dot defect</td><td>N ≦ 0</td></tr><tr><td>Black dot defect</td><td>N ≦ 2</td></tr><tr><td>Total</td><td>N ≦ 2</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
<tr><td>5</td><td>Line Defect</td><td>None</td><td>Minor</td><td>1.5</td></tr>
<tr><td>6</td><td>Uneven Brightness : Line Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>7</td><td>Uneven Brightness : Dot Shape</td><td>None</td><td>Major</td><td>0.65</td></tr>
<tr><td>8</td><td>Display pattern</td><td> 

Unit:mm
<table><tr><td>$\frac{A+B}{2} \le 0.30$</td><td>0 < C</td><td>$\frac{D+E}{2} \le 0.25$</td><td>$\frac{F+G}{2} \le 0.25$</td></tr></table>
Note: 1. Acceptable up to 3 damages
2. NG if there're to two or more pinholes per dot</td><td>Minor</td><td>1.5</td></tr>
<tr><td>9</td><td>Scratch of Polarizer :Dot Shape s
Size:
$D = \frac{A+B}{2}$</td><td><table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>D ≤ 0.1</td><td>Ignore</td></tr><tr><td>0.1 < D ≤ 0.3</td><td>3</td></tr><tr><td>0.3 < D</td><td>0</td></tr></table></td><td>Minor</td><td>1.5</td></tr>
</table>

<table>
<tr>
<td>10</td>
<td>Scratch of Polarizer :

Line Shape

  </td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.05</td><td>L ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.1<W≤0.05</td><td>0.3 < L ≤ 2.0</td><td>N≦3.</td></tr>
<tr><td>0.1<W</td><td>-</td><td>See dot shape</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>11</td>
<td>Bubble in polarizer</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.3</td><td>Ignore</td></tr>
<tr><td>0.30 < D ≤ 0.50</td><td>1</td></tr>
<tr><td>0.50 < D</td><td>0</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>12</td>
<td>Stains inclusion : Line shape</td>
<td>
<table>
<tr><th>Width (mm)</th><th>Length (mm)</th><th>Acceptable number</th></tr>
<tr><td>W≤0.04</td><td>Ignore</td><td>Not Allowed</td></tr>
<tr><td>0.04<W≤0.06</td><td>L ≤ 0.8</td><td>Not Allowed</td></tr>
<tr><td>0.06<W</td><td>-</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
<tr>
<td>13</td>
<td>Stains inclusion : dot shape</td>
<td>
<table>
<tr><th>Size D (mm)</th><th>Acceptable number</th></tr>
<tr><td>D ≤ 0.1</td><td>Not Allowed</td></tr>
<tr><td>0.1 < D ≤ 0.2</td><td>Not Allowed</td></tr>
<tr><td>0.25< D</td><td>Not Allowed</td></tr>
</table>
</td>
<td>Minor</td>
<td>1.5</td>
</tr>
</table>

10.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=72 hrs	
Low Temperature Operation	-20±3°C , t=72 hrs	
High Temperature Storage	80±3°C , t=72hrs	1,2
Low Temperature Storage	-30±3°C , t=72 hrs	1,2
Humidity Test	40°C , Humidity 90%, 72 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 min. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency：10~55~10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 USE PRECAUTIONS

11.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light

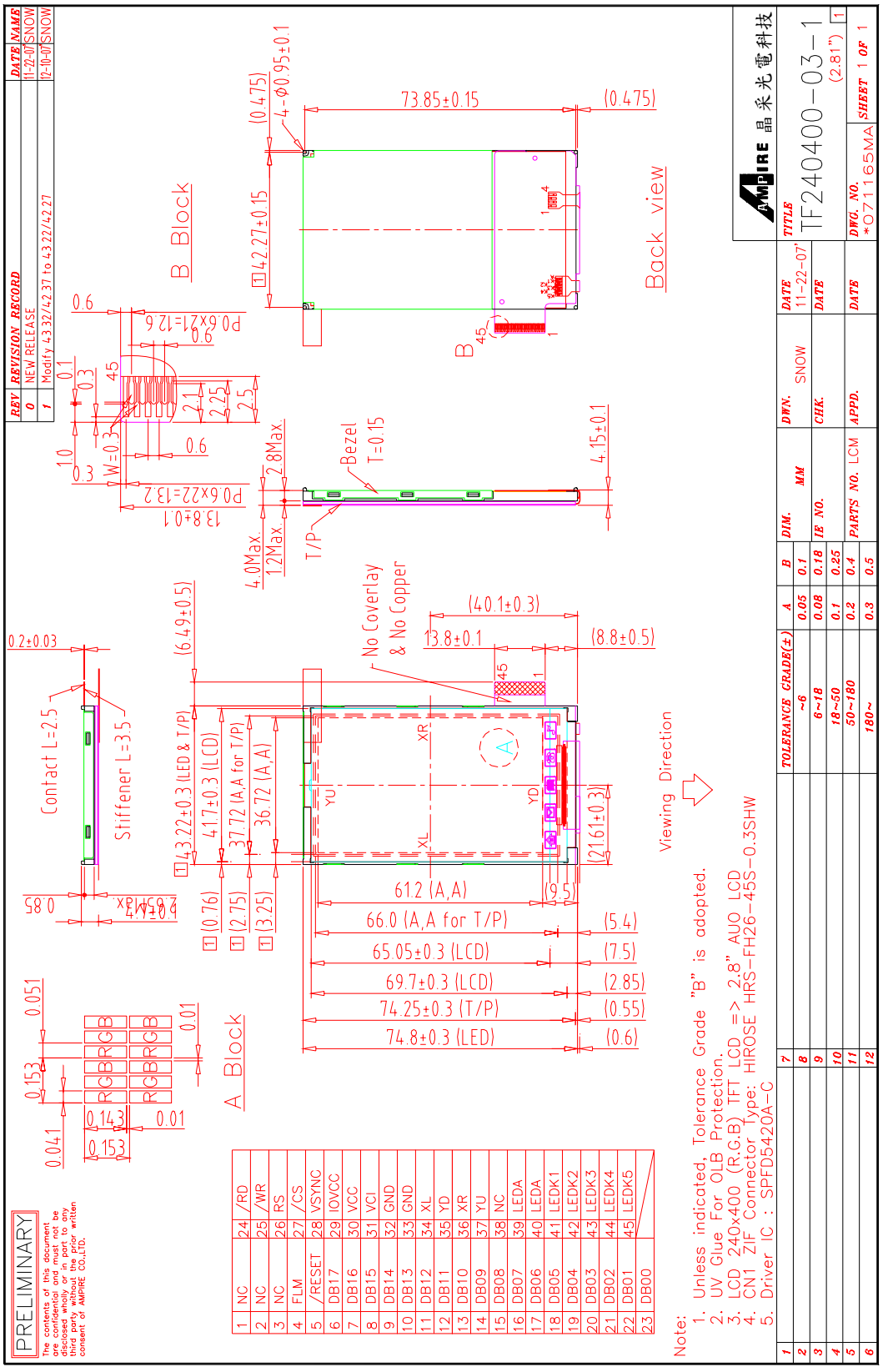
emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.
3) AMIPRE will provide one year warranty for all products and three months warrantee for all repairing products

12. MECHANIC DRAWING



1	NC	2	NC	3	NC	4	FLM	5	/RESET	6	DB17	7	DB16	8	DB15	9	DB14	10	DB13	11	DB12	12	DB11	13	DB10
14	DB09	15	DB08	16	DB07	17	DB06	18	DB05	19	DB04	20	DB03	21	DB02	22	DB01	23	DB00	24	/RD	25	/WR	26	RS
27	/CS	28	VSYNC	29	IOVCC	30	VCC	31	VCI	32	GND	33	GND	34	XL	35	YD	36	XR	37	YU	38	NC	39	LEDA
40	LEDA	41	LEDK1	42	LEDK2	43	LEDK3	44	LEDK4	45	LEDK5														