

A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

5.7-in COLOR TFT MODULE W/ TOUCH

| | |
|----------------------|-------------------------|
| CUSTOMER: | |
| CUSTOMER PART NO. | |
| AMP DISPLAY PART NO. | AM-320240N1TMQW-TW6H(R) |
| APPROVED BY: | |
| DATE: | |

☐

APPROVED FOR SPECIFICATIONS

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APPROVED FOR SPECIFICATION AND PROTOTYPES

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RECORD OF REVISION

| Revision Date | Page | Contents | Editor |
|---------------|------|--|--------|
| 2007/10/9 | - | New Release TFT LCD controller + Pin Header (8bit 80 interface) + TP + TP controller | Edward |

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1 Features

5.7 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 5.7" TFT-LCD panel, LCD controller, power driver circuit and backlight unit.

1.1 TFT Panel Feature :

- (1) Construction: 5.7" a-Si color TFT-LCD, White LED / CCFL Backlight and PCB.
- (2) Resolution (pixel): 320(R.G.B) X240
- (3) Number of the Colors : 262K colors (R , G , B 6 bit digital each)
- (4) LCD type : Transmissive Color TFT LCD (normally White)
- (5) Interface: 34 pin Pin Header.
- (6) Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.
- (7) Viewing Direction: 6 O'clock (The direction it's hard to be discolored):

1.2 LCD Controller Feature:

- (1) MCU interface 8/9/16/18 bit 80&68 series MCU interface.
- (2) Display RAM size : 640x240x3x6 bits. Ex:320x240 two frame buffer with 262K colors.
- (3) Arbitrary display memory start position selection.
- (4) MCU interface : 8 bit 80 MPU interface.
- (5) 8 bit / 16 bit interface support 65K (R5G6B5) /262K(R6G6B6) colors data format.
- (6) 9 bit / 18 bit interface support 262K(R6G6B6) colors data format only.

2 Physical specifications

| Item | Specifications | Unit | |
|-------------------------|---------------------------|------|--|
| Display resolution(dot) | 960 (W) x 240(H) | Mm | |
| Active area | 115.2 (W) x 86.4 (H) | Mm | |
| Screen size | 5.7(Diagonal) | Mm | |
| Pixel size | 120 (W) x 360 (H) | Um | |
| Color configuration | R.G.B stripe | | |
| Overall dimension | 131.0(W)x102.2(H)x14.5(D) | Mm | |
| Weight | T.B.D | Mg | |
| Backlight unit | LED | | |

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3 Default Setting & Option

- Interface :

The user can select the MCU interface by change the Jumper & Resister Array.

| Setting Interface Type | JP1 | RA1 | RA2 | RA3 | RA4 | Remark |
|---------------------------|-------------------------------|-------------|-------------|-------------|-------------------|----------------|
| 80-18Bit interface | 1,2 short 2,3 open | 2K ohm | OPEN | OPEN | OPEN | |
| 80-16Bit interface | 1,2 short 2,3 open | OPEN | 2K ohm | OPEN | OPEN | |
| 80-9Bit interface | 1,2 short 2,3 open | OPEN | OPEN | 2K ohm | OPEN | |
| 80-8Bit interface | 1,2 short 2,3 open | OPEN | OPEN | OPEN | 2K ohm | Default |
| 68-18Bit interface | 1,2 open 2,3 short | 2K ohm | OPEN | OPEN | OPEN | |
| 68-16Bit interface | 1,2 open 2,3 short | OPEN | 2K ohm | OPEN | OPEN | |
| 68-9Bit interface | 1,2 open 2,3 short | OPEN | OPEN | 2K ohm | OPEN | |
| 68-8Bit interface | 1,2 open 2,3 short | OPEN | OPEN | OPEN | 2K ohm | |

- Connector

The user can select the connector type.

| Option | | Support interface | Remark |
|--|--|--------------------------------------|----------------|
| 24 Pin FFC Cable (Pitch1.0x24pin) | | 80/68 8bit interface only | |
| 34Pin Pin Header (Pitch 2.54 x 34 pin) | | 80/68 8/9/16/18 bit interface | Default |

- Touch panel and Touch panel controller:

The user can select the with TP controller or without TP controller.

| Pin Define Option | SK/X1 | DO/X2 | DI/Y1 | TPCS/Y2 | IRQ | Remark |
|---|-----------|-----------|-----------|-------------|------------|----------------|
| Without TP | NC | NC | NC | NC | NC | |
| With TP / Without TP controller | X1 | X2 | Y1 | Y2 | NC | |
| With TP / With TP controller | SK | DO | DI | TPCS | IRQ | Default |

If user want to change the default setting for mass production, please contact with Amprie. We'll apply a new P/N for you.

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4 Electrical specification

4.1 Absolute max. ratings

4.1.1 Electrical Absolute max. ratings

| Item | Symbol | Condition | Min. | Max. | Unit | Remark |
|---------------|-----------------|-----------|------|---------|------|--------|
| Power voltage | VDD | VSS=0 | -0.3 | 5.5 | V | |
| Input voltage | V _{in} | | -0.3 | VDD+0.3 | V | Note 1 |

Note1: /CS,/WR,/RD,RS,DB0~DB7

4.1.2 Environmental Absolute max. ratings

| Item | OPERATING | | STORAGE | | Remark |
|---------------|----------------|-----|----------------|-----|-----------------|
| | MIN | MAX | MIN | MAX | |
| Temperature | -20 | 70 | -30 | 80 | Note2,3,4,5,6,7 |
| Humidity | Note1 | | Note1 | | |
| Corrosive Gas | Not Acceptable | | Not Acceptable | | |

Note1 : Ta ≤ 40°C : 85% RH max

Ta > 40°C : Absolute humidity must be lower than the humidity of 85%RH at 40°C

Note2 : For storage condition Ta at -30°C < 48h , at 80°C < 100h

For operating condition Ta at -20°C < 100h

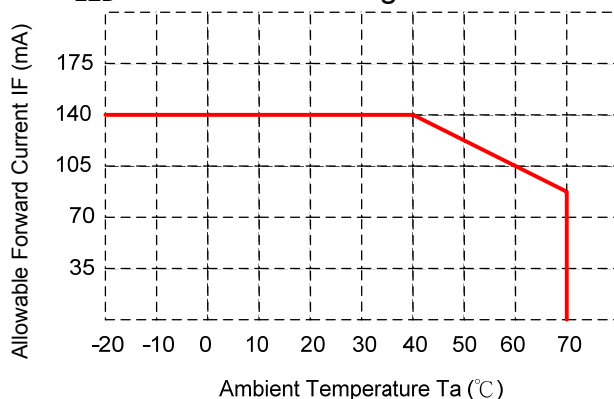
Note3 : Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Note4 : The response time will be slower at low temperature.

Note5 : Only operation is guaranteed at operating temperature. Contrast , response time, another display quality are evaluated at +25°C

Note6 :

- LED BL : When LCM is operated over 40°C ambient temperature, the I_{LED} of the LED back-light should be follow :



Note7 : This is panel surface temperature, not ambient temperature.

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Note8 :

- LED BL:When LCM be operated over than 40°C , the life time of the LED back-light will be reduced.

4.1.3 LED back-light Unit Absolute max. ratings

| Item | Symbol | Ratings | Unit | Remark |
|----------------------|--------|---------|------|--------|
| Peak forward Current | IF | 350 | mA | |
| Reverse Voltage | VR | 30 | V | |
| Power Dissipation | Po | 1.2 | W | |

4.2 Electrical characteristics

4.2.1 DC Electrical characteristic of the LCD

Typical operting conditions (VSS=0V)

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------------------------|---------|-----------------|------|------|------|------|--------|
| Power supply | | VDD | 3.1 | 5.0 | 5.2 | V | |
| Input Voltage for logic | H Level | V _{IH} | 2.0 | - | 5.5 | V | Note 1 |
| | L Level | V _{IL} | VSS | - | 0.8 | V | |
| Output Voltage for Logic | H Level | V _{OH} | 2.4 | - | VDD | V | Note 2 |
| | L Level | V _{OL} | VSS | | 0.4 | V | |
| Power Supply current | | IDD | - | 150 | - | mA | Note 3 |

Note1: With 5V Tolerance Input , /CS, /WR,/RD,RS,DB0~DB17

Note2: DB0~DB17

Note3: f_v =60Hz , Ta=25°C , VDD=3.3V , DCLK=10MHz, PLL frequency=40MHz,

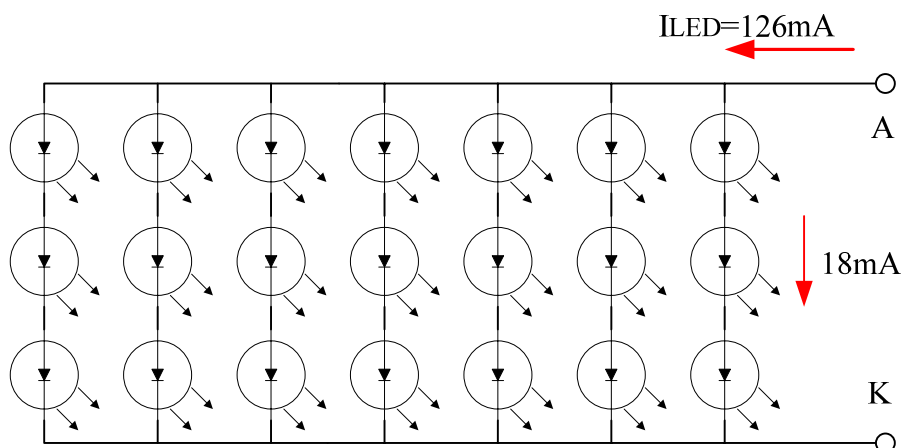
Display pattern : All Black

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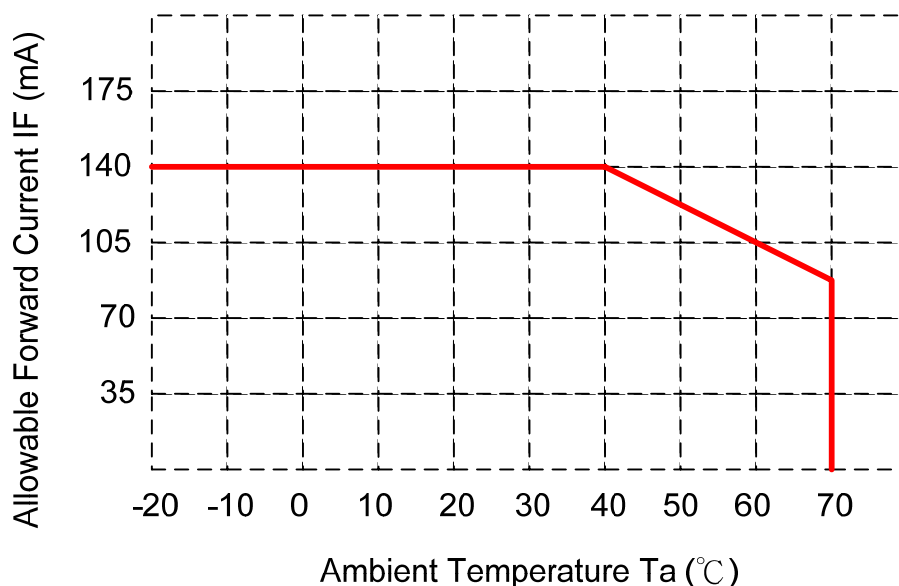
4.2.2 Electrical characteristic of LED Back-light

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---------------------|-----------|--------|------|------|------|--------------------------------------|
| LED voltage | V_{AK} | -- | 10.5 | 12 | V | $I_{LED} = 140mA, T_a = 25^{\circ}C$ |
| LED forward current | I_{LED} | -- | 126 | 140 | mA | $T_a = 25^{\circ}C$ |
| | I_{LED} | -- | 84 | 105 | mA | $T_a = 60^{\circ}C$ |
| Lamp life time | | 30,000 | - | - | Hr | $I_{LED} = 126mA, T_a = 25^{\circ}C$ |



- The constant current source is needed for white LED back-light driving.

When LCM is operated over 60°C ambient temperature, the I_{LED} of the LED back-light should be adjusted to 105mA max

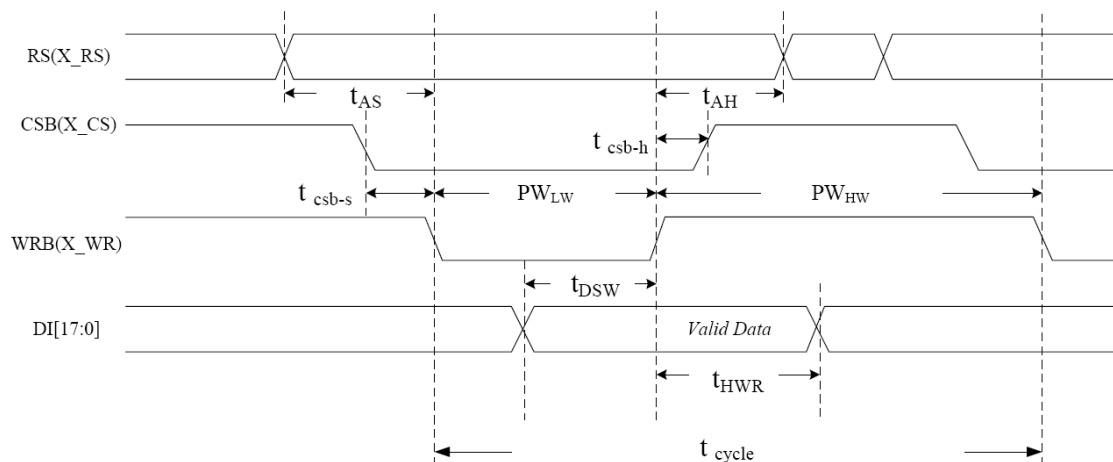


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3.3 AC Timing characteristic of the Graphic TFT LCD controller

4.3 80 series Timing

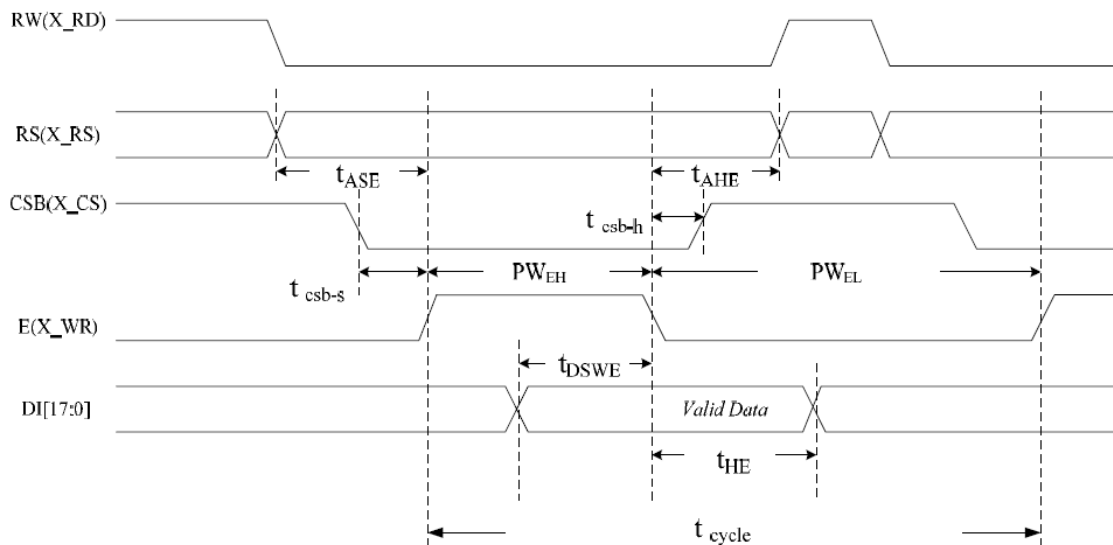


| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|-------------|-------------------------------|-----|-----|-----|------|--------|
| t_{cycle} | Enable cycle time | 100 | 200 | | ns | |
| PW_{HW} | Enable high-level pulse width | 66 | 70 | | ns | |
| PW_{LW} | Enable low-level pulse width | 33 | 130 | | ns | |
| t_{AS} | RS setup time | 16 | 25 | | ns | |
| t_{AH} | RS hold time | 16 | 45 | | ns | |
| t_{DSW} | Write data setup time | 50 | 50 | | ns | |
| t_{HWR} | Write data hold time | 50 | 40 | | ns | |
| t_{csb-s} | CSB setup time | 16 | 20 | | ns | |
| t_{csb-h} | CSB hold time | 16 | 30 | | ns | |

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4.4 68series Timing



| Symbol | Parameter | Min | Typ | Max | Unit | Remark |
|-------------|-------------------------------|-----|-----|-----|------|--------|
| t_{cycle} | Enable cycle time | 100 | 200 | | ns | |
| PW_{EH} | Enable high-level pulse width | 66 | 70 | | ns | |
| PW_{EL} | Enable low level pulse width | 33 | 130 | | ns | |
| t_{ase} | RS setup time | 16 | 25 | | ns | |
| t_{ah} | RS hold time | 16 | 45 | | ns | |
| t_{DSWE} | Write data setup time | 50 | 50 | | ns | |
| t_{HE} | Write data hold time | 50 | 40 | | ns | |
| t_{csb-s} | CSB setup time | 16 | 20 | | ns | |
| t_{csbh} | CSB hold time | 16 | 30 | | ns | |

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5 Optical specification**5.1 Optical characteristic :**

| Item | | Symbol | Conditon | Min. | Typ. | Max. | Unit | Remark |
|------------------------------|--------|--------------|--------------------------------------|-------|-------|-------|----------|--|
| Response Time | Rise | T_r | $\Theta=0^\circ$ | - | 15 | 30 | ms | Note 1,2,3,5 |
| | Fall | T_f | | - | 35 | 50 | ms | |
| Contrast ratio | | CR | At optimized viewing angle | 200 | 350 | - | | Note 1,2,4,5 |
| Viewing Angle | Top | $CR \geq 10$ | | 55 | 60 | - | deg. | Note1,2, 5,6 |
| | Bottom | | | 45 | 50 | - | | |
| | Left | | | 55 | 60 | - | | |
| | Right | | | 55 | 60 | - | | |
| Brightness LED BL Without TP | | Y_L | $I_{LED}=126mA, 25^\circ C$ | 427.5 | 450 | - | cd/m^2 | Note 7 |
| | | | $I_{LED}=140mA, 25^\circ C$ | 475 | 500 | - | cd/m^2 | |
| Brightness LED BL With TP | | Y_L | $I_{LED}=126mA, 25^\circ C$ | 342 | 360 | - | cd/m^2 | Note 7 |
| | | | $I_{LED}=140mA, 25^\circ C$ | 380 | 400 | - | cd/m^2 | |
| Red chromaticity | | XR | $\Theta=0^\circ$ $\Theta=0^\circ$ | 0.610 | 0.640 | 0.670 | | Note 7 For reference only. These data should be update according the prototype. |
| | | YR | | 0.314 | 0.344 | 0.374 | | |
| Green chromaticity | | XG | | 0.268 | 0.298 | 0.328 | | |
| | | YG | | 0.553 | 0.583 | 0.613 | | |
| Blue chromaticity | | XB | | 0.102 | 0.132 | 0.162 | | |
| | | YB | | 0.107 | 0.137 | 0.167 | | |
| White chromaticity | | XW | | 0.282 | 0.312 | 0.342 | | |
| | | YW | | 0.299 | 0.329 | 0.359 | | |

()For reference only. These data should be update according the prototype.

Note 1:

- LED BL :Ambient temperature= $25^\circ C$,and lamp current $I_{LED}=140mA$.To be measured in the dark room.
- CCFL BL: Ambient temperature= $25^\circ C$,and lamp current $I_L=6 mArms$.To be measured in the dark room.

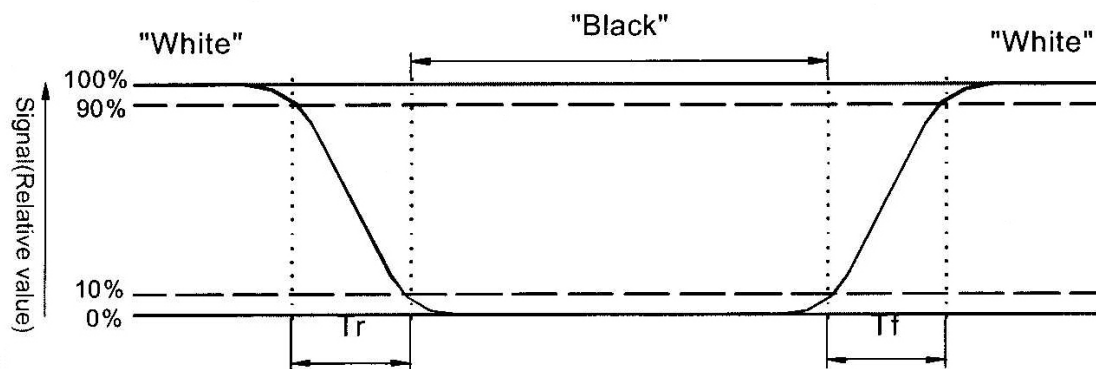
Note 2:To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7,after 10 minutes operation.

Note 3.Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from”white” to “black” (rising time),respectively.The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

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Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5:White $V_i = V_{i50} + 1.5V$

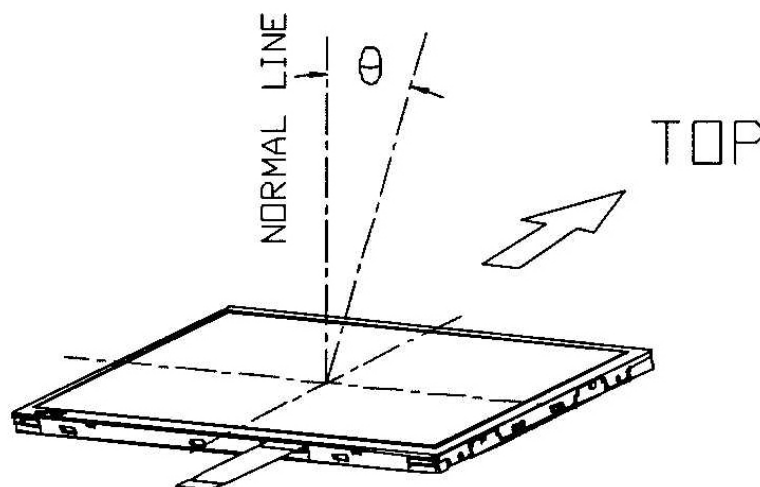
Black $V_i = V_{i50} + 2.0V$

" \pm " means that the analog input signal swings in phase with V_{COM} signal.

" $\frac{-}{+}$ " means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%.The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

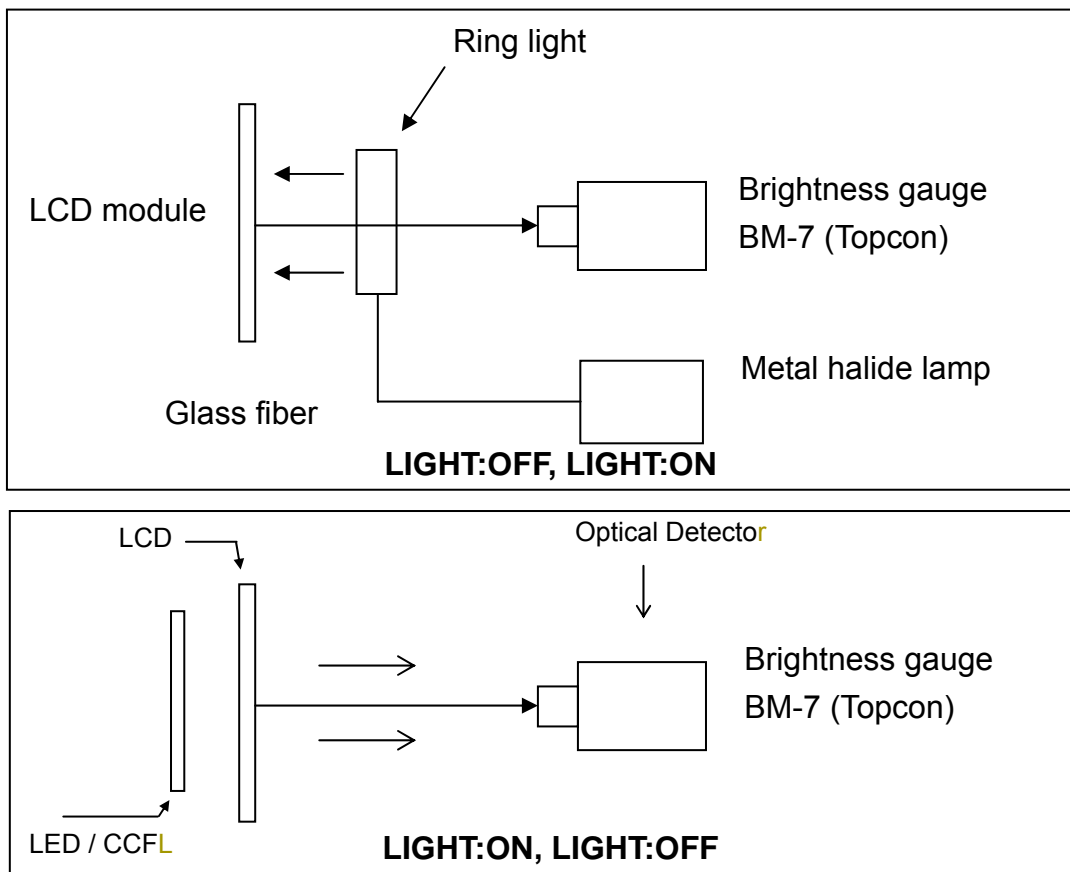
Note 6.Definition of viewing angle,Refer to figure as below.



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Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



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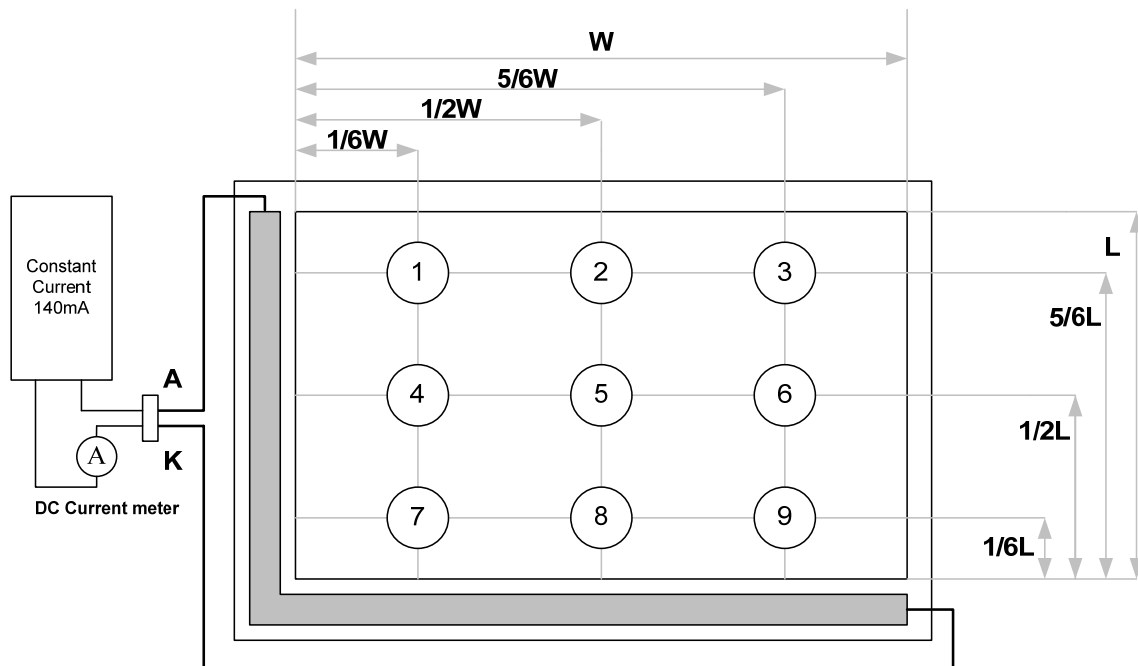
5.2 Optical characteristic of the LED Back-light

| ITEM | MIN | TYP | MAX | UNIT | Condition |
|-----------------------|------|------|------|-------|--------------------------------------|
| Bare Brightness | 3500 | -- | -- | Cd/m2 | $I_{LED} = 140mA, T_a = 25^{\circ}C$ |
| AVG. X of 1931 C.I.E. | 0.28 | 0.31 | 0.34 | -- | $I_{LED} = 140mA, T_a = 25^{\circ}C$ |
| AVG. X of 1931 C.I.E. | 0.28 | 0.31 | 0.34 | -- | $I_{LED} = 140mA, T_a = 25^{\circ}C$ |
| Brightness Uniformity | 80 | -- | -- | % | $I_{LED} = 140mA, T_a = 25^{\circ}C$ |

() For reference only. These data should be update according the prototype.

Note1 : Measurement after 10 minutes from LED BL operating.

Note2 : Measurement of the following 9 places on the display.



Note3: The Uniformity definition

$(\text{Min Brightness} / \text{Max Brightness}) \times 100\%$

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5.3 Touch Panel Electrical Specification

| Parameter | Condition | Standard Value |
|-----------------------|-----------|------------------------|
| Terminal Resistance | X Axis | 400 ~ 900 Ω |
| | Y Axis | 200 ~ 500 Ω |
| Insulating Resistance | DC 25 V | More than 10M Ω |
| Linearity | -- | ± 1.5 % |
| Notes life by Pen | Note a | 100,000 times(min) |
| Input life by finger | Note b | 1,000,000 times (min) |

Note A .

Notes area for pen notes life test is 10 x 9 mm.

Size of word is 7.5 x 6.72

Shape of pen end : R0.8

Load : 250 g

Note B

By Silicon rubber tapping at same point

Shape of rubber end : R8

Load : 200g

Frequency : 5 Hz

Interface

| No. | Symbol | Function |
|-----|--------|------------------------------------|
| 1 | XR | Touch Panel Right Signal in X Axis |
| 2 | YU | Touch Panel Upper Signal in Y Axis |
| 3 | XL | Touch Panel Left Signal in X Axis |
| 4 | YL | Touch Panel Low Signal in Y Axis |

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6 Interface specifications

6.1 Driving signals for the TFT panel

6.1.1 24pin FFC connector (Without for reference only)

(Suitable ZIF connector)

| Pin no | Symbol | I/O | Description | Remark |
|--------|-----------|-----|---|--------|
| 1 | /RESET | I | Reset signal for TFT LCD controller | |
| 2 | /RD(R/W) | I | 80mode : /RD low active signal for TFT LCD controller 68mode : R/W signal Hi: read Lo:Write | |
| 3 | /WR(E) | I | 80mode : /WR low active signal for TFT LCD controller 68mode : E signal latch on rising edge | |
| 4 | /CS | I | Chip select low active signal for TFT LCD controller | |
| 5 | RS | I | Register and Data select for TFT LCD controller | |
| 6 | DB0 | I/O | Data Bus | |
| 7 | DB1 | I/O | Data Bus | |
| 8 | DB2 | I/O | Data Bus | |
| 9 | DB3 | I/O | Data Bus | |
| 10 | DB4 | I/O | Data Bus | |
| 11 | DB5 | I/O | Data Bus | |
| 12 | DB6 | I/O | Data Bus | |
| 13 | DB7 | I/O | Data Bus | |
| 14 | VDD | - | Power supply for the logic (3.3V) | |
| 15 | VSS | - | GND | |
| 16 | NC | - | No connection | |
| 17 | NC | - | No connection | |
| 18 | SK/X1 | - | Serial clock for Touch panel controller Touch Panel Left Signal in X Axis | |
| 19 | DO/X2 | - | Data Output for Touch panel controller Touch Panel Right Signal in X Axis | |
| 20 | DI / Y1 | - | Data In for Touch panel controller Touch Panel Upper Signal in Y Axis | |
| 21 | TPCS / Y2 | - | Chip Select for Touch panel controller Touch Panel Lower Signal in X Axis | |
| 22 | INT | - | Interrupt for Touch panel controller | |
| 23 | NC | - | No connection | |
| 24 | NC | - | No connection | |

18~22 : SK, DO, DI, CS, INT for Touch Panel controller TSC2046

/ X1, X2, Y1, Y2 for Touch Panel (without TSC2046)

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6.1.234pin PIN Header

| Pin no | Symbol | Description | |
|--------|----------|---|--|
| 1 | /RESET | Reset signal for TFT LCD controller | |
| 3 | /RD(R/W) | 80mode : /RD low active signal for TFT LCD controller 68mode : R/W signal Hi: read Lo:Write | |
| 5 | /WR(E) | 80mode : /WR low active signal for TFT LCD controller 68mode : E signal latch on rising edge | |
| 7 | /CS | Chip select low active signal for TFT LCD controller | |
| 9 | RS | Register and Data select for TFT LCD controller | |
| 11 | DB0 | Data Bus | |
| 13 | DB1 | Data Bus | |
| 15 | DB2 | Data Bus | |
| 17 | DB3 | Data Bus | |
| 19 | DB4 | Data Bus | |
| 21 | DB5 | Data Bus | |
| 23 | DB6 | Data Bus | |
| 25 | DB7 | Data Bus | |
| 27 | VDD | Power supply for the logic (3.3V) | |
| 29 | VDD | Power supply for the logic (3.3V) | |
| 31 | VSS | GND | |
| 33 | VSS | GND | |

| Pin no | Symbol | Description | |
|--------|-----------|--|--|
| 2 | SK/X1 | Serial clock for Touch panel controller Touch Panel Left Signal in X Axis | |
| 4 | DO/X2 | Data Output for Touch panel controller Touch Panel Right Signal in X Axis | |
| 6 | DI / Y1 | Data In for Touch panel controller Touch Panel Upper Signal in Y Axis | |
| 8 | TPCS / Y2 | Chip Select for Touch panel controller Touch Panel Lower Signal in X Axis | |
| 10 | INT | Interrupt for Touch panel controller | |
| 12 | DB8 | Data Bus | |
| 14 | DB9 | Data Bus | |
| 16 | DB10 | Data Bus | |
| 18 | DB11 | Data Bus | |
| 20 | DB12 | Data Bus | |
| 22 | DB13 | Data Bus | |
| 24 | DB14 | Data Bus | |
| 26 | DB15 | Data Bus | |
| 28 | DB16 | Data Bus | |
| 30 | DB17 | Data Bus | |
| 32 | NC | No connection | |
| 34 | NC | No connection | |

Pni No 2,4,6,8: SK, DO, DI, CS, INT for Touch Panel controller TSC2046

/ X1, X2, Y1, Y2 for Touch Panel (without TSC2046)

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Driving signals for the back-light**6.1.3 LED Back-light**

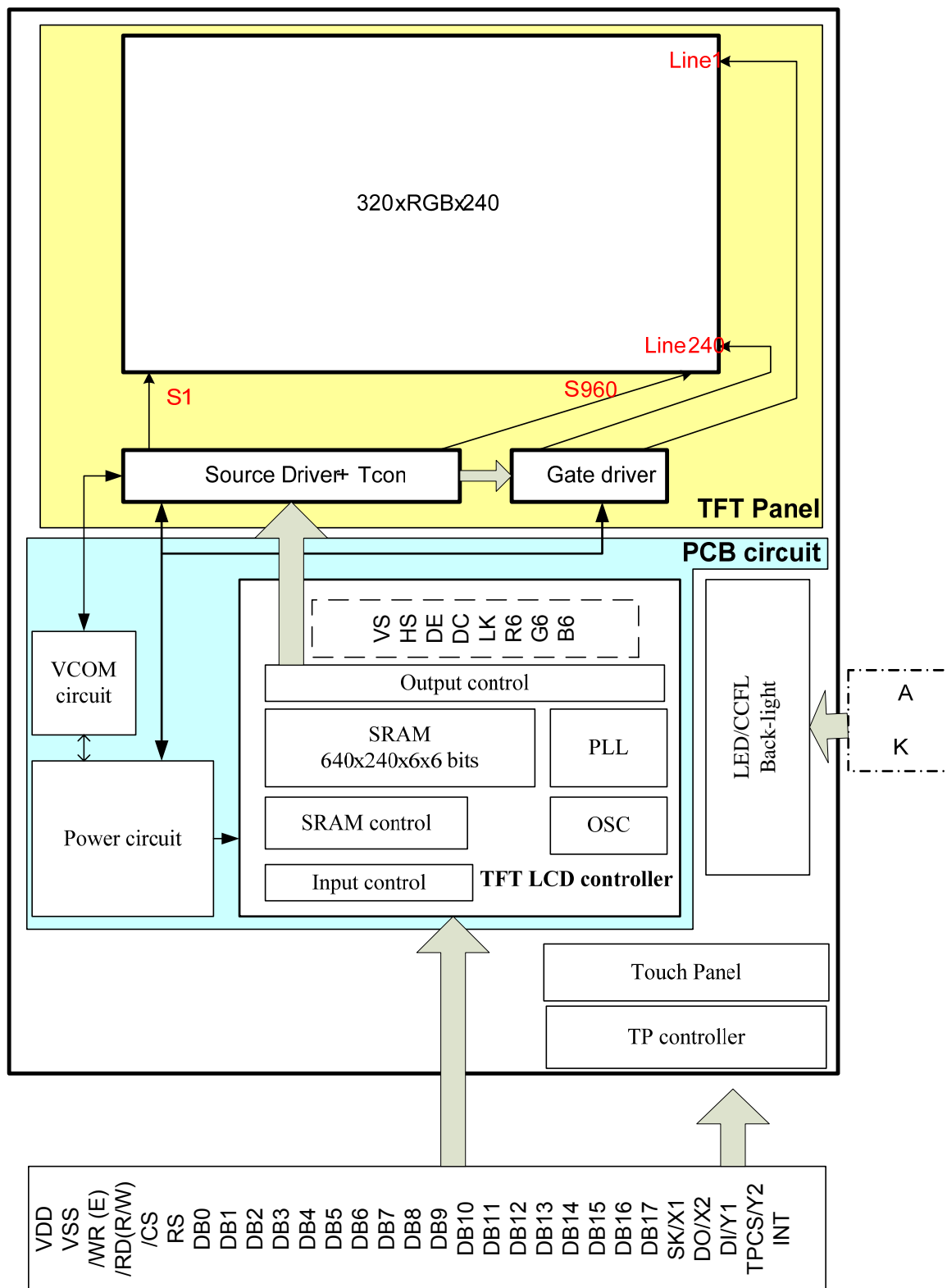
JST Housing: BHR-03VS-1

| Pin no | Symbol | Level | Description | Remark |
|--------|--------|-------|---------------|--------|
| 1 | A | - | LED Anode | |
| 2 | NC | - | No connection | |
| 3 | K | - | LED Cathode | |

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7 BLOCK DIAGRAM

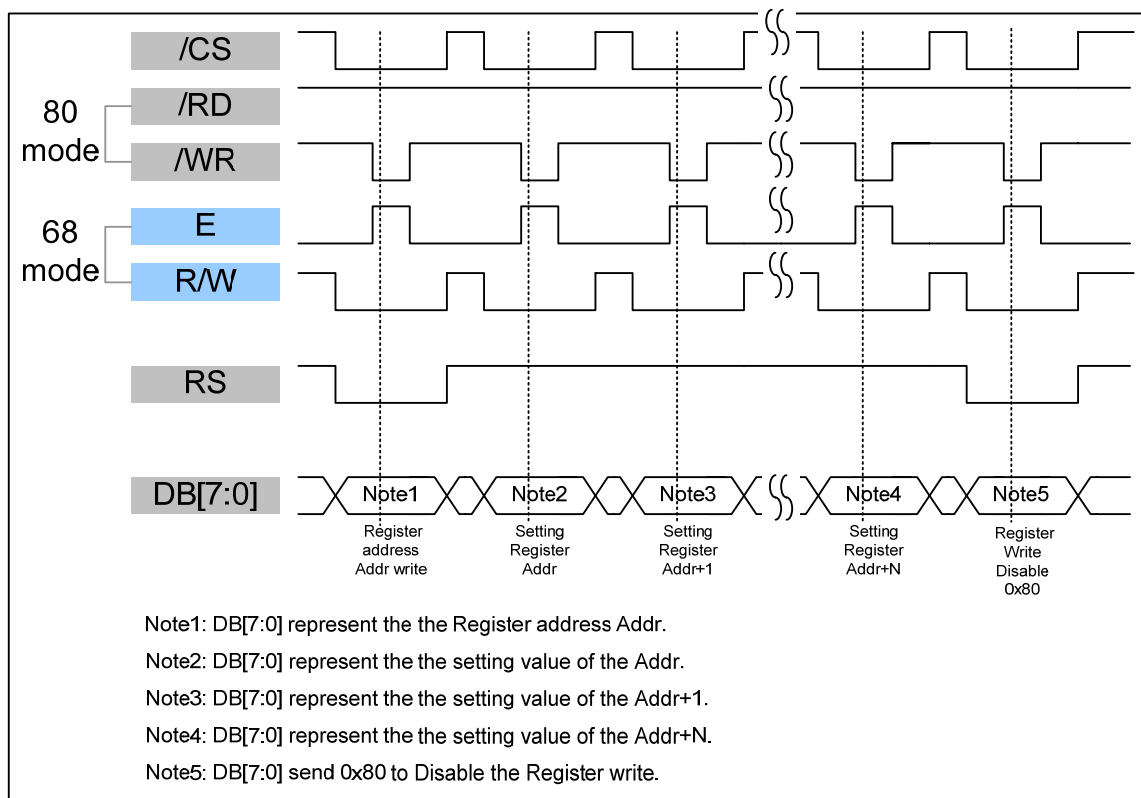


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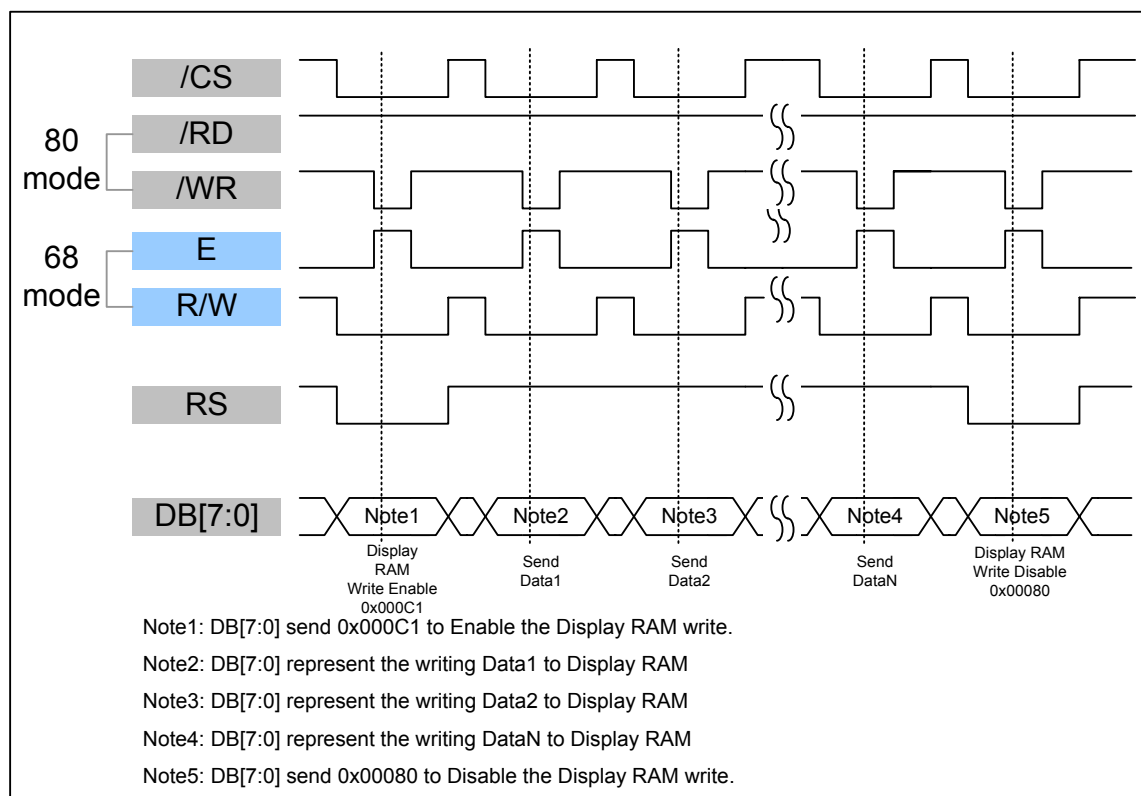
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8 Interface Protocol

8.1 8Bit-80/68- Write to Command Register



8.2 8Bit-80/68-Write to Display RAM



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8.3 Data transfer order Setting

8.3.1 8 bit interface 65K color (Pin12 65K/262K =Low)

| DB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|----|----|----|----|----|----|---|---|----|----|----|----|----|----|----|----|
| 1 st data | X | X | X | X | X | X | X | X | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 |
| 2 nd data | X | X | X | X | X | X | X | X | G2 | G1 | G0 | B4 | B3 | B2 | B1 | B0 |

8.3.2 8 bit interface 262K color (Pin12 65K/262K =High)

| DB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|----|----|----|----|----|----|---|---|----|----|----|----|----|----|----|----|
| 1 st data | X | X | X | X | X | X | X | X | | | | | | | R5 | R4 |
| 2 nd data | X | X | X | X | X | X | X | X | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 |
| 3 rd data | X | X | X | X | X | X | X | X | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

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9 Register Depiction

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|------------------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 00 | 00 | MSB of X-axis start position | | | | | | | | |
| Description | set the horizontals start position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 01 | 00 | LSB of X-axis start position | | | | | | | | |
| Description | set the horizontals start position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 02 | 01 | MSB of X-axis end position | | | | | | | | |
| Description | set the horizontals end position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 03 | 3F | LSB of X-axis end position | | | | | | | | |
| Description | set the horizontals end position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 04 | 00 | MSB of Y-axis start position | | | | | | | | |
| Description | set the vertical start position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 05 | 00 | LSB of Y-axis start position | | | | | | | | |
| Description | Set the vertical start position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 06 | 00 | MSB of Y-axis end position | | | | | | | | |
| Description | set the vertical end position of display active region | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 07 | EF | LSB of Y-axis end position | | | | | | | | |
| Description | Set the vertical end position of display active region | | | | | | | | | |

To simplify the address control of display RAM access, the window area address function

allows for writing data only within a window area of display RAM specified by registers REG[00]~REG[07] .

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After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

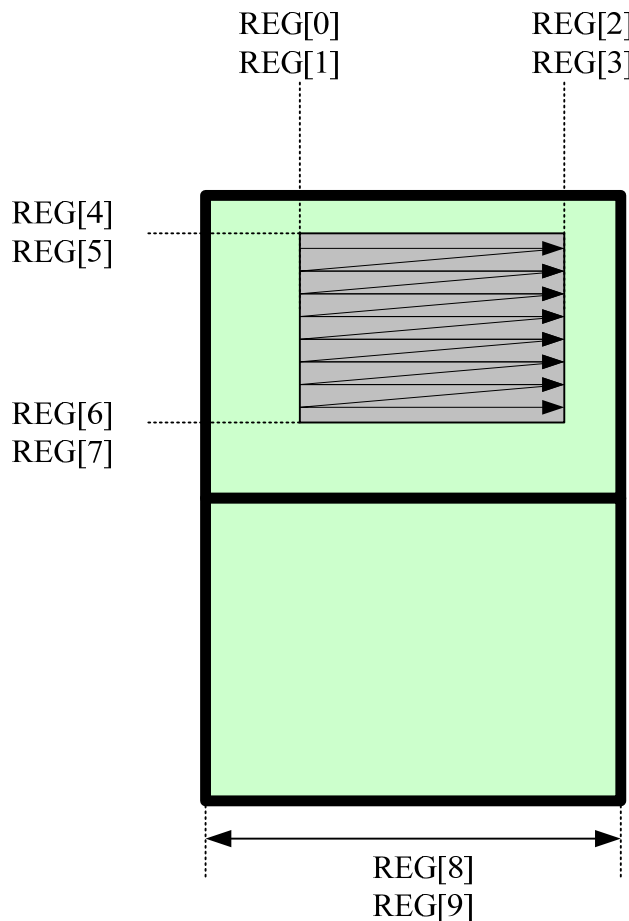
MIN X address (REG[0] & REG[1])

MAX X address (REG[2] & REG[3])

MIN Y address (REG[4] & REG[5])

MAX Y address (REG[6] & REG[7])

Therefore, data can be written consecutively without thinking the data address.



| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|----------------------|-----|-----|-----|-----|-----|-----|----------------------------|-----|--------|
| 08 | 01 | X | X | X | X | X | X | _PanelXSize H_Byte[1:0] | | |
| Description | Set the panel X size | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|----------------------|-------------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 09 | 40 | _PanelXSize L_Byte[7:0] | | | | | | | | |
| Description | Set the panel X size | | | | | | | | | |

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The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09] must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|----------------------------|-----|-----|-----|-----|-----|--|-----|-----|--------|
| 0A | 00 | X | X | X | X | X | [17:16] bits of memory write start address | | | |
| Description | Memory write start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|----------------------------|---|-----|-----|-----|-----|-----|-----|-----|--------|
| 0B | 00 | [15:8] bits of memory write start address | | | | | | | | |
| Description | Memory write start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|----------------------------|--|-----|-----|-----|-----|-----|-----|-----|--------|
| 0C | 00 | [7:0] bits of memory write start address | | | | | | | | |
| Description | Memory write start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|----------|----------|---------|-----|----------|---------|---------|-----|--------|
| 0x10 | 0x0D | Bit_SWAP | OUT_TEST | BUS_SEL | | Blanking | P/S_SEL | CLK_SEL | | |
| Description | "0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz | | | | | | | | | |
| | "0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel | | | | | | | | | |
| | "0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation) | | | | | | | | | |
| | "0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B | | | | | | | | | |
| | "0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0]) | | | | | | | | | |
| | "0x10_bit_swap[7]" : 0-normal | | | | | | | | | |
| | The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|-----|-----|------|-----|-----|------|-----|-----|--------|
| 0x11 | 00 | X | X | EVEN | | | _ODD | | | |
| Description | " Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved | | | | | | | | | |
| | Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved Must Set to 0x05 for AM320240N1 | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|--|---------------------|-----|-----|-----|---------------------|-----|-----|-----|--------|
| 0x12 | 00 | | | | | Hsync_stH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Hsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x13 | 00 | Hsync_stL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Hsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x14 | 00 | | | | | Hsync_pwH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Hsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x15 | 10 | Hsync pwL_Byte[7:0] | | | | | | | | |

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| | | | | | | | | | | |
|------------------------|---|--------------------|-----|-----|-----|--------------------|-----|-----|-----|--------|
| Description | For TFT output timing adjust: Hsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x16 | 00 | | | | | Hact_stH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x17 | 38 | Hact_stL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x18 | 01 | | | | | Hact_pwH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: DE pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x19 | 40 | Hact_pwL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: DE pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|--|-------------------|-----|-----|-----|-------------------|-----|-----|-----|--------|
| 0x1A | 01 | | | | | HtotalH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x1B | B8 | HtotalL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Hsync total clocks H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|--|---------------------|-----|-----|-----|---------------------|-----|-----|-----|--------|
| 0x1C | 00 | | | | | Vsync_stH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Vsync start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x1D | 00 | Vsync_stL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Vsync start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x1E | 00 | | | | | Vsync_pwH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Vsync pulse width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x1F | 08 | Vsync_pwL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Vsync pulse width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x20 | 00 | | | | | Vact_stH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Vertical DE pulse start position H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x21 | 12 | Vact_stL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Vertical DE pulse start position L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x22 | 00 | | | | | Vact_pwH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|--------------------|-----|-----|-----|-------------------|-----|-----|-----|--------|
| 0x23 | F0 | Vact_pwL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Vertical Active width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x24 | 01 | | | | | VtotalH_Byte[3:0] | | | | |
| Description | For TFT output timing adjust: Vertical total width H-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x25 | 09 | VtotalL_Byte[7:0] | | | | | | | | |
| Description | For TFT output timing adjust: Vertical total width L-Byte The default setting is suitable for AM320240N1. Don't need to modify it. | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---------------------------|-----|-----|-----|-----|-----|---|-----|-----|--------|
| 26 | 00 | X | X | X | X | X | [17:16] bits of memory read start address | | | |
| Description | Memory read start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---------------------------|---|-----|-----|-----|-----|-----|-----|-----|--------|
| 27 | 00 | [15:8] bits of memory write start address | | | | | | | | |
| Description | Memory read start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---------------------------|--|-----|-----|-----|-----|-----|-----|-----|--------|
| 28 | 00 | [7:0] bits of memory write start address | | | | | | | | |
| Description | Memory read start address | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|----------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 29 | 00 | [7:1] Reversed | | | | | | | | |
| Description | [0] Load output timing related setting (H sync., V sync. and DE) to take effect | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|-----|----------------------|-----|-----|-----|-----|-----|-----|--------|
| 0x2A | 00 | X | TestPatternRout[6:0] | | | | | | | |
| Description | When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0] | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x2B | 00 | X | TestPatternGout[6:0] | | | | | | | |
| Description | When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0] | | | | | | | | | |
| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
| 0x2C | 00 | X | TestPatternBout[6:0] | | | | | | | |
| Description | When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0] | | | | | | | | | |

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.

REG[2A]=0x3F
REG[2B]=0x00
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x3F
REG[2C]=0x00

REG[2A]=0x00
REG[2B]=0x00
REG[2C]=0x3F

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|-----|-----|-----|-----|-----|------------------------|---------------|-----|--------|
| 0x2D | 00 | X | X | X | X | [3] | Rising/falling edge[2] | _rotate [1:0] | | |
| Description | [3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON | | | | | | | | | |
| | Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK. | | | | | | | | | |
| | _rotate [1:0]: 00 : rotate 0 degree 01 : rotate 90 degree 10 : rotate 270 degree 11 : rotate 180 degree | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---------------------------|-----|-----|-----|-----|-----|-------------------------|-----|-----|--------|
| 30 | 00 | X | X | X | X | X | H byte H-Offset[3:0] | | | |
| Description | Set the Horizontal offset | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---------------------------|----------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 31 | 00 | L byte H-Offset[7:0] | | | | | | | | |
| Description | Set the Horizontal offset | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|-------------------------|-----|-----|-----|-----|-----|--------------------------|-----|-----|--------|
| 32 | 00 | X | X | X | X | X | _H byte V-Offset[3:0] | | | |
| Description | Set the Vertical offset | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|-------------------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 33 | 00 | _L byte V-Offset[7:0] | | | | | | | | |
| Description | Set the Vertical offset | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|----------------|-----|-----|-----|-----|-----------------------|-----|-----|--------|
| 34 | 00 | [7:4] Reserved | | | | | _H byte H-def[3:0] | | | |
| Description | [3:0] MSB of image horizontal physical resolution in memory | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|--------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 35 | 40 | _L byte H-def[7:0] | | | | | | | | |
| Description | [7:0] LSB of image horizontal physical resolution in memory | | | | | | | | | |

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| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|----------------|-----|-----|-----|-----|--------------------|-----|-----|--------|
| 36 | 01 | [7:4] Reserved | | | | | _H byte V-def[3:0] | | | |
| Description | [3:0] MSB of image vertical physical resolution in memory | | | | | | | | | |

| Register Address (Hex) | Default (Hex) | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Remark |
|------------------------|---|--------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 37 | E0 | _L byte V-def[7:0] | | | | | | | | |
| Description | [7:0] LSB of image vertical physical resolution in memory | | | | | | | | | |

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].

EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0

EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

10 Application Note:

```
void main(void)
```

```
{
```

```
    Initial_AMP506 ( );
```

```
    Full_386SCR(0xf800);
```

```
    Full_386SCR(0x07e0);
```

```
    Full_386SCR(0x001f);
```

```
}
```

```
void AMP506_80Mode_Command_SendAddress(BYTE Addr)
```

```
{
```

```
    SET_nRD;           // /RD=1
```

```
    CLR_RS;            // RS=0
```

```
    CLR_CS1;           // /CS=0
```

```
    CLR_nWRL;          // /WR=0
```

```
    DB16OUT(Addr);     // Data Bus OUT
```

```
    SET_nWRL;          ///WR=1    /
```

```
    SET_RS;            // RS=1
```

```
    SET_CS1;           // CS=1
```

```
}
```

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```
void AMP506_80Mode_Command_SendData(BYTE Data)
```

```
{
    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Data);
    SET_nWRL;
    SET_RS;
    SET_CS1;
}
```

```
void AMP506_Command_Write(uint8 CMD_Address,uint8 CMD_Value)
```

```
{
    AMP506_80Mode_Command_SendAddress(CMD_Address);
    AMP506_80Mode_Command_SendData(CMD_Value);
}
```

```
void AMP506_80Mode_16Bit_Memory_SendData(uint16 Dat16bit)
```

```
{
    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Dat16bit>>8);
    SET_nWRL;                // Low to High Latch Data to AMP506 Buffer
    SET_CS1;

    SET_nRD;
    SET_RS;
    CLR_CS1;
    CLR_nWRL;
    DB16OUT(Dat16bit);
    SET_nWRL;                // Low to High Latch Data to AMP506 Buffer
    SET_CS1;
}
```

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}

void Initial_AMP506(void)

{

AMP506_Command_Write(0x40,0x12); /*[7:6] Reserved

[5] PLL control pins to select out frequency range

0: 20MHz ~ 100MHz 1: 100MHz ~ 300MHz

[4] Reserved [3] Reserved

[2:1] Output Driving Capability

00: 4mA 01: 8mA 10: 12mA 11: 16mA

[0] Output slew rate

0: Fast 1: Slow

*/

AMP506_Command_Write(0x41,0x01); //Set PLL=40Mhz * (0x42) / (0x41)

AMP506_Command_Write(0x42,0x01); //0x41 [7:6] Reserved [5:0] PLL Programmable

pre-divider, 6bit(1~63)

//0x42 [7:6] Reserved [5:0] PLL Programmable loop

divider, 6bit(1~63)

AMP506_Command_Write(0x00,0x00); // MSB of horizontal start coordinate value

AMP506_Command_Write(0x01,0x00); // LSB of horizontal start coordinate value

AMP506_Command_Write(0x02,0x01); // MSB of horizontal end coordinate value

AMP506_Command_Write(0x03,0x3F); // LSB of horizontal end coordinate value

AMP506_Command_Write(0x04,0x00); // MSB of vertical start coordinate value

AMP506_Command_Write(0x05,0x00); // LSB of vertical start coordinate value

AMP506_Command_Write(0x06,0x01); // MSB of vertical end coordinate value

AMP506_Command_Write(0x07,0x3F); // LSB of vertical end coordinate value

AMP506_Command_Write(0x08,0x01); // MSB of input image horizontal resolution

AMP506_Command_Write(0x09,0x40); // LSB of input image horizontal resolution

AMP506_Command_Write(0x0a,0x00); //[17:16] bits of memory write start address

AMP506_Command_Write(0x0b,0x00); //[15:8] bits of memory write start address

AMP506_Command_Write(0x0c,0x00); //[7:0] bits of memory write start address

AMP506_Command_Write(0x10,0x0D); /*[7] Output data bits swap 0: Normal 1:Swap

[6] Output test mode enable 0: disable 1: enable

[5:4] Serial mode data out bus selection

00: X_ODATA17 ~ X_ODATA12 active , others are set to

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zero

01: X_ODATA11 ~ X_ODATA06 active , others are set to

zero

10: X_ODATA05 ~ X_ODATA00 active , others are set to

zero

11: reserved

[3] Output data blanking

0: set output data to 0 **1: Normal display**

[2] Parallel or serial mode selection

0: serial data out **1: parallel data output**

[1:0] Output clock selection

00: system clock divided by 2

01: system clock divided by 4

10: system clock divided by 8

11: reserved */

AMP506_Command_Write(0x11,0x05);

/*[7] Reserved

[6:4] Even line of serial panel data out sequence or data bus order of parallel panel

000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others:

reserved

[3] Reversed

[2:0] Odd line of serial panel data out sequence

000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others:

reserved */

AMP506_Command_Write(0x12,0x00); // [3:0] MSB of output H sync. pulse start

position

AMP506_Command_Write(0x13,0x00); //[7:0] LSB of output H sync. pulse start position

AMP506_Command_Write(0x14,0x00); // [3:0] MSB of output H sync. pulse width

AMP506_Command_Write(0x15,0x10); //[7:0] LSB of output H sync. pulse width

AMP506_Command_Write(0x16,0x00); //[3:0] MSB of output DE horizontal start

position

AMP506_Command_Write(0x17,0x38); //[7:0] LSB of output DE horizontal start

position

AMP506_Command_Write(0x18,0x01); //[3:0] MSB of output DE horizontal active region in

pixel

AMP506_Command_Write(0x19,0x40); //[7:0] LSB of output DE horizontal active region

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in pixel

AMP506_Command_Write(0x1a,0x01); // [7:4] Reserved [3:0] MSB of output H total in

pixel

AMP506_Command_Write(0x1b,0xb8); // [7:0] LSB of output H total in pixel

AMP506_Command_Write(0x1c,0x00); // [3:0] MSB of output V sync. pulse start

position

AMP506_Command_Write(0x1d,0x00); // [7:0] of output V sync. pulse start position

AMP506_Command_Write(0x1e,0x00); // [7:4] Reserved [3:0] MSB of output V sync.

pulse width

AMP506_Command_Write(0x1f,0x08); // [7:0] LSB of output V sync. pulse width

AMP506_Command_Write(0x20,0x00); // [3:0] MSB of output DE vertical start position

AMP506_Command_Write(0x21,0x12); // [7:0] LSB of output DE vertical start position

AMP506_Command_Write(0x22,0x00); // [3:0] MSB of output DE vertical active region

in line

AMP506_Command_Write(0x23,0xf0); // [7:0] LSB of output DE vertical active region

in line

AMP506_Command_Write(0x24,0x01); // [7:4] Reversed [3:0] MSB of output V total in

line

AMP506_Command_Write(0x25,0x09); // [7:0] LSB of output V total in line

AMP506_Command_Write(0x26,0x00); // [17:16] bits of memory read start address

AMP506_Command_Write(0x27,0x00); // [7:0] [15:8] bits of memory read start address

AMP506_Command_Write(0x28,0x00); // [7:0] [7:0] bits of memory read start address

AMP506_Command_Write(0x29,0x01);

// [7:1] Reversed [0] Load output timing related setting (H sync., V sync. and DE) to take effect

AMP506_Command_Write(0x2d,0x08); /* [7:4] Reserved

[3] Output pin X_DCON level control

[2] Output clock inversion 0: Normal 1: Inverse

[1:0] Image rotate

00: 0° 01: 90° 10: 270° 11: 180°

*/

AMP506_Command_Write(0x30,0x00); // [7:4] Reserved [3:0] MSB of image horizontal shift

value

AMP506_Command_Write(0x31,0x00); // [7:0] LSB of image horizontal shift value

AMP506_Command_Write(0x32,0x00); // [7:4] Reserved [3:0] MSB of image vertical shift

value

AMP506_Command_Write(0x33,0x00); // [7:0] LSB of image vertical shift value

AMP506_Command_Write(0x34,0x01);

// [3:0] MSB of image horizontal physical Resolution in memory

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```
AMP506_Command_Write(0x35,0x40);
```

```
//[7:0] LSB of image horizontal physical resolution in memory
```

```
AMP506_Command_Write(0x36,0x01);
```

```
//[7:4] Reserved [3:0] MSB of image vertical physical resolution in memory
```

```
AMP506_Command_Write(0x37,0xe0);
```

```
//[7:0] LSB of image vertical physical resolution in memory
```

```
}
```

```
void AMP506_WindowSet(uint16 S_X,uint16 S_Y,uint16 E_X,uint16 E_Y)
```

```
{
```

```
    AMP506_80Mode_Command_SendAddress(0x00);
```

```
    AMP506_80Mode_Command_SendData((S_X)>>8);
```

```
    AMP506_80Mode_Command_SendData(S_X);
```

```
    AMP506_80Mode_Command_SendData((E_X-1)>>8);
```

```
    AMP506_80Mode_Command_SendData(E_X-1);
```

```
    AMP506_80Mode_Command_SendData(S_Y>>8);
```

```
    AMP506_80Mode_Command_SendData(S_Y);
```

```
    AMP506_80Mode_Command_SendData((E_Y-1)>>8);
```

```
    AMP506_80Mode_Command_SendData(E_Y-1);
```

```
}
```

```
void Full_386SCR(uint16 Dat16bit)
```

```
{
```

```
    int32 k,l;
```

```
    AMP506_WindowSet(0,0,Resolution_X,Resolution_Y);
```

```
    AMP506_80Mode_Command_SendAddress(0xc1); // _DisplayRAM_WriteEnable_
```

```
    for(k=0;k<240*2;k++)
```

```
    {
```

```
        for(l=0;l<320;l++)
```

```
        {
```

```
            AMP506_80Mode_16Bit_Memory_SendData(Dat16bit);
```

```
        }
```

```
    }
```

```
    AMP506_80Mode_Command_SendAddress(0x80); // DisplayRAM_WriteDisable _
```

```
}
```

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The TFT LCD controller default value is for AM320240N1 already. So we can start to write our data in a few steps:

Target: To write a 640x240 data to Display RAM and scroll the display data by change the Horizontal offset register.

10.1 Step 1: Make sure the interface Protocol.

10.2 Step 2: Define the Horizontal ram seize = 640 and Vertical ram size =240
640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 ,

REG[37]=0xF0

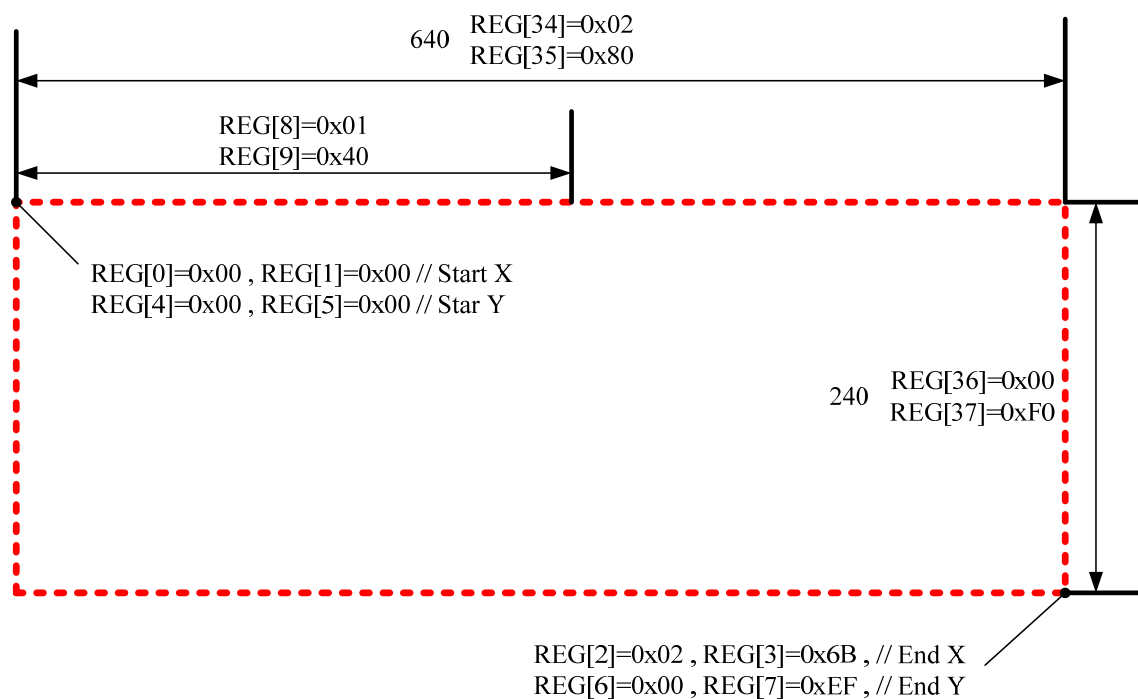
10.3 Step 3: Define the Panel X Size = 320

REG[8]=0x01 , REG[9]=0x40

10.4 Step4: Define the Write window. Start=(0,0) End=(619,239)

REG[0]=0x00 , REG[1]=0x00 , REG[2]=0x02 , REG[3]=0x6B , // Start X , End X

REG[4]=0x00 , REG[5]=0x00 , REG[6]=0x00 , REG[7]=0xEF , // Star Y ,End Y



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10.5 Step5: Write the 640x240x18 bit data consecutively



10.6 Step6: The display will show the following image.



10.7 Step7: Change the Horizontal offset to switch or scroll the display data.

Set the Horizontal offset = 160 , REG[30]=00 REG[31]=A0 . You will see



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10.8 Step8: Change the Horizontal offset to switch or scroll the display data.

































Set the Horizontal offset = 320 , REG[30]=01 REG[31]=40 . You will see



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DISPLAYED COLOR AND INPUT DATA

| | | Color & Gray Scale | DATA SIGNAL | | | | | | | | | | | | | | | | | |
|-------------|---|--------------------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Color |  | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Red(0) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Green(0) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Blue(0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| |  | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| |  | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| |  | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Red |  | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Red(62) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Red(61) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Red(31) | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Red(1) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Red(0) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Green |  | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Green(62) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Green(61) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Green(31) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Green(1) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Green(0) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Blue |  | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| |  | Blue(62) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| |  | Blue(61) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Blue(31) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| |  | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| |  | Blue(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| |  | Blue(0) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

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11 QUALITY AND RELIABILITY

11.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $60 \pm 25\% \text{ RH}$.

11.2 SAMPLING PLAN

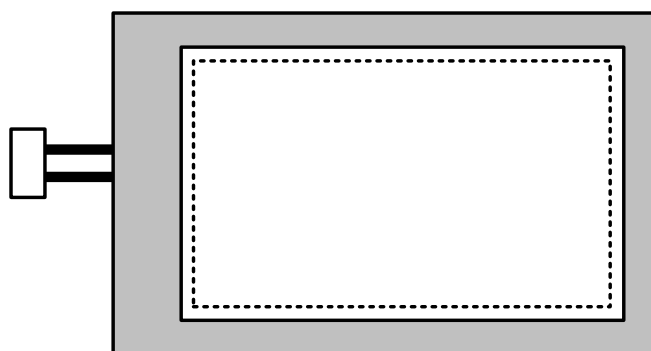
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .


11.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

11.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



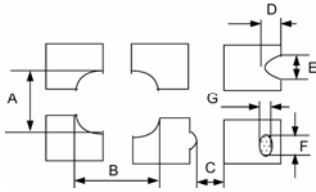
 Zone A (Active Area)

 Zone B (Viewing Area)

Preliminary

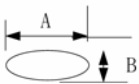
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11.5 INSPECTION QUALITY CRITERIA

| No. | Item | Criterion for defects | Defect type | | | | | | | | | | | | | | | |
|---------------------------|------------------------|---|---------------------------|-------------------|---------------------------|---------------------------|----------------------|---|----------------------|----------------------|------------|--------------------|----------------------|---|--------------|----------------------|---|-------|
| 1 | Non display | No non display is allowed | Major | | | | | | | | | | | | | | | |
| 2 | Irregular operation | No irregular operation is allowed | Major | | | | | | | | | | | | | | | |
| 3 | Short | No short are allowed | Major | | | | | | | | | | | | | | | |
| 4 | Open | Any segments or common patterns that don't activate are rejectable. | Major | | | | | | | | | | | | | | | |
| 5 | Black/White spot (I) | <table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>$D \leq 0.15$</td><td>Ignore</td></tr><tr><td>$0.15 < D \leq 0.20$</td><td>3</td></tr><tr><td>$0.20 < D \leq 0.30$</td><td>2</td></tr><tr><td>$0.30 < D$</td><td>0</td></tr></table> | Size D (mm) | Acceptable number | $D \leq 0.15$ | Ignore | $0.15 < D \leq 0.20$ | 3 | $0.20 < D \leq 0.30$ | 2 | $0.30 < D$ | 0 | Minor | | | | | |
| Size D (mm) | Acceptable number | | | | | | | | | | | | | | | | | |
| $D \leq 0.15$ | Ignore | | | | | | | | | | | | | | | | | |
| $0.15 < D \leq 0.20$ | 3 | | | | | | | | | | | | | | | | | |
| $0.20 < D \leq 0.30$ | 2 | | | | | | | | | | | | | | | | | |
| $0.30 < D$ | 0 | | | | | | | | | | | | | | | | | |
| 6 | Black/White line (I) | <table><tr><th>Length(mm)</th><th></th><th>Acceptable number</th></tr><tr><td>$10 < L$</td><td>$0.03 < W \leq 0.04$</td><td>5</td></tr><tr><td>$5.0 < L \leq 10$</td><td>$0.04 < W \leq 0.06$</td><td>3</td></tr><tr><td>$1.0 < L \leq 5.0$</td><td>$0.06 < W \leq 0.07$</td><td>2</td></tr><tr><td>$L \leq 1.0$</td><td>$0.07 < W \leq 0.09$</td><td>1</td></tr></table> | Length(mm) | | Acceptable number | $10 < L$ | $0.03 < W \leq 0.04$ | 5 | $5.0 < L \leq 10$ | $0.04 < W \leq 0.06$ | 3 | $1.0 < L \leq 5.0$ | $0.06 < W \leq 0.07$ | 2 | $L \leq 1.0$ | $0.07 < W \leq 0.09$ | 1 | Minor |
| Length(mm) | | Acceptable number | | | | | | | | | | | | | | | | |
| $10 < L$ | $0.03 < W \leq 0.04$ | 5 | | | | | | | | | | | | | | | | |
| $5.0 < L \leq 10$ | $0.04 < W \leq 0.06$ | 3 | | | | | | | | | | | | | | | | |
| $1.0 < L \leq 5.0$ | $0.06 < W \leq 0.07$ | 2 | | | | | | | | | | | | | | | | |
| $L \leq 1.0$ | $0.07 < W \leq 0.09$ | 1 | | | | | | | | | | | | | | | | |
| 7 | Black/White sport (II) | <table><tr><th>Size D (mm)</th><th>Acceptable number</th></tr><tr><td>$D \leq 0.30$</td><td>Ignore</td></tr><tr><td>$0.30 < D \leq 0.50$</td><td>5</td></tr><tr><td>$0.50 < D \leq 1.20$</td><td>3</td></tr><tr><td>$1.20 < D$</td><td>0</td></tr></table> | Size D (mm) | Acceptable number | $D \leq 0.30$ | Ignore | $0.30 < D \leq 0.50$ | 5 | $0.50 < D \leq 1.20$ | 3 | $1.20 < D$ | 0 | Minor | | | | | |
| Size D (mm) | Acceptable number | | | | | | | | | | | | | | | | | |
| $D \leq 0.30$ | Ignore | | | | | | | | | | | | | | | | | |
| $0.30 < D \leq 0.50$ | 5 | | | | | | | | | | | | | | | | | |
| $0.50 < D \leq 1.20$ | 3 | | | | | | | | | | | | | | | | | |
| $1.20 < D$ | 0 | | | | | | | | | | | | | | | | | |
| 8 | Black/White line (II) | <table><tr><th>Length (mm)</th><th>Width (mm)</th><th>Acceptable number</th></tr><tr><td>$20 < L$</td><td>$0.05 < W \leq 0.07$</td><td>5</td></tr><tr><td>$10 < L \leq 20$</td><td>$0.07 < W \leq 0.09$</td><td>3</td></tr><tr><td>$5.0 < L \leq 10$</td><td>$0.09 < W \leq 0.10$</td><td>2</td></tr><tr><td>$L \leq 5.0$</td><td>$0.10 < W \leq 0.15$</td><td>1</td></tr></table> | Length (mm) | Width (mm) | Acceptable number | $20 < L$ | $0.05 < W \leq 0.07$ | 5 | $10 < L \leq 20$ | $0.07 < W \leq 0.09$ | 3 | $5.0 < L \leq 10$ | $0.09 < W \leq 0.10$ | 2 | $L \leq 5.0$ | $0.10 < W \leq 0.15$ | 1 | Minor |
| Length (mm) | Width (mm) | Acceptable number | | | | | | | | | | | | | | | | |
| $20 < L$ | $0.05 < W \leq 0.07$ | 5 | | | | | | | | | | | | | | | | |
| $10 < L \leq 20$ | $0.07 < W \leq 0.09$ | 3 | | | | | | | | | | | | | | | | |
| $5.0 < L \leq 10$ | $0.09 < W \leq 0.10$ | 2 | | | | | | | | | | | | | | | | |
| $L \leq 5.0$ | $0.10 < W \leq 0.15$ | 1 | | | | | | | | | | | | | | | | |
| 9 | Back Light | 1. No Lighting is rejectable 2. Flickering and abnormal lighting are rejectable | Major | | | | | | | | | | | | | | | |
| 10 | Display pattern | <div><p>Unit:mm</p><table><tr><td>$\frac{A+B}{2} \leq 0.30$</td><td>$0 < C$</td><td>$\frac{D+E}{2} \leq 0.25$</td><td>$\frac{F+G}{2} \leq 0.25$</td></tr></table><p>Note: 1. Acceptable up to 3 damages 2. NG if there're to two or more pinholes per dot</p></div> | $\frac{A+B}{2} \leq 0.30$ | $0 < C$ | $\frac{D+E}{2} \leq 0.25$ | $\frac{F+G}{2} \leq 0.25$ | Minor | | | | | | | | | | | |
| $\frac{A+B}{2} \leq 0.30$ | $0 < C$ | $\frac{D+E}{2} \leq 0.25$ | $\frac{F+G}{2} \leq 0.25$ | | | | | | | | | | | | | | | |

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| | | | | | | | |
|----|---|--|--|-------------------|--------------|-------------------------|-------|
| 11 | Blemish & Foreign matters Size: $D = \frac{A+B}{2}$ | Size D (mm) | | Acceptable number | Minor | | |
| | | $D \leq 0.15$ | | Ignore | | | |
| | | $0.15 < D \leq 0.20$ | | 3 | | | |
| | | $0.20 < D \leq 0.30$ | | 2 | | | |
| | | $0.30 < D$ | | 0 | | | |
| 12 | Scratch on Polarizer  | Width (mm) | | | Length (mm) | Acceptable number | Minor |
| | | $W \leq 0.0$ | | | Ignore | Ignore | |
| | | 3 | | | $L \leq 2.0$ | Ignore | |
| | | $0.03 < W \leq 0.05$ | | | $L > 2.0$ | 1 | |
| | | $0.05 < W \leq 0.08$ | | | $L > 1.0$ | 1 | |
| | | $0.08 < W$ | | | $L \leq 1.0$ | Ignore | |
| | | Note(1) Regard as a blemish | | | Note(1) | Note(1) | |
| 13 | Bubble in polarizer | Size D (mm) | | Acceptable number | Minor | | |
| | | $D \leq 0.20$ | | Ignore | | | |
| | | $0.20 < D \leq 0.50$ | | 3 | | | |
| | | $0.50 < D \leq 0.80$ | | 2 | | | |
| | | $0.80 < D$ | | 0 | | | |
| 14 | Stains on LCD panel surface | Stains that cannot be removed even when wiped lightly with a soft cloth or similar cleaning too are rejectable. | | | | Minor | |
| 15 | Rust in Bezel | Rust which is visible in the bezel is rejectable. | | | | Minor | |
| 16 | Defect of land surface contact (poor soldering) | Evident crevices which is visible are rejectable. | | | | Minor | |
| 17 | Parts mounting | 1. Failure to mount parts 2. Parts not in the specifications are mounted 3. Polarity, for example, is reversed | | | | Major Major Major | |
| 18 | Parts alignment | 1. LSI, IC lead width is more than 50% beyond pad outline. | | | | Minor | |
| | | 2. Chip component is off center and more than 50% of the leads is off the pad outline. | | | | Minor | |
| 19 | Conductive foreign matter (Solder ball, Solder chips) | 1. $0.45 < \phi$, $N \geq 1$ | | | | Major | |
| | | 2. $0.30 < \phi \leq 0.45$, $N \geq 1$ ϕ :Average diameter of solder ball (unit: mm) | | | | Minor | |
| | | 3. $0.50 < L$, $N \geq 1$ L : Average length of solder chip (unit: mm) | | | | Minor | |
| 20 | Faulty PCB correction | 1. Due to PCB copper foil pattern burnout, the pattern is connected, using a jumper wire for repair; 2 or more places are corrected per PCB. | | | | Minor | |
| | | 2. Short circuited part is cut, and no resist coating has been performed. | | | | Minor | |

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| | | | | | | |
|----|------------|--|----------|-----------|------------------------------|-------|
| 21 | Defect Dot | The TFT panel may have bright dot or Dark dot. The acceptable number defection: | | | | Minor |
| | | Bright dot | Dark dot | Total dot | Distance between Dark-- dark | |
| | | 2 | 3 | 4 | $L \geq 5 \text{ mm}$ | |

12 Reliability test items (Note2):

| No. | Test items | Conditions | Remark |
|-----|------------------------------------|--|--------------------------------|
| 1 | High temperature storage | Ta=80℃ 240Hrs | |
| 2 | Low temperature storage | Ta=-30℃ 240Hrs | |
| 3 | High temperature operation | Ta=70℃ 240Hrs | |
| 4 | Low temperature operation | Ta=-20℃ 240Hrs | |
| 5 | High temperature and high humidity | Ta=40℃,85% RH 240Hrs | Operation |
| 6 | Heat shock | -30℃~80℃/200 cycles 1Hrs/cycle | Non-operation |
| 7 | Electrostatic discharge | ±200V,200Pf(0Ω),once for each terminal | Non-operation |
| 8 | Vibration | Frequency range :8~33.3Hz Stoke :1.3mm Sweep :2.9G,33.3~400Hz Cycle :15 minutes 2 hours for each direction of X,Z 4 hours for Y direction | JIS C7021, A-10 Condition A |
| 9 | Mechanical shock | 100G, 6ms,±X, ±Y,±Z 3 times for each direction | JIS C7021, A-7 Condition C |
| 10 | Vibration (With carton) | Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/octave from 200~500Hz | IEC 68~34 |
| 11 | Drop (with carton) | Height:60cm 1 corner,3 edges,6 surfaces | JIS Z0202 |

13 USE PRECAUTIONS

13.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

13.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1\text{M}\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

13.3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.

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- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

13.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

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13.5 Other

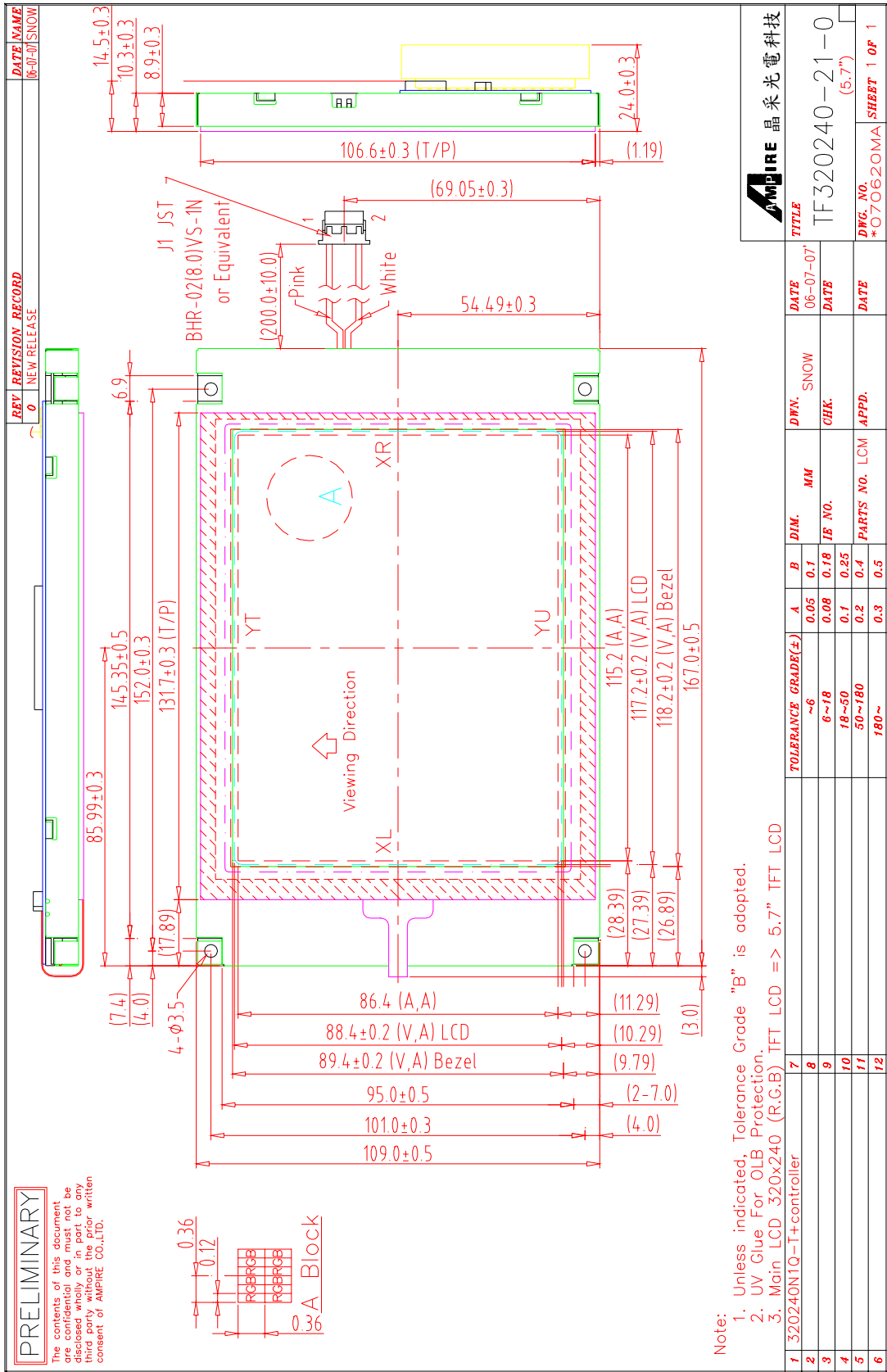
- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

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14 OUTLINE DIMENSION

14.1 OUTLINE DIMENSION-1 (With FFC P1.0x24 pins)



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