



A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

7.0-IN ANALOG TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A M 4 8 0 2 3 4 G T M C W - 0 0
APPROVED BY:	
DATE:	

☐

APPROVED FOR SPECIFICATIONS

☐

APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

9856 SIXTH STREET RANCHO CUCAMONGA CA 91730
TEL: 909-980-13410 FAX: 909-980-1419
WWW.AMPDISPLAY.COM

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2007/6/15	-	New Release	Donlin

1 Features

Ampire 7 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module for video equipments. This module is composed of a 7" TFT-LCD panel, a driver circuit and backlight unit.

- (1) Construction: 7" a-Si color TFT-LCD, White CCFL Backlight and PCB.
- (2) Resolution (pixel): 480(R.G.B) X234

2 Physical specifications

Item	Specifications	Unit	
Display resolution(dot)	1440 (W) x 234(H)	mm	
Active area	154.08 (W) x 86.58 (H)	mm	
Screen size	7.0(Diagonal)	mm	
Dot pitch	0.107 (W) x 0.370 (H)	mm	
Color configuration	R.G.B stripe		
Overall dimension	164.9(W)x100.0(H)x5.7(D)	mm	
Weight	180	g	
Backlight unit	CCFL		

3 Electrical specification

3.1 Absolute max. ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V _{CC}	GND=0	-0.3	7	V	
	AV _{DD}	AV _{SS} =0	-0.3	7	V	
	V _{GH}	GND=0	-0.3	18	V	
	V _{GL}		-15	0.3	V	
	V _{GH} -V _{GL}		-	33	V	
Input signal voltage	V _i		-0.3	AV _{DD} +0.3	V	Note 1
	V ₁		-0.3	V _{CC} +0.3	V	Note 2
	V _{COM}		-2.9	5.2	V	

Note1:VR,VG,VB

Note2:STHL,STHR,OEHL,L/R,CPH1~CPH3,STVL,OEVL,CKV,U/D.

3.2 Electrical characteristics

a. Typical operating conditions (GND=AVss=0V, Note 4)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V _{CC}	3	5	5.2	V	
		AV _{DD}	4.8	5	5.2	V	
		V _{GH}	14.3	15	15.7	V	
		V _{GL}	-10.5	-10	-9.5	V	
Video signal Amplitude (VR, VG, VB)		V _{iA}	0.4	-	AV _{DD} -0.4	V	Note 1
		V _{iAC}	-	3	-	V	AC component
		V _{iDC}	-	AV _{DD} /2	-	V	DC component
VCOM		V _{CAC}	3.5	5.6	6.5	Vp-p	AC component, Note 2
		V _{CDC}	1.4	1.7	2.0	V	DC component
Input Signal voltage	H Level	V _{IH}	0.8 V _{CC}	-	V _{CC}	V	Note 3
	L Level	V _{IL}	0	-	0.2 V _{CC}	V	

Note1: Refer to Fig.2

Note2: The brightness of LCD panel could be changed by adjusting the AC component of VCOM.

Note3: STHL, STHR, OEHL, L/R, CPH1~CPH3, STVR, STVL, OEVL, CKV, U/D

Note4: Be sure to apply GND, V_{CC} and V_{GL} to the LCD first, and then apply V_{GH}.

display horizontal synchronous signal to avoid interference.

Note 5:For starting the backlight unit, the output voltage of DC/AC's transformer
Should be larger than the maximum lamp starting voltage.

Note 6:The “ Lamp life time” is defined as the module brightness decrease to 50%
Original brightness at Ta=25℃, IL=6mA.

3.3 AC Timing

a. Timing condition

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
High tans low level pulse width	t_{CPH}	99	103	107	ns	CPH1~CPH3
CPH pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3
CPH pulse delay	t_{C12} t_{C23} t_{C31}	30	$t_{CPH}/3$	$t_{CPH}/2$	ns	CPH1~CPH3
STH setup time	t_{SUH}	20	-	-	ns	STHR,STHL
STH hold time	t_{HDH}	20	-	-	ns	STHR,STHL
STH pulse width	t_{STH}	-	1	-	t_{CPH}	STHR,STHL
STH period	t_H	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t_{OEH}	-	1.22	-	μs	OEH
Sample and hold disable time	t_{DIS1}	-	8.28	-	μs	
OEV pulse width	t_{OEV}	-	5.40	-	μs	OEV
CKV pulse width	t_{CKV}	-	4.18	-	μs	CKV
Clean enable time	t_{DIS2}	-	3.74	-	μs	
Horizontal display start	t_{SH}	-	0	-	$T_{CPH}/3$	
Horizontal display timing range	t_{DH}	-	1440	-	$T_{CPH}/3$	
STV setup time	t_{SUV}	400	-	-	ns	STVL,STVR
STV hold time	t_{HDV}	400	-	-	ns	STVL,STVR
STV pulse width	t_{STV}	-	-	1	t_H	STVL,STVR
Horizontal lines per field	t_V	256	262	268	t_H	Note 2
Vertical display start	t_{SV}		3	-	t_H	
Vertical display timing range	t_{DV}		234	-	t_H	
VCOM rising time	t_{rCOM}		-	5	μs	
VCOM falling time	t_{fCOM}		-	5	μs	
VCOM delay time	t_{DCOM}		-	3	μs	
RGB delay time.	t_{DCOM}		-	1	μs	

Note 1:For all of the logic signals.

Note 2:Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously.

b. Timing diagram

Please refer to the attached drawing,from Fig.3 to Fig.7

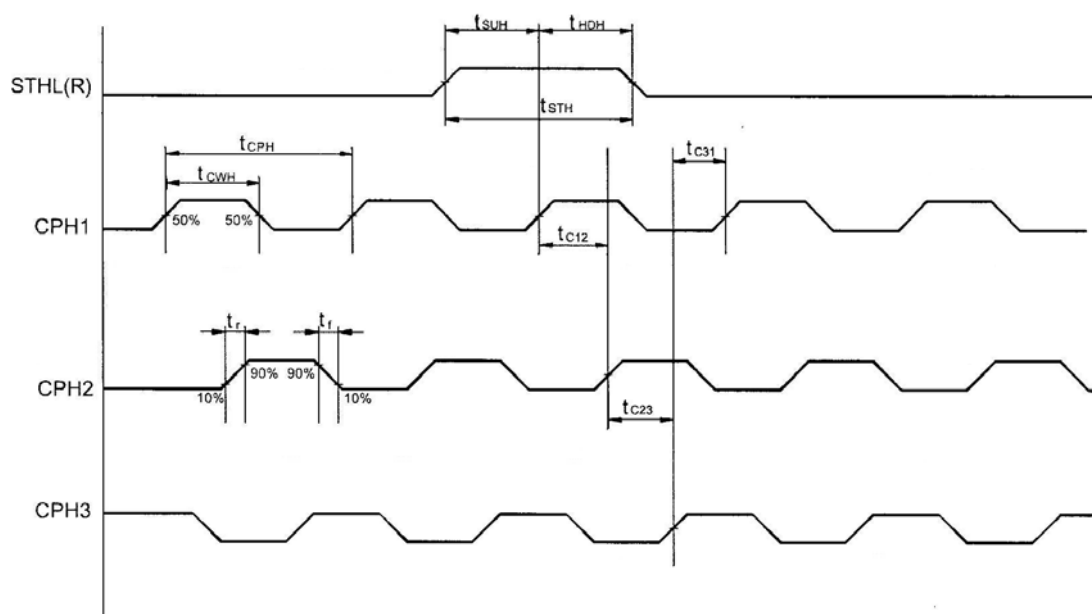


Fig.3 Sampling clock timing

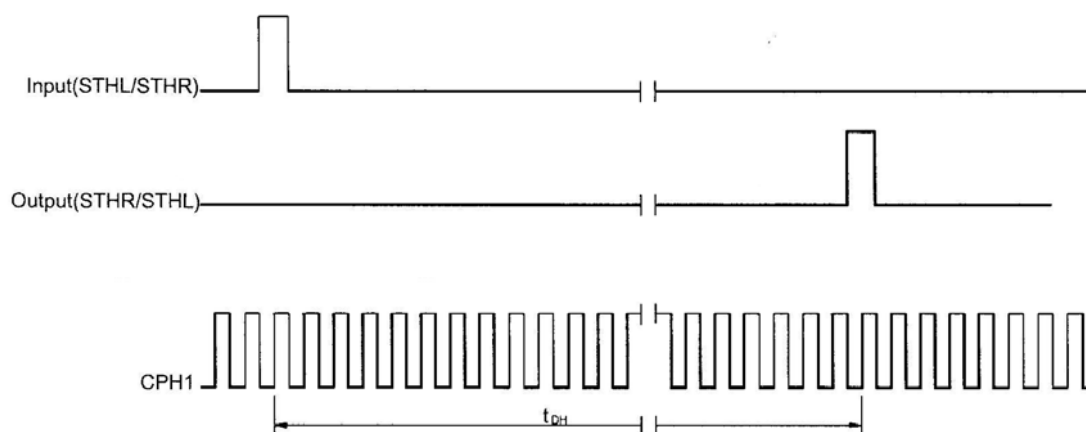


Fig.4 Horizontal display timing rage

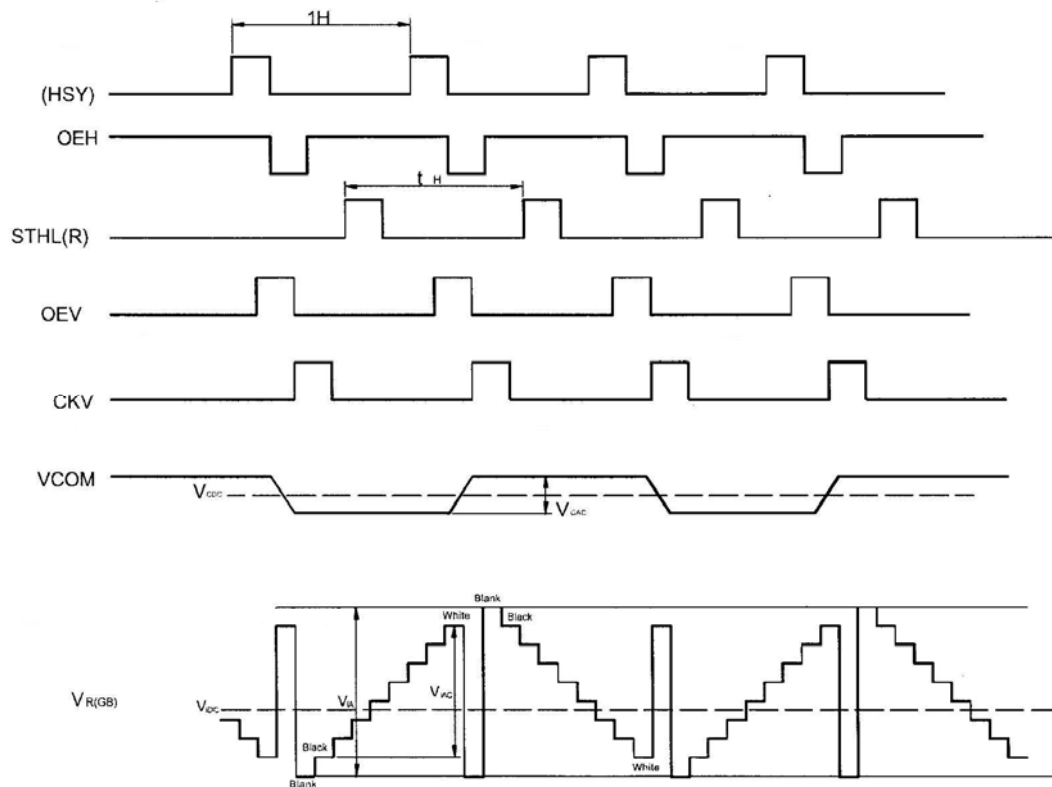


Fig.5 Horizontal timing

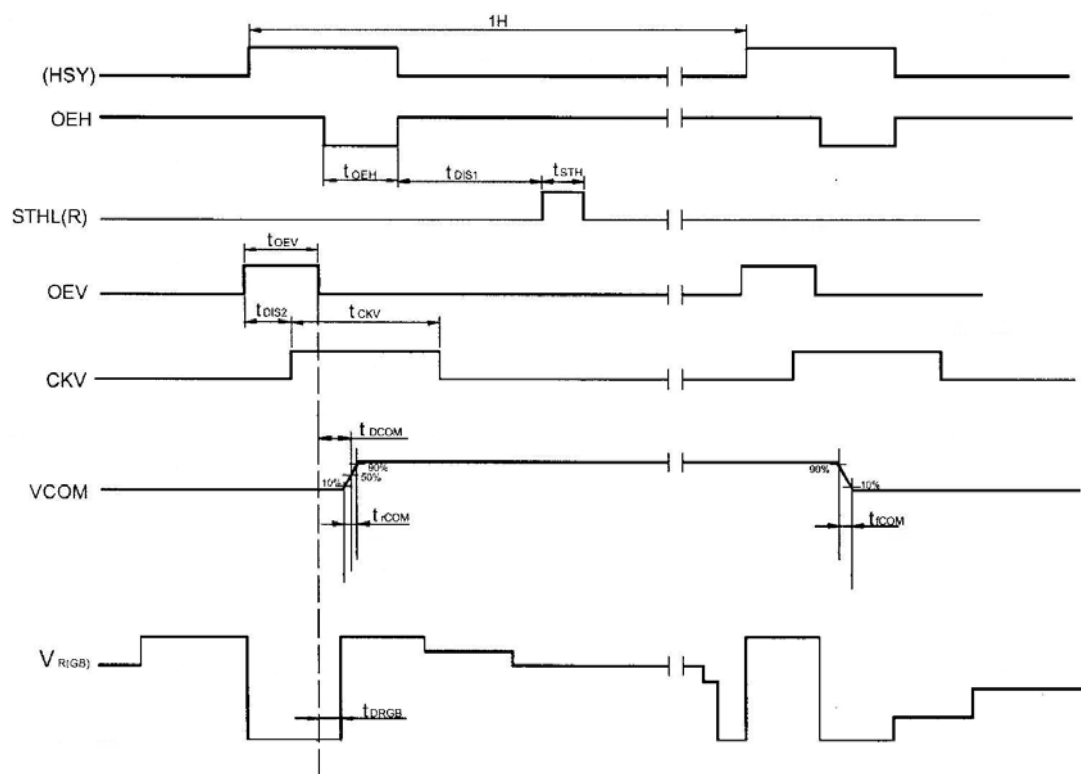


Fig.6 Detail horizontal timing

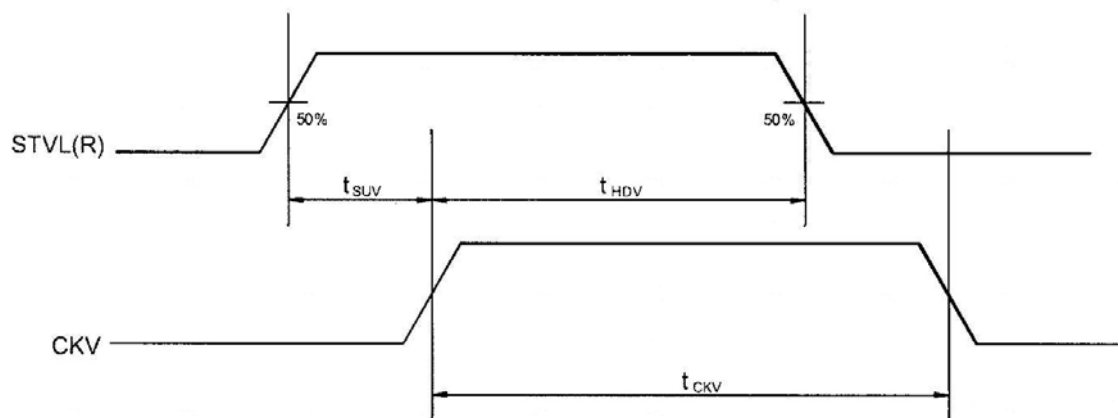


Fig.7 Vertical shift clock timing

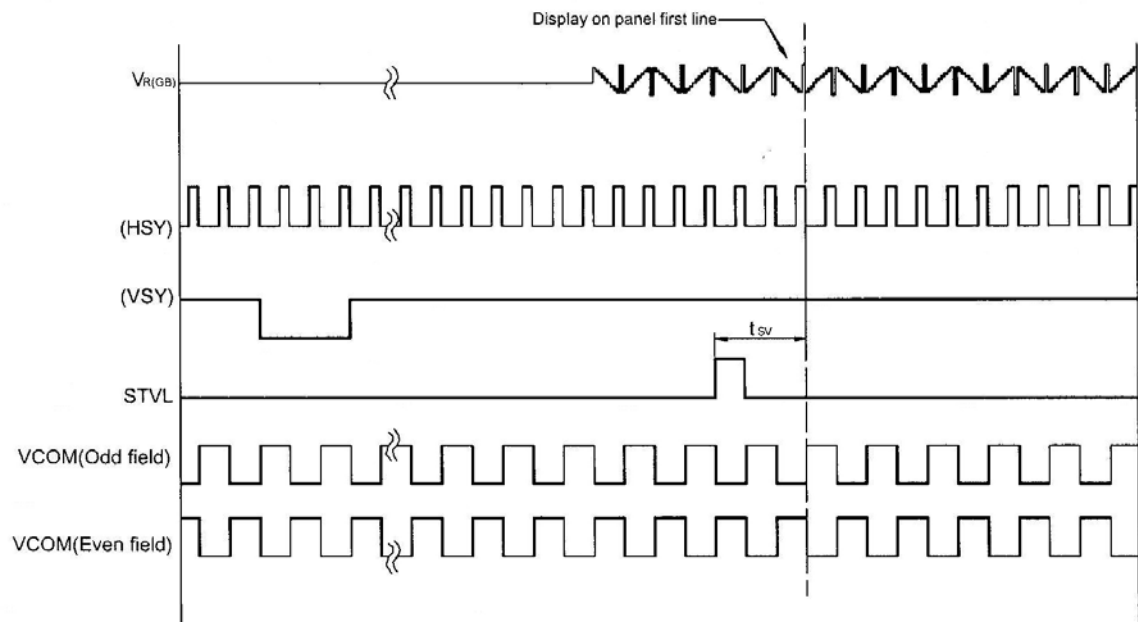


Fig.8 Vertical timing(From up to down)

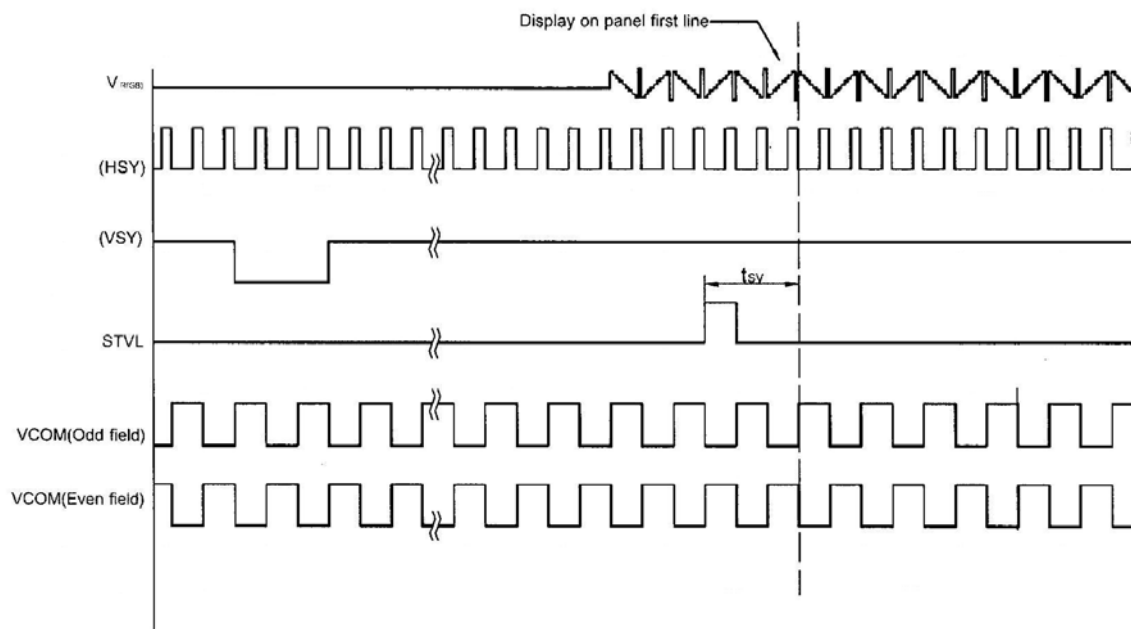
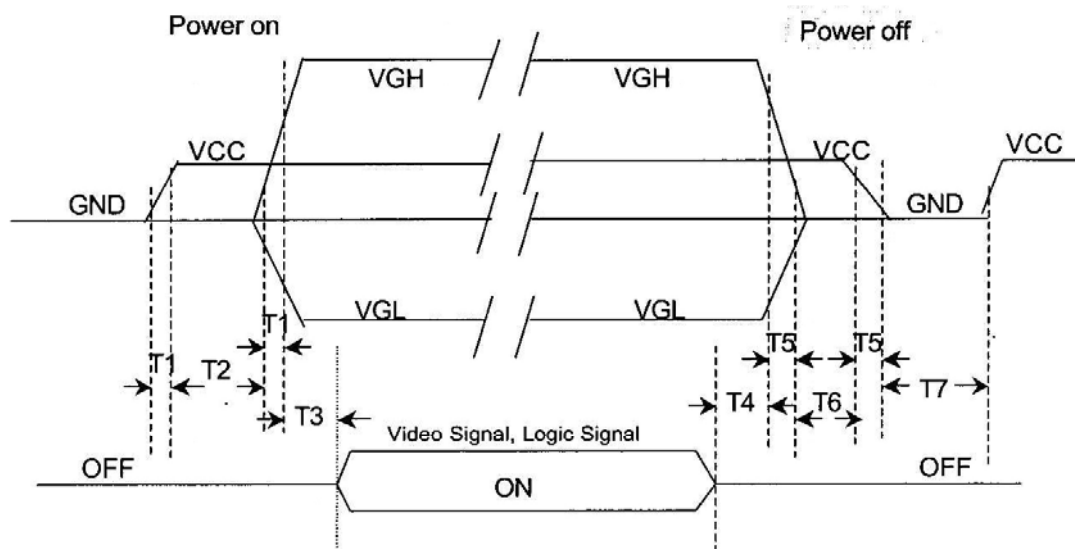


Fig.9 Horizontal timing(From down to up)

3.4 Power Sequence

Sequence for power on/off and signal on/off



- T1 \leq 15ms (From 10%*VCC to 90%*VCC , when VCC is Low to High) ;
- T2 \leq 10ms (From 90%*VCC to 10%*VGH , when VCC is Low to High) ;
- T3 \leq 10ms (From 90%*VGH to Video signal , when VGH is Low to High) ;
- T4 \leq 10ms (From Video signal to 90%*VGH , when VGH is High to Low) ;
- T5 \leq 20ms (From 90%*VCC to 10%*VCC , when VCC is High to Low) ;
- T6 \leq 10ms (From 10%*VGH to 90%*VCC , when VCC is Low to High) ;
- T7 \geq 0.4s (From 10%*VCC is H→L to 10%*VCC is L→H) .

4 Optical specification(Note1,Note2)

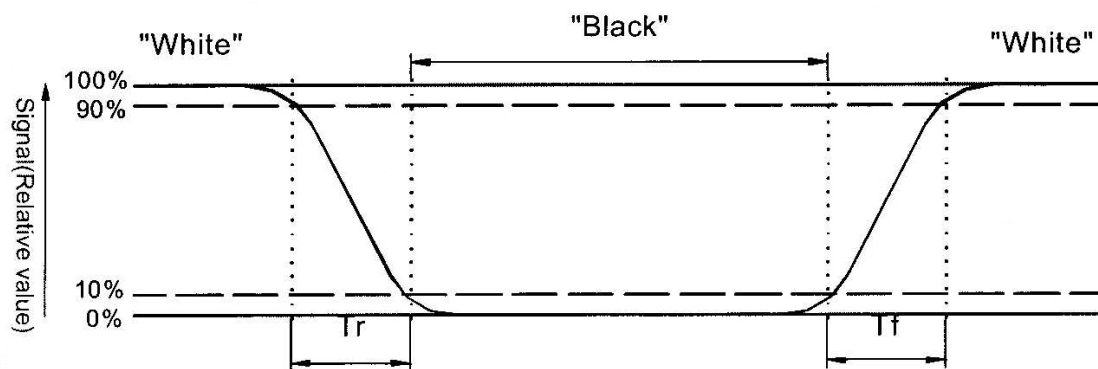
Item		Symbol	Conditon	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	T_r	$\Theta=0^\circ$	-	15		ms	Note 3,5
	Fall	T_f		-	35		ms	
Contrast ratio		CR	At optimized viewing angle	150	250	-		Note 4,5
Viewing angle	Top	$CR \geq 10$			35	-	deg.	Note 5,6
	Bottom				55	-		
	Left				70	-		
	Right				70	-		
Brightness		Y_L	$I_L=6mA, 25^\circ C$	-	250		cd/m ²	Note 7
White chromaticity		X	$\Theta=0^\circ$		0.31			Note 7
		Y	$\Theta=0^\circ$		0.33			

Note 1: Ambient temperature=25°C, and lamp current $I_L=6$ mArms. To be measured in the dark room.

Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black” (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector Output when LCD is at "Black" state}}$$

Note 5: White $V_i = V_{i50} + 1.5V$

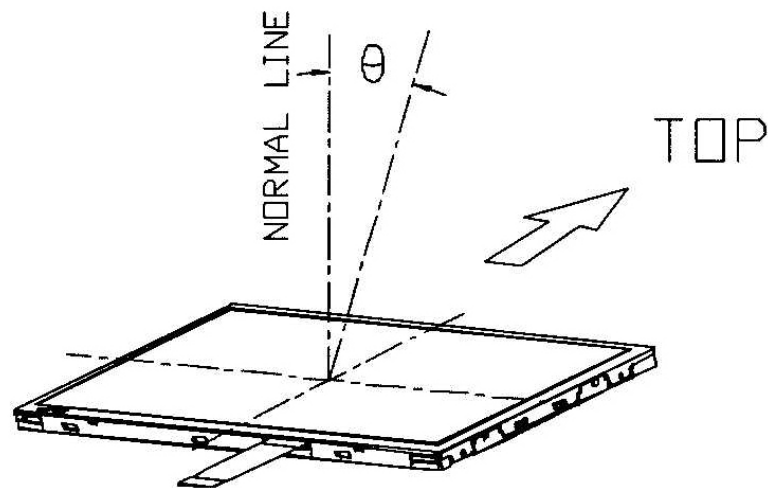
Black $V_i = V_{i50} + 2.0V$

“ \pm ” means that the analog input signal swings in phase with V_{COM} signal.

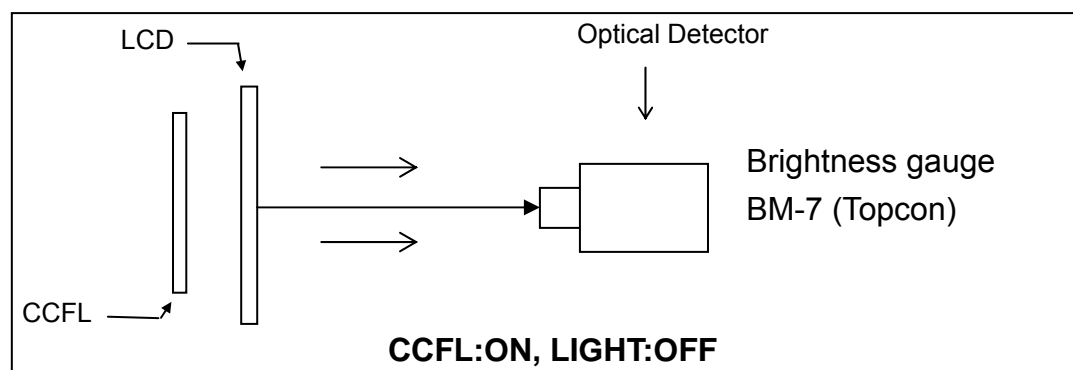
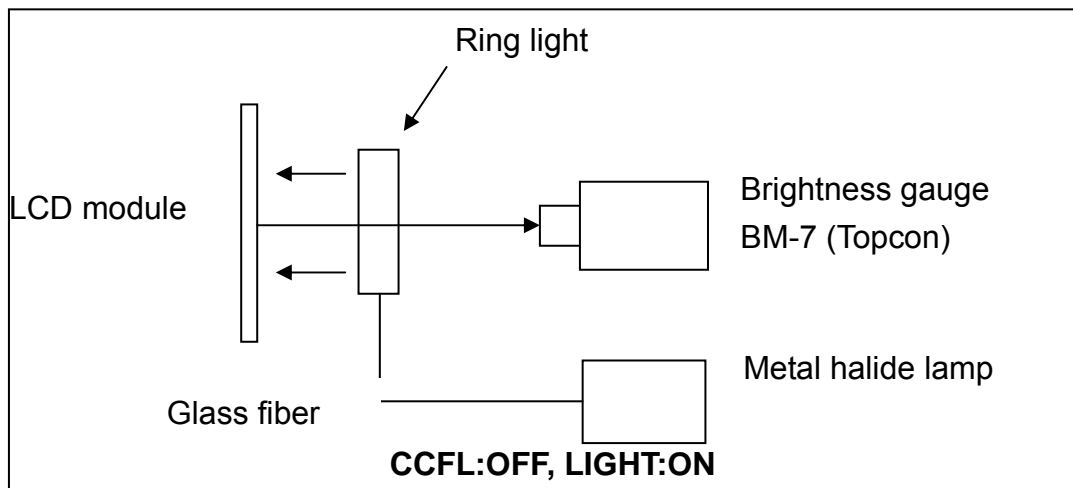
“ $\frac{-}{+}$ ” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} : The analog input voltage when transmission is 50%. The 100% Transmission is defined as the transmission of LCD panel when all the Input terminals of module are electrically opened.

Note 6. Definition of viewing angle, Refer to figure as below.



Note 7. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



5 Interface specifications

a.TFT –LCD panel driving section

Pin no	Symbol	I/O	Description	Remark
1	GND	-	Ground for logic circuit	
2	V _{CC}	I	Supply voltage of logic control circuit for scan drive	
3	V _{GL}	I	Negative power for scan driver	
4	V _{GH}	I	Positive power for scan driver	
5	STVR	I/O	Vertical start pulse	Note 1
6	STVL	I/O	Vertical start pulse	Note 1
7	CKV	I	Shift clock input for scan driver	
8	U/D	I	UP/DOWN scan control input	Note 1,2
9	OE _V	I	Output enable input for scan driver	
10	VCOM	I	Common electrode driving signal	
11	VCOM	I	Common electrode driving signal	
12	L/R	I	LEFT/RIGHT scan control input	Note 1,2
13	MOD	I	Sequential sampling and simultaneous sampling setting	Note 3
14	OE _H	I	Output enable input for data driver	
15	STHL	I/O	Start pulse for horizontal scan line	Note 1
16	STHR	I/O	Start pulse for horizontal scan line	Note 1
17	CPH3	I	Sampling and shifting clock pulse for data driver	
18	CPH2	I	Sampling and shifting clock pulse for data driver	
19	CPH1	I	Sampling and shifting clock pulse for data driver	
20	V _{CC}	I	Supply voltage of logic control circuit for data driver	
21	GND	-	Ground fo logic circuit	
22	VR	I	Altemated video signal input(Red)	
23	VG	I	Altemated video signal input(Green)	
24	VB	I	Altemated video signal input(Blue)	
25	AV _{DD}	I	Supply voltage for analog circuit	
26	AV _{SS}	-	Ground for analog circuit	

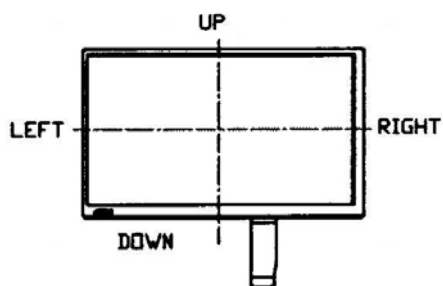
Note 1: Selection of scanning mode(please refer to the following table)

Setting of scan Control input		IN/OUT state for start pulse				Scanning direction
U/D	L/R	STVR	STVL	STHR	STHL	
GND	V _{CC}	OUT	IN	OUT	IN	From up to down,and from left to right
V _{CC}	GND	IN	OUT	IN	OUT	From down to up,and from right to left
GND	GND	OUT	IN	IN	OUT	From up to down,and from right to left
V _{CC}	V _{CC}	IN	OUT	OUT	IN	From down to up,and from left to right

IN: Input; OUT: output

Note 2:Definition of scanning direction.

Refer to figure as below:



Note 3:MOD = H:Simultaneous sampling.

MOD = L:Sequential sampling.

Please set CPH2 and CPH3 to GND when MOD =H

b.Backlight driving section

No.	Symbol	I/O	Description	Remark
1	HI	I	Power supply for backlight unit(High voltage)	-
2	GND	-	Ground for backlight unit	-

6 QUALITY AND RELIABILITY

6.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $60 \pm 25\% \text{ RH}$.

6.2 SAMPLING PLAN

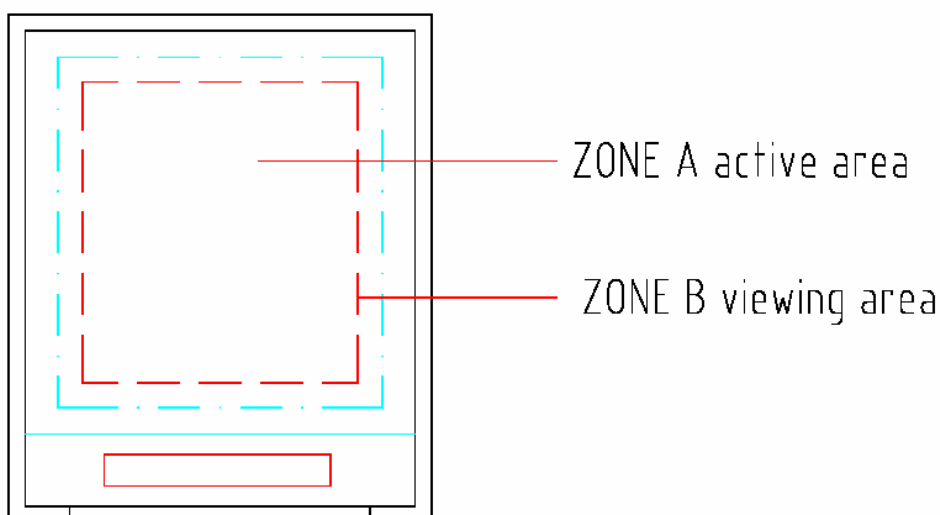
Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

6.3 ACCEPTABLE QUALITY LEVEL

A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

6.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.



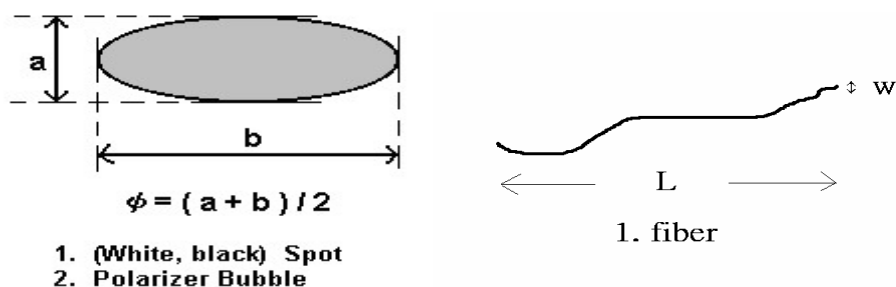
6.5 INSPECTION QUALITY CRITERIA

DEFECT TYPE			LIMIT				Note		
VISUAL DEFECT	INTERNAL	SPOT	$\varphi < 0.15\text{mm}$		Ignore		Note1		
			$0.15\text{mm} \leq \varphi \leq 0.5\text{mm}$		$N \leq 4$				
			$0.5\text{mm} < \varphi$		$N = 0$				
		FIBER	$W \leq 0.1\text{mm}, L \leq 5\text{mm}$		$N \leq 3$		Note1		
			$1.0\text{mm} < W, 1.5\text{mm} < L$		$N = 0$				
		POLARIZER BUBBLE	$\varphi < 0.25\text{mm}$		Ignore		Note1		
			$0.25\text{mm} \leq \varphi \leq 0.5\text{mm}$		$N \leq 2$				
			$0.5\text{mm} < \varphi$		$N = 0$				
		Mura	It' OK if mura is slight visible through 6%ND filter						
ELECTRICAL DEFECT	BRIGHT DOT		A Grade			B Grade			
			C Area	O Area	Total	C Area	O Area	Total	Note3
			$N \leq 0$	$N \leq 2$	$N \leq 2$	$N \leq 2$	$N \leq 3$	$N \leq 5$	Note2
	DARK DOT		$N \leq 2$	$N \leq 3$	$N \leq 3$	$N \leq 3$	$N \leq 5$	$N \leq 8$	
	TOTAL DOT		$N \leq 2$	$N \leq 4$	$N \leq 4$	$N \leq 5$	$N \leq 6$	$N \leq 8$	Note2
	TWO ADJACENT DOT		$N \leq 0$	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	$N \leq 1$ pair	Note4
	THREE OR MORE ADJACENT DOT		NOT ALLOWED						
	LINE DEFECT		NOT ALLOWED						

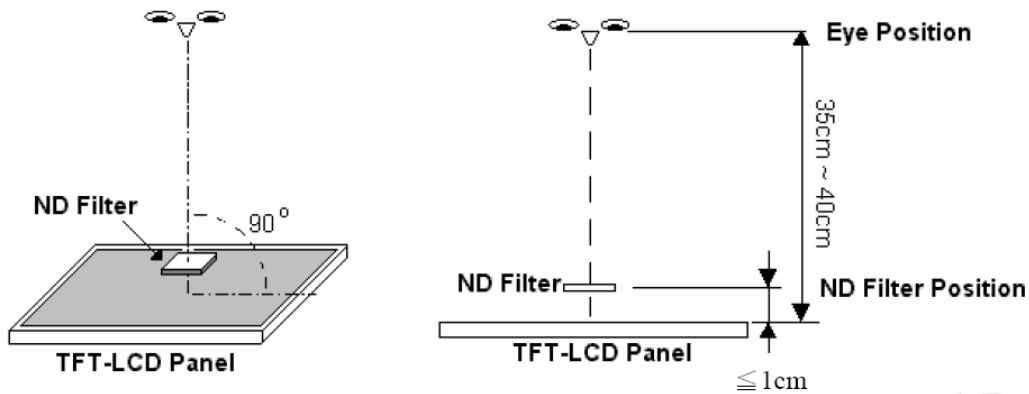
(1) One pixel consists of 3 sub-pixels, including R,G, and B dot.(Sub-pixel = Dot)

(2) **LITTLE BRIGHT DOT $N \leq 10$ at 5% ND-Filter**

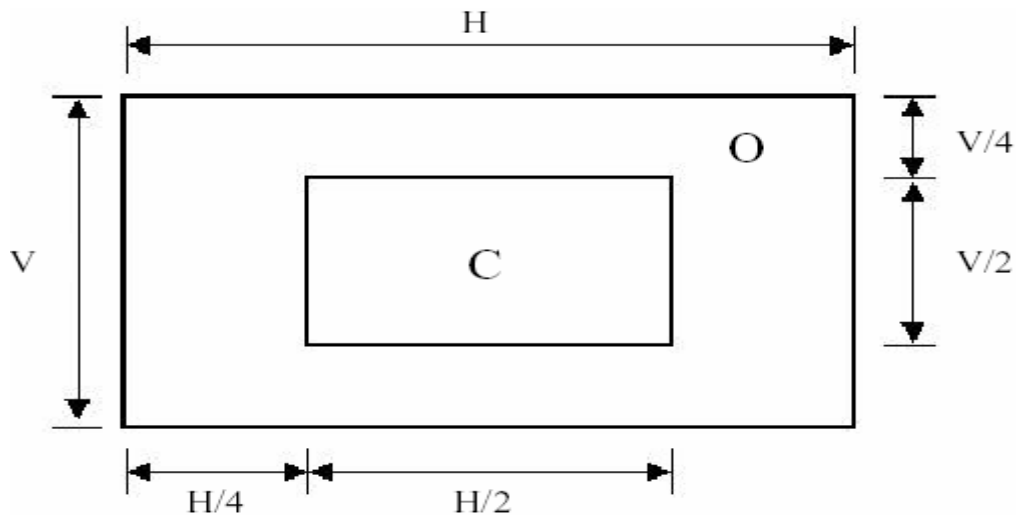
[Note1] W : Width[mm], L : Length[mm], N : Number, φ : Average Diameter



[Note2] Bright dot is defined through 5% transmission ND Filter as following.



[Note3]

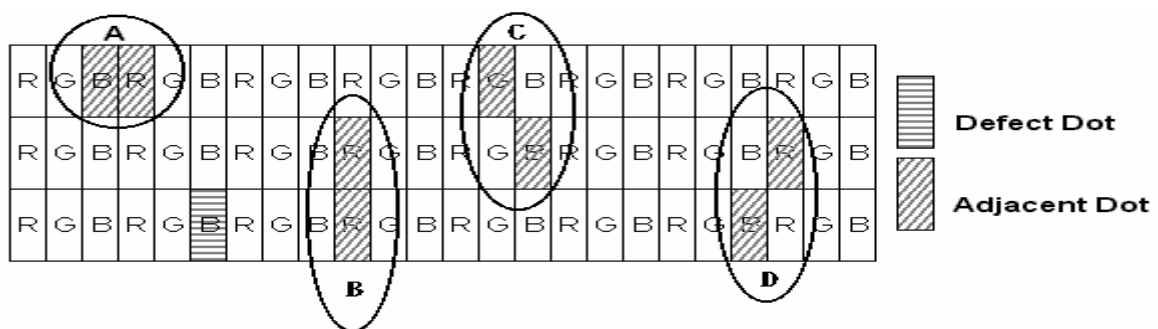


C Area: Center of display area

O Area: Outer of display area

[Note4]

Judge defect dot and adjacent dot as following. Allow below (as A, B, C and D status) adjacent defect dots, including bright and dark adjacent dot. And they will be counted 2 defect dots in total quantity.



- (1) The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.
- (2) Defects on the Black Matrix, out of Display area, are not considered as a defect or counted.

7 Reliability test items (Note2):

No.	Test items	Conditions	Remark
1	High temperature storage	Ta=70℃ 240Hrs	
2	Low temperature storage	Ta=-20℃ 240Hrs	
3	High temperature operation	Ta=60℃ 240Hrs	
4	Low temperature operation	Ta=0℃ 240Hrs	
5	High temperature and high humidity	Ta=70℃,90% RH 240Hrs	Operation
6	Heat shock	-0℃~60℃/200 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200Pf(0Ω),once for each terminal	Non-operation
8	Vibration	Frequency range :8~33.3Hz Stoke :1.3mm Sweep :2.9G,33.3~400Hz Cycle :15 minutes 2 hours for each direction of X,Z 4 hours for Y direction	JIS C7021, A-10 Condition A
9	Mechanical shock	100G, 6ms,±X, ±Y,±Z 3 times for each direction	JIS C7021, A-7 Condition C
10	Vibration (With carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/octave from 200~500Hz	IEC 68~34
11	Drop (with carton)	Height:60cm 1 corner,3 edges,6 surfaces	JIS Z0202

Note 1:Ta:Ambient temperature.

Note 2:In the standard conditions, there is not display function NG issue occurred.

All the cosmetic specification is judged before the reliability stress.

8 USE PRECAUTIONS

8.1 Handling precautions

- 1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
- 2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
- 3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
- 4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

8.2 Installing precautions

- 1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. $1\text{M}\Omega$ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
- 2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
- 3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
- 4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

8.3 Storage precautions

- 1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
- 2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.

- 3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

8.4 Operating precautions

- 1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
- 2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
- 3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC drive voltage.
- 4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
- 5) Make certain that each signal noise level is within the standard (L level: 0.2V_{dd} or less and H level: 0.8V_{dd} or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
- 6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
- 7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
- 8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

8.5 Other

- 1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
- 2) The residual image may exist if the same display pattern is shown for hours. This residual image, however, disappears when another display pattern is shown or the drive is interrupted and left for a while. But this is not a problem on reliability.

9 OUTLINE DIMENSION

