

A Brighter Solution

AMP DISPLAY INC.

SPECIFICATIONS

LCD MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	A F - 2 4 0 1 6 0 E F I Q Y - 0 0 H
APPROVED BY:	
DATE:	

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APPROVED FOR SPECIFICATIONS

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APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

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RECORD OF REVISION

Revision Date	Contents	Editor
2004/3/26	New Release	Patrick

1 FEATURES

- (1) Display format : 240×160 dots, 1/160 duty, 1/13 bias.
- (2) Construction : LCD panel, Edge LED Yellow -Green backlight and COF technology.
- (3) Display type : FSTN, Transflective, Positive , 6 o'clock view.
- (4) Controller : “ULTRACHIP” UC1611
- (5) Interface for 8080 or 6800 series family MPU, select by BM0, BM1 setting.
- (6) Extended temperature type.

2 MECHANICAL DATA

Parameter	Stand Value	Unit
Dot size	0.23(W) × 0.23(H)	mm
Dot pitch	0.24(W) × 0.24(H)	mm
Active area	57.59(W) × 38.39(H)	mm
Viewing area	63.0(W) × 42.5(H)	mm
Module size	81.0(W) × 115.5(H) × 6.5Max.(T)	mm

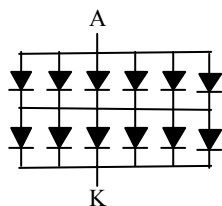
3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic Circuit Supply Voltage	VDD-VSS	-0.3	+4.0	V
LCD Driving Voltage	VLCD	-4	+18.0	V
Input Voltage	Vi	-0.3	VDD+0.3	V
Operating Temp.	TOP	-20	70	°C
Storage Temp.	TSTG	-30	80	°C

4 ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
----- Electronic Characteristics -----							
Logic Circuit Supply Voltage	VDD-VSS	--	2.4	2.8	3.3	V	
LCD Driving Voltage (FSTN)	VLCD	-20 °C	--	--	--	V	* The LCD driving should be decided by real design.
		0 °C	--	--	--		
		25 °C	13.6	13.7	13.8		
		50 °C	--	--	--		
		70 °C	--	--	--		
Input Voltage	VIH	--	0.8VDD	--	VDD	V	
	VIL	--	-0	--	0.2 VDD	V	
Logic Supply Current	IDD	VDD=2.8V	--	2.1	2.8	mA	
----- Optical Characteristics (FSTN) -----							
Contrast	CR	25°C	2	5	--		Note 1
Rise Time	tr	25°C	--	170	--	ms	Note 2
Fall Time	tf	25°C	--	200	--	ms	
Viewing Angle Range	θ f	25°C & CR≥2	--	35	--	Deg.	Note 3
	θ b		--	40	--		
	θ l		--	40	--		
	θ r		--	40	--		
Frame Frequency	fF	25°C	--	70	--	Hz	
----- Edge LED Yellow-Green Back-light Characteristics -----							
Forward Voltage	VF	--	--	4.1	--	V	Supply Voltage between A&K
Forward Current	IF	VF=4.1V	--	90	--	mA	
LCM Luminous intensity		VF=4.1V	--	4	--	cd/m ²	

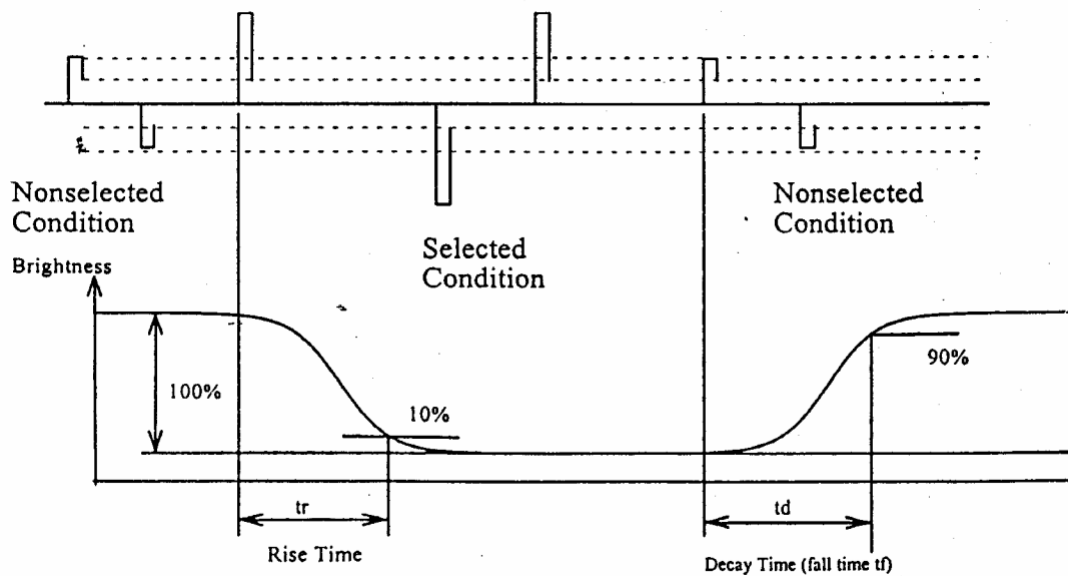
* LED Dice number = 12



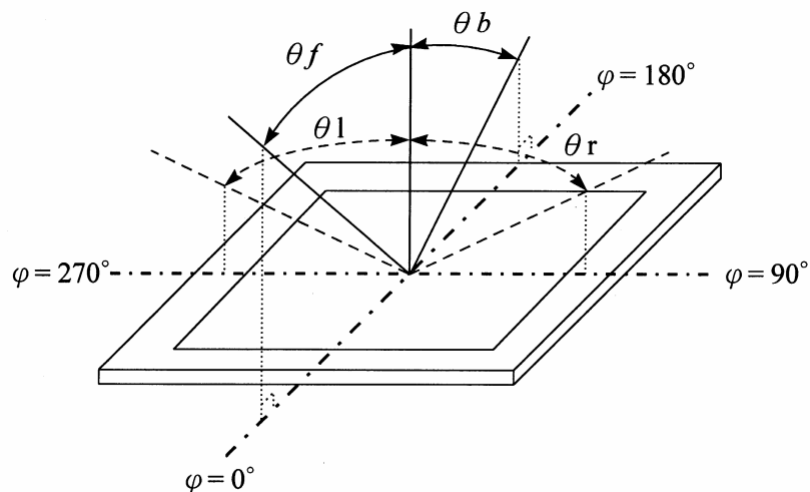
(NOTE 1) Contrast ratio :

$$CR = (\text{Brightness in OFF state}) / (\text{Brightness in ON state})$$

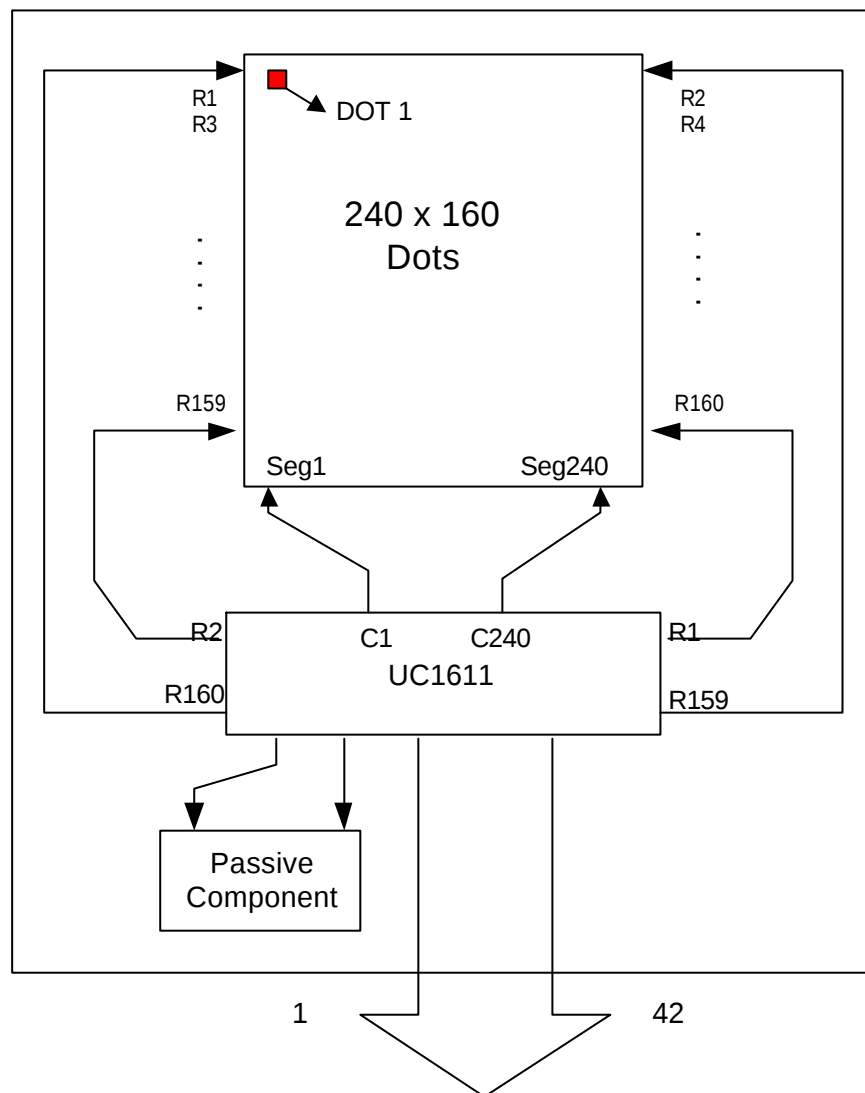
(NOTE 2) Response time :



(NOTE 3) Viewing angle



5 BLOCK DIAGRAM & POWER SUPPLY



Default Setting:

Symbol	H/L	Description
VCM	OPEN	Leave that pin "open" in single LCM situation.
VS1	OPEN	
VS0	OPEN	
PUMP_DN	OPEN	
DISP_ON	OPEN	
SCLK	OPEN	
SM	L	Master mode or default in other situation

6 INTERFACE

No.	Symbol	Function	
1	NC	No Connection	
2	VDD	Power supply for logic and other analog circuits.	
3	VSS	Ground (0V)	
4	BM0	Bus modes : “HL” : 8 bit 8080 “HH” : 8 bit 6800 BM[1:0] “LL” : 4 bit 8080 “LH” : 4 bit 6800	
5	BM1		
6	WR1	Bus Type : 8080 mode “/RD” ; 68mode “E”	
7	WR0	Bus Type : 8080 mode “/WR” ; 68 mode “R/W”	
8	CD	Select Control data or Display data for read/write operation. (“H” : Display data, “L” : control data)	
9	CS1	Chip Select. Chip is selected when CS1=“H” . When the chip is not selected, D[7:0] will be high impedance.	
10	RST	When RST=“L” , all control register are re-initialized by their default state and/or by their pin configurations if applicable.	
11	D0	8 bits Data Bus for 8080 or 6800 series	4 bits Data Bus for 8080 or 6800 series
12	D1		
13	D2		
14	D3		
15	D4		
16	D5		
17	D6		
18	D7		
19	VSS	Ground (0V)	
20	NC	No Connection	

7 INSTRUCTION SET

The following is a list of host commands support by UC1611

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

Useful Data bits
- Don't Care

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action
Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte @ PA/CA
Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte @ PA/CA
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status Summary
Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]=D[3:0]
Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]=D[3:0]
Set Mux rate.	0	0	0	0	1	0	0	0	#	#	Set MR[1:0]=D[1:0]
Set Temp. Compensation.	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]=D[1:0]
Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]=D[1:0]
Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]=D[1:0]
Set Adv. Program Control (double byte command)	0	0	0	0	1	1	0	0	#	#	Set APC[R][7:0]=D[7:0], where R = 0, or 1
	0	0	#	#	#	#	#	#	#	#	
Set Max CA (double byte command)	0	0	0	0	1	1	0	0	1	0	Set MC = D[6:0]
	0	0	-	#	#	#	#	#	#	#	
Set Start Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]=D[3:0]
Set Start Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]=D[3:0]
Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]=D[3:0]
Set Page Address MSB	0	0	0	1	1	1	#	#	#	#	Set PA[7:4]=D[3:0]
Set V _{REF} potential meter (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[5:0]=D[5:0]
	0	0	#	#	#	#	#	#	#	#	Set GN[1:0]=D[7:6]
Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]=D[2:0]
Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]=D[3:0]
Set Frame Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]=D[1:0]
Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]=D0
Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]=D0
Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]=D[2:0]
Set LCD Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]=D[2:0]
Set N-Line Inversion	0	0	1	1	0	1	1	#	#	#	Set DC[7:5]=D[1:0]
Set Gray Scale Mode	0	0	1	1	0	1	0	0	#	#	Set LC[6:5] = D[1:0]
System Reset	0	0	1	1	1	0	0	0	1	0	System Reset sequence
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]= D[1:0]
Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	Set AC[3]=0, CA=CR;
Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	Set AC[3]=1, CR=CA;
Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.
	0	0	#	#	#	#	#	#	#	#	

* Other than commands listed above, all other bit patterns result in NOP (No Operation).

DATA FORMAT :

MSF		Line Addresss
0	1	
D3/0	D7/4	00H
D7/4	D3/0	01H
D3/0	D7/4	02H
D7/4	D3/0	03H
D3/0	D7/4	04H
D7/4	D3/0	05H
D3/0	D7/4	06H
D7/4	D3/0	07H
D3/0	D7/4	08H
D7/4	D3/0	09H
D3/0	D7/4	0AH
D7/4	D3/0	0BH
D3/0	D7/4	0CH
D7/4	D3/0	0DH
D3/0	D7/4	0EH
D7/4	D3/0	0FH
D3/0	D7/4	10H
D7/4	D3/0	11H
D3/0	D7/4	12H
D7/4	D3/0	13H
D3/0	D7/4	14H
D7/4	D3/0	15H
D3/0	D7/4	16H
D7/4	D3/0	17H
D3/0	D7/4	18H
D7/4	D3/0	19H
D3/0	D7/4	1AH
D7/4	D3/0	1BH
D3/0	D7/4	1CH
D7/4	D3/0	1DH
D3/0	D7/4	1EH
D7/4	D3/0	1FH

RAM					
				Page 0	
				Page 1	
				Page 2	
				Page 3	
				Page 4	
				Page 5	
				Page 6	
				Page 7	
				Page 8	
				Page 9	
				Page 10	
				Page 11	
				Page 12	
				Page 13	
				Page 14	
				Page 15	

D390	D774	30-H
D774	D390	30-H
D390	D774	35-H
D774	D390	35-H
D390	D774	40-H
D774	D390	40-H
D390	D774	42-H
D774	D390	43-H
D390	D774	44-H
D774	D390	45-H
D390	D774	46-H
D774	D390	47-H
D390	D774	48-H
D774	D390	49-H
D390	D774	45-H
D774	D390	46-H
D390	D774	40-H
D774	D390	40-H
D390	D774	41-H
D774	D390	44-H

	Page 70	
	Page 71	
	Page 72	
	Page 73	
	Page 74	
	Page 75	
	Page 76	
	Page 77	
	Page 78	
	Page 79	

MY=0		MY=1			
SL=0	SL=8	SL=0	SL=0	SL=8	SL=8
R1	R145	R160	R96	R16	R16
R2	R146	R159	R95	R15	R15
R3	R147	R158	R94	R14	R14
R4	R148	R157	R93	R13	R13
R5	R149	R156	R92	R12	R12
R6	R150	R155	R91	R11	R11
R7	R151	R154	R90	R10	R10
R8	R152	R153	R89	R9	R9
R9	R153	R152	R88	R8	R8
R10	R154	R151	R87	R7	R7
R11	R155	R150	R86	R6	R6
R12	R156	R149	R85	R5	R5
R13	R157	R148	R84	R4	R4
R14	R158	R147	R83	R3	R3
R15	R159	R146	R82	R2	R2
R16	R160	R145	R81	R1	R1
R17	R1			R160	R96
R18	R2			R159	R95
R19	R3			R158	R94
R20	R4			R157	R93
R21	R5			R156	R92
R22	R6			R155	R91
R23	R7			R154	R90
R24	R8			R153	R89
R25	R9			R152	R88
R26	R10			R151	R87
R27	R11			R150	R86
R28	R12			R149	R85
R29	R13			R148	R84
R30	R14			R147	R83
R31	R15			R146	R82
R32	R16			R145	R81

R141	R20	10-10-10	10-10-10
R142	R19	10-10-10	10-10-10
R143	R18	10-10-10	10-10-10
R144	R17	10-10-10	10-10-10
R145	R16	10-10-10	10-10-10
R146	R15	10-10-10	10-10-10
R147	R14	10-10-10	10-10-10
R148	R13	10-10-10	10-10-10
R149	R12	10-10-10	10-10-10
R150	R11	10-10-10	10-10-10
R151	R10	10-10-10	10-10-10
R152	R9	10-10-10	10-10-10
R153	R8	10-10-10	10-10-10
R154	R7	10-10-10	10-10-10
R155	R6	10-10-10	10-10-10
R156	R5	10-10-10	10-10-10
R157	R4	10-10-10	10-10-10
R158	R3	10-10-10	10-10-10
R159	R2	10-10-10	10-10-10
R160	R1	10-10-10	10-10-10

[illegible]

CONTROL REGISTERS :

UC1611 contains registers which control the chip operation. These registers can be modified by commands. The commands supported by UC1611 are described in the next section.

Name: The Symbolic reference of the register byte.
Note that, some symbol names refers to collection of bits (flags) within one register byte.

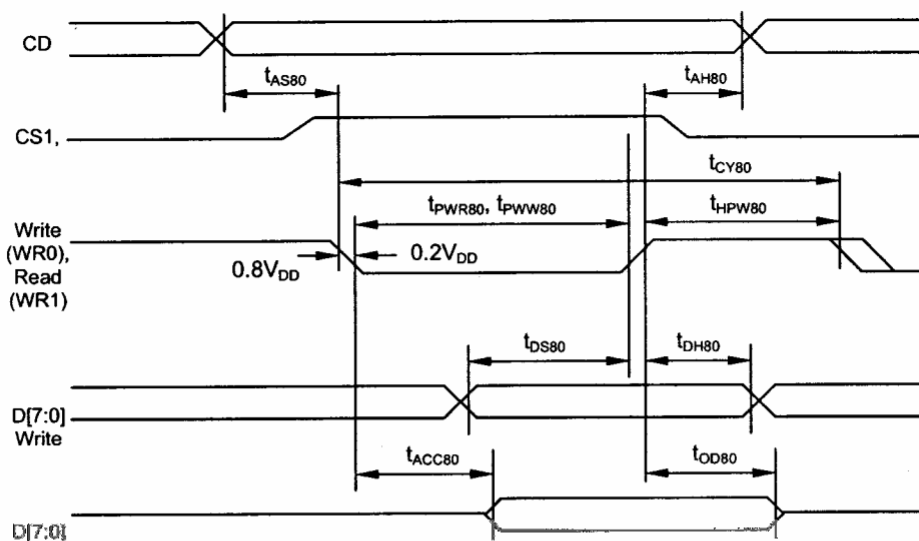
Default: Value after *Power-up-Reset* and *System-Reset*.
"PIN" means default value depends on the connection of associated configuration pin(s).

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value are between 0 (for no scrolling) and (159 – 2xFL). Setting SL outside of this range cause undefined effect on the displayed image.
FL	4	0H	Fixed lines. The first FLx2 lines of each frame are fixed and are not affected by scrolling (SL). When FL is non-zero, the screen is effectively separated into two region: one scrollable, one non-scrollable.
CR	8	0H	Return Column Address.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	7	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_D .
TC	2	1H	Temperature Compensation (per °C). 00: 0.0% 01: -0.05% 10: -0.1% 11: -0.2%
GN	2	3H	Gain = V_D / V_{PM}
PM	6	10H	Electronic Potential Meter to generate V_{PM} from V_{REF}
MR	2	3H	Multiplexing Rate: Number of pixel rows: 0: 64 1: 96 2: 128 3: 160
OM	2	0	Operating Modes 10: Sleep 11: Normal 01: (Not used) 00: Reset
BZ	1	–	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1		Reset in progress, Host Interface not ready
PC	4	0DH	Power Control. PC[1:0]: 00: LCD: <20nF 01: LCD: 20~28nF 10: LCD: 28~40nF 11: LCD: 40~56nF PC[3:2]: 00: External V_{LCD} 01: 6x pump 10: 7x pump 11: 8x pump
APC0	8	00H	Advanced Program Control. Default value should work fine.

Name	Bits	Default	Description
DC	8	0H	Display Control: DC[0]: PXV: Pixels Inverse DC[1]: APO: All Pixels ON DC[4:2]: Display ON/OFF. Each bit controls a set of column drivers (80-80-80). When DC[4:2] is set to "HLH", the chip is turned into a 160x160 controller-driver and the programmers' view of CA becomes 0~159. DC[5]: N-Line inversion. 0: Invert every 17 lines. 1: Invert every 9 lines. DC[6:7]: Idle insertion control when N-Line inversion.
AC	4	1H	Address Control: AC[0]: WA: Automatic column/page Wrap Around AC[1]: Auto-Increment order 0: Column (CA) first 1: Page (PA) first AC[2]: PID: PA (page address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, when CUM=1, CA increment on write only, wrap around suspended
MC	8	EFH	CA max. CA wrapping boundary: when CA+1 = MC, CA will reset to 0. The proper value range for MC is 0~239 or 0~159, depends on the value of DC[4:2]. The chip's behavior is undefined when MC is out of these ranges.
LC	6	08H	LCD Control: LC[0]: MSF: MSB First mapping Option LC[1]: MX, Mirror X (Column sequence inversion) LC[2]: MY, Mirror Y (Row sequence inversion) LC[4:3]: Frame Rate 0: 135 fps 1: 150 fps 2: 165 fps 1: 185 fps LC[6:5]: Gray Scale selection 00 : 16 gray scale 01 : 8 gray scale 10 : black/white

8 TIMING CHARACTERISTICS

8080-SYSTEM

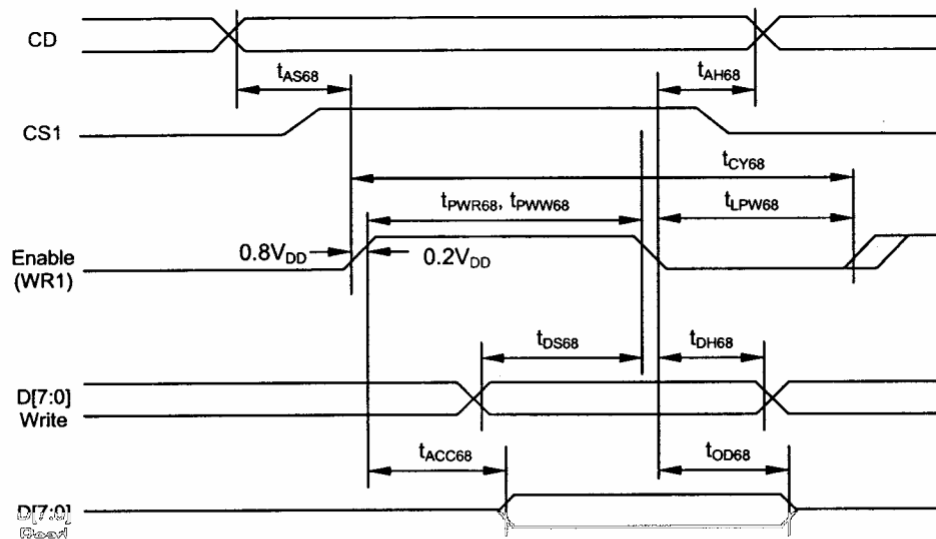


Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80}	CD	Address setup time		20	—	ns
t_{AH80}	CD	Address hold time		40	—	ns
t_{CY80}		System cycle time		100	—	ns
t_{PWR80}	WR1	Pulse width (read)		45	—	ns
t_{PWW80}	WR0	Pulse width (write)		45	—	ns
t_{HPW80}	WR0, WR1	High pulse width		40	—	ns
t_{DS80}	D0~D7	Data setup time		30	—	ns
t_{DH80}	D0~D7	Data hold time		10	—	ns
t_{ACC80}		Read access time	$C_L = 100\text{pF}$	—	50	ns
t_{OD80}		Output disable time		10	50	ns

6800-SYSTEM



Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= -30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68}	CD	Address setup time		20	—	ns
t_{AH68}	CD	Address hold time		40	—	ns
t_{CY68}		System cycle time		100	—	ns
t_{PWR68}	WR1	Pulse width (read)		45	—	ns
t_{PWW68}		Pulse width (write)		45	—	ns
t_{LPW68}		Low pulse width		40	—	ns
t_{DS68}	D0-D7	Data setup time		30	—	ns
t_{DH68}		Data hold time		10	—	ns
t_{ACC68}		Read access time	$C_L = 100pF$	—	50	ns
t_{OD68}		Output disable time		10	50	ns

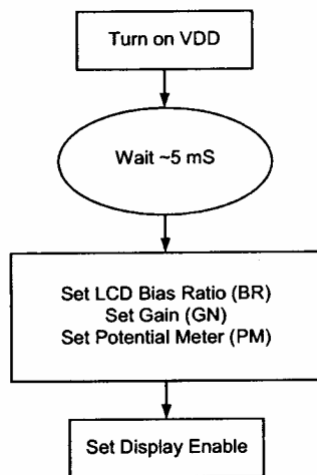
POWER ON/OFF SEQUENCE :

Power-ON Sequence :

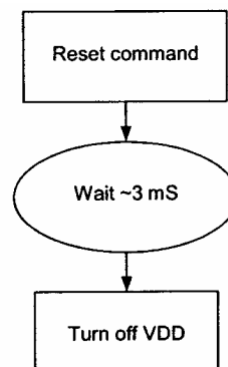
UC1611 power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of System-Reset command after Power-ON-Reset. System programmer are only commands to UC1611. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

Power-OFF Sequence :

To prevent the charge stored in capacitors C_{BX+} , C_{BX-} , and C_{LCD} from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.



Reference Power-ON sequence



Reference Power-OFF sequence

9 QUALITY AND RELIABILITY

9.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : $25 \pm 5^{\circ}\text{C}$

Humidity : $60 \pm 25\% \text{ RH}$.

9.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL -STD-105E , level II, normal single sampling plan .

9.3 ACCEPTABLE QUALITY LEVEL

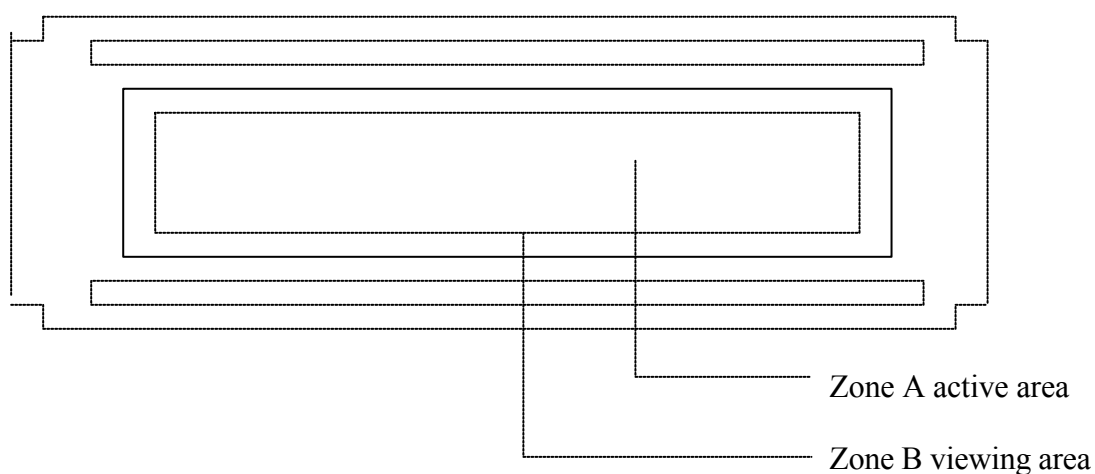
A major defect is defined as one that could cause failure to o r materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

9.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of follow ing limits.

9.5 INSPECTION QUALITY CRITERIA

Item	Description of defects				Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut				Major	0.65
Dimension	Deviation from drawings				Major	1.5
Black spots	Ave . dia . D	area A	area B		Minor	2.5
	D≤0.2	Disregard				
	0.2<D≤0.3	3	4			
	0.3<D≤0.4	2	3			
	0.4<D	0	1			
Black lines	Width W, Length L		A	B	Minor	2.5
	W≤0.03		disregard			
	0.03<W≤0.05		3	4		
	0.05<W≤0.07 , L≤3.0		1	1		
	See line criteria					
Bubbles in polarizer	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N = 1				Minor	2.5
Color uniformity	Rainbow color or newton ring.				Minor	2.5
Glass Scratches	Obvious visible damage.				Minor	2.5
Contrast ratio	See note 1				Minor	2.5
Response time	See note 2				Minor	2.5
Viewing angle	See note 3				Minor	2.5



9.6 RELIABILITY

Test Item	Test Conditions	Note
	Extended Temp. type	
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-20±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-30±3°C , t=96 hrs	1,2
Thermal Shock Test	-20°C ~ 25 °C ~ 70 °C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	40 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency: 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions
(15 ~ -35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

10 HANDLING PRECAUTIONS

- (1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.
- (2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.
- (3) Under no circumstances should the position of the bezel tabs or their shape be modified.
- (4) Do not modify the display PCB in either shape or positioning of components.
- (5) Do not modify or move location of the zebra or heat seal connectors.
- (6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.
- (7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.
- (8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.
- (9) Prior to initial power up input signals should not be applied.
- (10) Protect the module against static electricity and observe appropriate anti-static precautions.

11 OUTLINE DIMENSION

