晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	Telian
CUSTOMER PART NO.	
AMPIRE PART NO.	AT-11264DFI-00H
APPROVED BY	
DATE	

☐ Approved For Specifications
☑ Approved For Specifications & Sample

AMPIRE CO., LTD.
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APPROVED BY	CHECKED BY	ORGANIZED BY

AMP DISPLAY INC.

A Brighter Solution

SPECIFICATIONS

SIZE TFT MODULE

CUSTOMER:	
CUSTOMER PART NO.	
AMP DISPLAY PART NO.	
APPROVED BY:	
DATE:	

☐ APPROVED FOR SPECIFICATIONS

☐ APPROVED FOR SPECIFICATION AND PROTOTYPES

AMP DISPLAY INC

9856 SIXTH STREET RANCHO CUCAMONGA CA 91730

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RECORD OF REVISION

Revision Date	Contents
2001/9/26	New Release
2001/9/27	Change controller KS0723TB-03 to KS0723TB-01 (Page 3)
	Modify block diagram & interface (Page 7,8)
2001/10/17	Added the electrical characteristics (Page 4,5)
2001/10/18	Modify the ABS Max. rating (Page 3)
2002/4/15	Change LCD polarizer to P5 (Page 3)
	Modify OLB connection define (Page 11)

1 FEATURES

(1) Display format : 112×64 dots, 1/65 duty, 1/9 bias.

(2) Construction : LCD panel and TAB IC.

(3) Display type : FSTN , Transflective, Positive , 6 o'clock view

(4) LCD polarizer type : P5

(5) Controller : KS0723TB-01

(6) Extend temperature type.

2 MECHANICAL DATA

Parameter	Stand Value	Unit
Dot size	0.24(W) × 0.28(H)	mm
Dot pitch	0.26(W) × 0.30(H)	mm
Active area	29.1(W) × 19.18 (H)	mm
Viewing area	34.0(W) × 23.0 (H)	mm
Module size	38.0(W) ×49.8(H) ×1.75Max(T)	mm

3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic Circuit Supply Voltage	VDD-VSS	-0.3	3.0	V
LCD Driving Voltage	VLCD	-0.3	+12.0	V
Input Voltage	V_I	-0.3	VDD+0.3	V
Operating Temp.	T_{OP}	-30	70	°C
Storage Temp.	T_{STG}	-40	80	°C

4 ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin used
Operating voltage(1)		V_{DD}		2.4	-	5.5	V	V_{DD} *1
Operating voltage(2)		V0		4.5	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	Ta = 25°C Duty ratio = 1/65	TBD	43.6	TBD	kHz	*8 CL
	External	f_{CL}		TBD	5.45	TBD		
Voltage converter Input voltage		V_{DD}	× 2	2.4	-	3.6	V	V_{DD}
			× 3	2.4	-	5.3		
			× 4	2.4	-	4.0		
			× 5	2.4	-	3.2		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	15.0	V	V0 *9
Reference voltage		V_{REF0}	Ta = 25°C 0.05%/°C	2.04	2.1	2.16	V	*10

DC Characteristics

Dynamic Current Consumption (1) when the built-in Power circuit is OFF (At operate mode)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption(1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V 1/65 Duty ratio Display Pattern OFF	-	15	23	µA	*11

Dynamic Current Consumption (2) when the built-in power circuit is ON (At operate mode)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, (VCI = V_{DD}, 4 times boosting) V0 – Vss = 11.0V, 1/65 Duty ratio, Display Pattern OFF, Normal Power Mode	-	40	60	µA	*12
		V_{DD}=3.0V, (VCI = V_{DD}, 4 times boosting) V0 - Vss=11.0V, 1/65 Duty ratio, Display Pattern Checker, Normal Power Mode	-	150	200	µA	*12

Current Consumption during Power Save mode

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin used
Sleep mode current	I_{DDS1}	During Sleep	-	-	5.0	µA	
Standby mode current	I_{DDS2}	During Standby	-	-	10.0	µA	

The relationship between oscillation frequency and frame frequency

Duty Ratio	ITEM	f_{CL}	f_{OSC}
1/65	On-chip oscillator circuit is used	$\frac{fosc}{8}$	$\frac{fosc}{2 \times 8 \times 65}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{fosc}{2 \times 65}$

[* Remark Solves]

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2 In case of external power supply is applied.
*3 CS1B, CS2, RS, DB0 to DB7, E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*4 DB0 to DB7, M, FR, DISP, CL pins.
*5 CS1B, CS2, RS, DB[7:0], E_RDB, RW_WRB, RESETB, MS, C68, PS, INTRS, HPMB, CLS, CL, M, FR, DISP pins.
*6 Applies when the DB[7:0], M, FR, DISP, and CL pins are in high impedance.
*7 Resistance value when ± 0.1[mA] is applied during the On status of the output pin SEGn or COMn. RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8 See **Table 21** for the relationship between oscillation frequency and frame frequency.
*9 The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10 On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12 Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU. The current consumption, when the built-in power supply circuit is on or off. The current flowing through voltage regulation resistors (Ra and Rb) is not included. It does not include the current of the LCD panel capacity, wiring capacity, etc

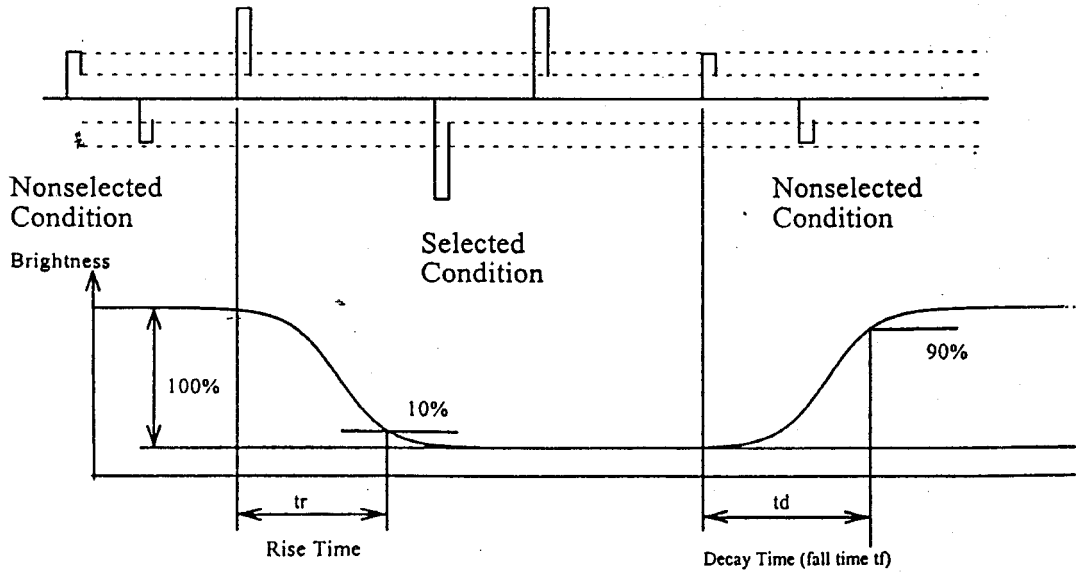
5 ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
----- Electronic Characteristics -----							
Logic Circuit Supply Voltage	VDD-VSS	--	2.4	--	3.6	V	
LCD Driving Voltage (FSTN)	VLCD	-20 °C	--	--	--	V	
		25 °C	--	9.0	--		
		70 °C					
Input Voltage	VIH	--	0.8VDD	--	VDD	V	
	VIL	--	VSS	--	0.2VDD	V	
Logic Supply Current	IDD	VDD=3.0V	--	150	200	uA	
----- Optical Characteristics (FSTN) -----							
Contrast	CR	25°C	8.2	12.8	--		Note 1
Rise Time	tr	25°C	--	150	--	ms	Note 2
Fall Time	tf	25°C	--	150	--	ms	
Viewing Angle Range	θ f	25°C & CR≥2	--	40	--	Deg.	Note 3
	θ b		--	35	--		
	θ l		--	40	--		
	θ r		--	40	--		
Frame Frequency	fF	25°C	--	70	--	Hz	

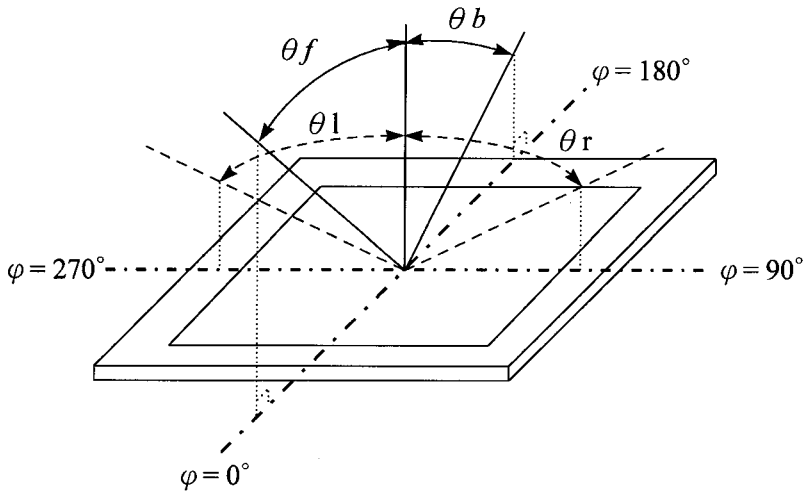
(NOTE 1) Contrast ratio :

CR = (Brightness in OFF state) / (Brightness in ON state)

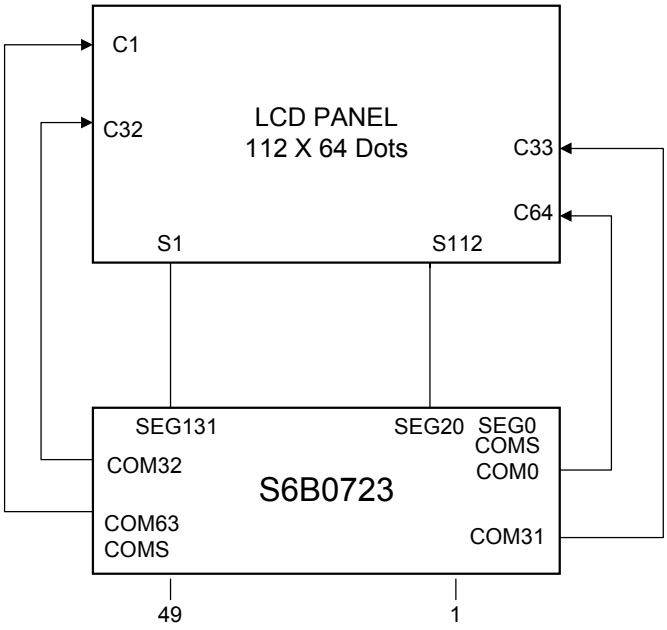
(NOTE 2) Response time :



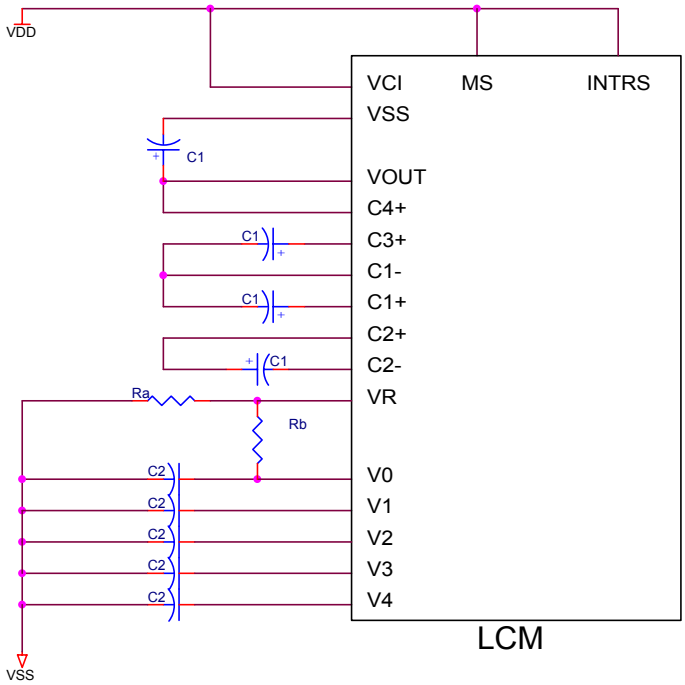
(NOTE 3) Viewing angle



6 BLOCK DIAGRAM & POWER SUPPLY



When not using iternal regulator resistors



<Voltage convert : 4 times>

When Using all LCD power circuits (VCI=VDD, 4-time V/C: ON, V/R: ON, V/F:ON)

7 INTERFACE

No.	Symbol	Function
1	DUMMY	No connection
2	INTRS	Internal resistor select pin “H”: internal “L”:external
3	HPMB	Power control pin of the power supply circuits for LCD driver “H”: Normal mode “L”:High power mode
4	PS	Parallel / serial data input select input “H”: Parallel “L”:Serial
5	C68	Interface Select “H” : 68-series “L” : 80-series
6	CLS	Built-in oscillator circuit enable / disable select pin “H”: enable “L”:disable
7	MS	Master / slave mode select input “H”: master mode “L”:slave mode
8	VR	V0 voltage adjustment pin
9	V0	LCD driver supply voltages Voltages should have the following relationship; V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
10	V4	
11	V3	
12	V2	
13	V1	
14	REF	Select the external VREF voltage via VEXT pin - REF=”H”: using the internal VREF -REF=“L”: using the external VREF
15	VEXT	This is the external input reference voltage(VREF) for the internal voltage regulator.
16	C2-	Capacitor 2 negative connection pin for voltage converter
17	C2+	Capacitor 2 positive connection pin for voltage converter
18	C1+	Capacitor 1 positive connection pin for voltage converter
19	C1-	Capacitor 1 negative connection pin for voltage converter
20	C3+	Capacitor 3 positive connection pin for voltage converter
21	C4+	Capacitor 4 positive connection pin for voltage converter
22	VOUT	Voltage converter input / output pin
23	VSS	Ground (0V)
24	VCI	This is the reference voltage for the voltage converter circuit for the LCD driving.
25	VDD	Power Supply for Logic
26	DUTY1	The LCD driver duty ratio select pin - 1/65 Duty : DUTY0,1= H
27	DUTY0	

28	DB7	8-bit data bus	Serial input data (SI)
29	DB6		Serial input clock (SCL)
30	DB5		When the serial interface selected (PS="L"), DB0~DB5 : high impedance
31	DB4		
32	DB3		
33	DB2		
34	DB1		
35	DB0		
36	E_RDB	68 –series: E ; 80-series : /RD	
37	RW_WRB	Read / Write execution control pin 68 series: "H": read "L": write 80 series: "H": write enable clock input pin	
38	RS	Register select input pin RS="H": Indicates that D0 to D7 are Display Data RS="L": Indicates that D0 to D7 are Control Data	
39	RESETB	Hardware reset input	
40	CS2	Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H".	
41	CS1B		
42	TEST4	No Connection	
43	DISP	LCD display blanking control input / output	
44	CL	Display clock input / output pin	
45	M	LCD AC Signal input / output	
46	TEST3	No connection	
47	TEST2	No connection	
48	TEST1	No connection	
49	DUMMY	No connection	

PIN CONNECTION FOR LCD

PAD NO.	IC PAD NAME	LCD PAD
1-2	DUMMY	DUMMY
3	FR	NC
4	FRS	NC
5	COMS	NC
6 – 37	COM63 – COM32	COM63 – COM32
38 – 149	SEG131 – SEG20	SEG131 – SEG20
150 – 169	SEG111 – SEG0	NC
170	COMS	NC
171 – 202	COM0 – COM31	COM0 – COM31
203 – 204	DUMMY	DUMMY

SHL=1

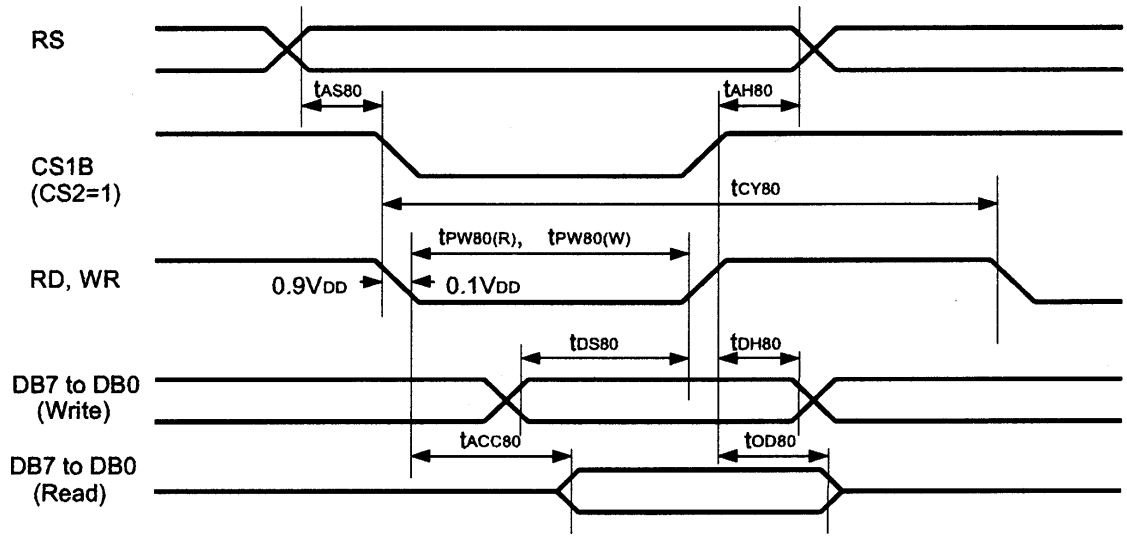
8 INSTRUCTION SET

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Display On/Off	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set Page Address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set Column Address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set Column Address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Read Status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Write Display Data	1	0	Write data								Write data into DDRAM
Read Display Data	1	1	Read data								Read data from DDRAM
ADC Select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC=0: normal direction (SEG0→SEG131) When ADC=1: reverse direction (SEG131→SEG0)
Reverse Display ON/OFF	0	0	1	0	1	0	0	1	1	REV	Select normal/reverse display When REV=0: normal display When REV=1: reverse display
Entire Display ON/OFF	0	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
LCD Bias Select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set Modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL=0: normal direction (COM0→COM63) When SHL=1: reverse direction (COM63→COM0)
Power Control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator Resistor Select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set Reference Voltage Mode	0	0	1	0	0	0	0	0	0	1	Set Reference Voltage Mode
Set Reference Voltage Register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set Reference Voltage Register
Set Static Indicator Mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set Static Indicator Register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power Save	-	-	-	-	-	-	-	-	-	-	Compound Instruction of display OFF and entire display ON

9 TIMING CHARACTERISTICS

9.1 Read / Write Characteristics (80-series MPU)

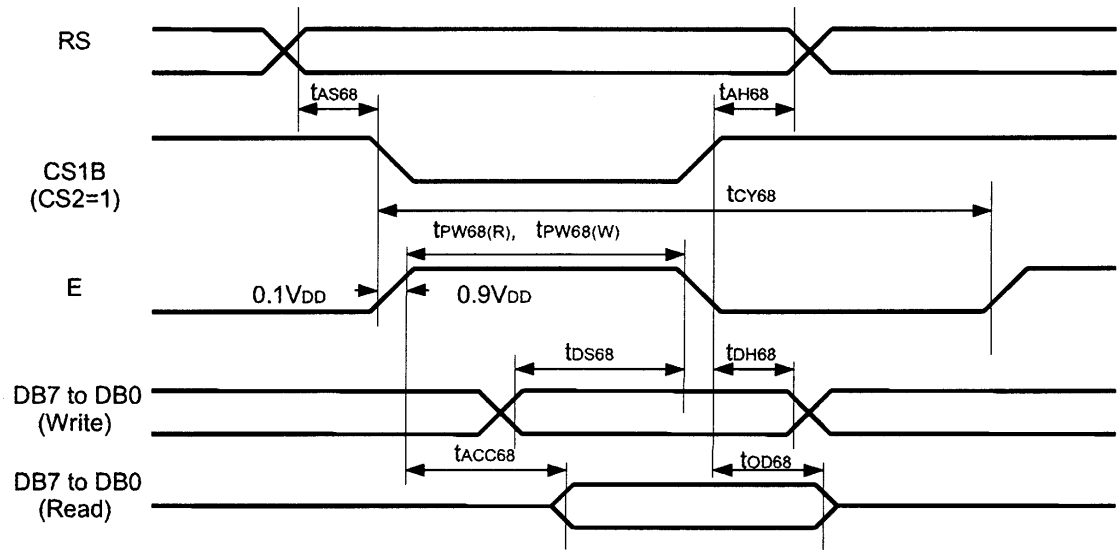


Read / Write Characteristics (80-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	tAS80 tAH80	0 0	-	-	ns	
System cycle	RS	tCY80	400			ns	
Pulse width (WR)	RW_WR	TPW80(W)	60			ns	
Pulse width (RD)	E_RD	TPW80(R)	210			ns	
Data setup time Data hold time	DB7 to DB0	tDS80 tDH80	40 15			ns	
Read access time Output disable time		tACC80 tOD80	- 10		140 100	ns	CL = 100 pF

9.2 Read / Write Characteristics (68-series MPU)

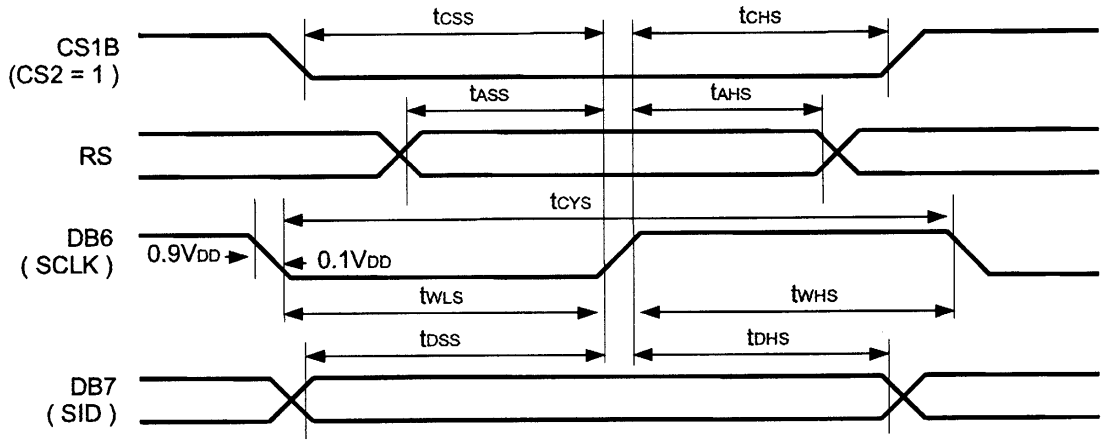


Read / Write Characteristics (68-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle		RS	t_{CY68}	300	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	35 13	-	-	ns	
Read access time Output disable time			t_{ACC68} t_{OD68}	- 10		140 90	ns	CL = 100 pF
Enable pulsewidth	Read Write	E_RD	$t_{PW68(R)}$ $t_{PW68(W)}$	120 60	-	-	-	

9.3 Serial Interface Characteristics



Serial Interface Characteristics

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	250 100 100	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	100 100	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	150 150	- -	- -	ns	

10 QUALITY AND RELIABILITY

10.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

10.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

10.3 ACCEPTABLE QUALITY LEVEL

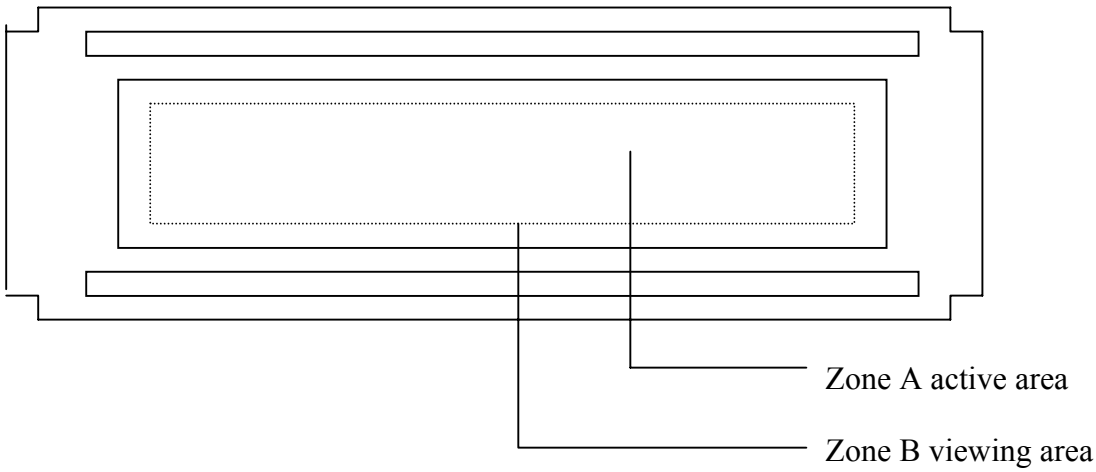
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

10.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.

10.5 INSPECTION QUALITY CRITERIA

Item	Description of defects			Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut			Major	0.65
Dimension	Deviation from drawings			Major	1.5
Black spots	Ave . dia . D	area A	area B	Minor	2.5
	D≤0.2	Disregard			
	0.2<D≤0.3	3	4		
	0.3<D≤0.4	2	3		
	0.4<D	0	1		
Black lines	Width W, Length L	A	B	Minor	2.5
	W≤0.03	disregard			
	0.03<W≤0.05	3	4		
	0.05<W≤0.07 , L≤3.0	1	1		
	See line criteria				
Bubbles in polarizer	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N = 1			Minor	2.5
Color uniformity	Rainbow color or newton ring.			Minor	2.5
Glass Scratches	Obvious visible damage.			Minor	2.5
Contrast ratio	See note 1			Minor	2.5
Response time	See note 2			Minor	2.5
Viewing angle	See note 3			Minor	2.5



10.6 RELIABILITY

Test Item	Test Conditions	Note
	Extend Temp. type	
High Temperature Operation	70±3°C , t=96 hrs	
Low Temperature Operation	-30±3°C , t=96 hrs	
High Temperature Storage	80±3°C , t=96 hrs	1,2
Low Temperature Storage	-40±3°C , t=96 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 80°C 30 m in. 5 min. 30 min. (1 cycle) Total 5 cycle	1,2
Humidity Test	40 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11 HANDLING PRECAUTIONS

(1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.

(2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.

(3) Under no circumstances should the position of the bezel tabs or their shape be modified.

(4) Do not modify the display PCB in either shape or positioning of components.

(5) Do not modify or move location of the zebra or heat seal connectors.

(6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.

(7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.

(8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.

(9) Prior to initial power up input signals should not be applied.

(10) Protect the module against static electricity and observe appropriate anti-static precautions.

12 OUTLINE DIMENSION