MF424-11

EPSON

SED1500 Series

LCD driver with RAM

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

SED1500 Series
Selection Guide

■ LCD drivers with RAM for small- and medium-sized displays

Ultra-low power consumption and on-chip RAM make this series ideal for compact LCD-based equipment.

SED1500 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1510D0C	0.9–6.0	1.8–6.0	1/4	32	4	128	Serial	18 (internal)	Al pad chip	Small segment-type LCD display. Command and data interface
SED1510D0B									Au bump chip	
SED1510F0C									QFP12-48pin	
SED1510F0E									QFP6-60pin	
SED1511D0A									Al pad chip	Small segment-type LCD dislays. Data only interface
SED1520D0A	2.4–7.0	3.5–13	1/16,1/32	61	16	2,560	8-bit parallel	18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1520D0B									Au bump chip	
SED1520F0A									QFP5-100pin	
SED1520F0C									QFP15-100pin	
SED1520T0A									TCP	
SED1520DAA								2 (external)	Al pad chip	
SED1520DAB									Au bump chip	
SED1520FAA									QFP5-100pin	
SED1520FAC									QFP15-100pin	
SED1520TAA#									TCP	
SED1521D0A			1/8–1/32	80	–			18 (external)	Al pad chip	Extension driver for the SED1520 and SED1522
SED1521D0B									Au bump chip	
SED1521F0A									QFP5-100pin	
SED1521F0C									QFP15-100pin	
SED1521T0A#									TCP	
SED1521DAA								2 (external)	Al pad chip	
SED1521DAB									Au bump chip	
SED1521FAA									QFP5-100pin	
SED1521FAC									QFP15-100pin	
SED1521TAA#									TCP	
SED152AD0A									Al pad chip	P-substrate version of SED1521
SED1522D0A			1/8,1/16	69	8			18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1522D0B									Au bump chip	
SED1522F0A									QFP5-100pin	
SED1522F0C									QFP15-100pin	
SED1522T0A#									TCP	
SED1522DAA								2 (external)	Al pad chip	
SED1522DAB									Au bump chip	
SED1522FAA									QFP5-100pin	
SED1522FAC									QFP15-100pin	
SED1522TAA#									TCP	
SED1540D0A		3.5–11	1/3,1/4	73	3, 4			18 (internal) 4 (external)	Al pad chip	Segment-type displays
SED1540D0B									Au bump chip	
SED1540F0A									QFP5-100pin	

: Planning TCP : Tape Carrier Package

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1560D0A	2.4–6.0	6.0–16.0	1/48, 1/49 1/64, 1/65	102	65	166×65 bits	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1560✻0B (1/9 bias) SED1560✻AB (1/7 bias) SED1561✻0B (1/7 bias) SED1561✻AB (1/5 bias)
SED1560DAA									Al pad chip	
SED1560D0B									Au bump chip	
SED1560DAB									Au bump chip	
SED1560T0B									TCP	
SED1560TQA									QTCP	
SED1561D0A			1/24, 1/25 1/32, 1/33	134	33				Al pad chip	
SED1561DAA									Al pad chip	
SED1561D0B									Au bump chip	
SED1561DAB									Au bump chip	
SED1561T0B									TCP	
SED1561TAB									TCP	
SED1561TQA									QTCP	
SED1562D0A			1/16, 1/17 (1/5bias)	150	17				Al pad chip	
SED1562D0B									Au bump chip	
SED1562T0B									TCP	
SED1562TQA									QTCP	
SED1565D0B	1.8–5.5	4.5–16.0	1/65 (1/7, 1/9 bias)	132	65	132×65 bits		33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
SED1565D1B*									Au bump chip	
SED1565D2B									Au bump chip	
SED1565T0A									TCP	
SED1565T0B									TCP	
SED1565T0C									TCP	
SED1566D0B			1/49 (1/6, 1/8 bias)		49				Au bump chip	
SED1566D1B*									Au bump chip	
SED1566D2B									Au bump chip	
SED1566T0A									TCP	
SED1567D0B			1/33 (1/5, 1/6 bias)		33				Au bump chip	
SED1567D1B*									Au bump chip	
SED1567D2B									Au bump chip	
SED1567T0B									TCP	
SED1567T0C									TCP	
SED1568D0B			1/55 (1/6, 1/8 bias)		55				Au bump chip	
SED1569D0B			1/53 (1/6, 1/8 bias)		53				Au bump chip	
SED1569T**									TCP	
SED1570D0A	2.7–5.5	8.0–20.0	1/64–1/200	80	–	200×80 bits	4-bit parallel	–	Al pad chip	Built-in self-refreshing function
SED1570D0B									Au bump chip	
SED1526D*A	2.4–6.0	3.5–Supply voltage ×3	1/8, 1/9 1/16, 1/17		17	80×33 bits	8-bit parallel or Serial	20	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1526✻0✻ (VREG) SED1526✻E✻ (no VREG) SED1526✻A✻ (redistribution of COMS) SED1528✻0✻ (VREG) SED1528✻E✻ (no VREG)
SED1526D*B									Au bump chip	
SED1526F*A									QFP5-128pin	
SED1526T*A									TCP	
SED1528D*A			1/32, 1/33	64	33				Al pad chip	
SED1528D*B									Au bump chip	
SED1528F*A									QFP5-128pin	
SED1528T*A									TCP	

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1530D0A	2.4–6.0	4.5–16.0	1/32, 1/33	100	33	132×65 bits	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (voltage quadrupler) SED153**0* (Common: Right side) SED153**A* (Common: Both side) SED153**B* (Common: Left side) SED153**F* (no VREG)
SED1530DAA									Al pad chip	
SED1530D0B									Au bump chip	
SED1530DAB									Au bump chip	
SED1530TAA									TCP	
SED1531D0A			1/64, 1/65	132	–				Al pad chip	
SED1531D0B									Au bump chip	
SED1531T0A									TCP	
SED1532D0A				100	33				Al pad chip	
SED1532DBA									Al pad chip	
SED1532D0B									Au bump chip	
SED1532DBA									Au bump chip	
SED1532T0A									TCP	
SED1532TBA									TCP	
SED1535D0B*			1/35	98	35				Au bump chip	

TCP : Tape Carrier Package

1. SED1510 Series

Contents

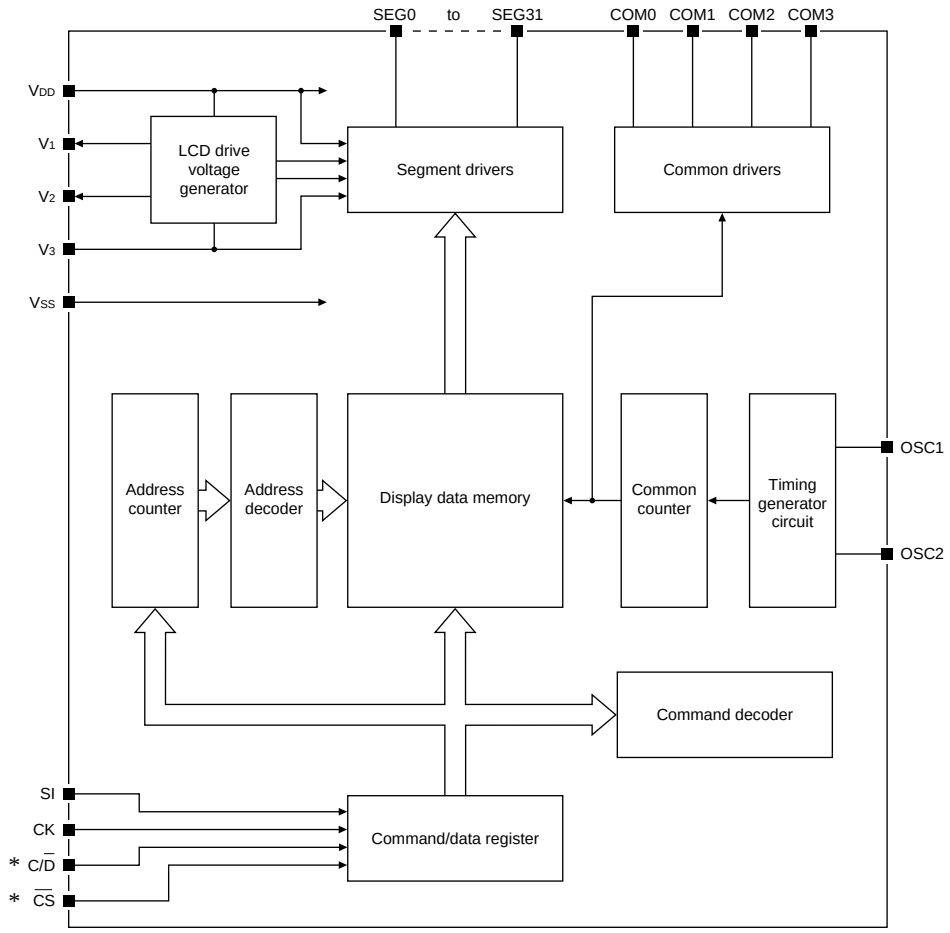
OVERVIEW

The SED1510Series is a segment driver IC for 1/4-duty LCD panels. It features 150 µW maximum power dissipation and a wide operating supply voltage range, making it ideal for use in battery-powered devices. The SED1510 series incorporates an LCD driving power circuit and allows simple configuration of the interface with a microcomputer (controllable by four or two signal lines for the SED1510 or SED1511, respectively), achieving a handy type unit at low cost.

FEATURES

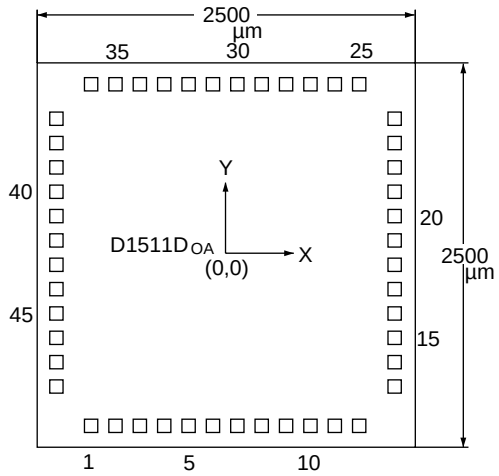
- 1/4-duty LCD segment driver
- 150 µW maximum power dissipation
- Serial data interface
- 128 bits of display data RAM
- On-chip oscillator
- LCD drive voltage generator
- Four common driver outputs
- 32 segment driver outputs
- 0.9 to 6.0 V supply for logic circuitry operation
- 1.8 to 6.0 V supply for LCD driver operation
- Series specification
  SED1510 D0C : chip (Al pad)
  SED1510 F0C : QFP12-48pin
  SED1510 F0E : QFP6-60pin
  SED1511D0A : chip (Al pad)

BLOCK DIAGRAM

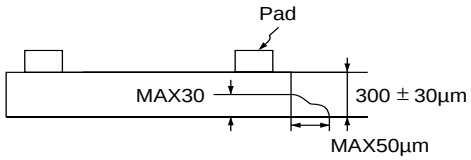


* Only for the SED1510.

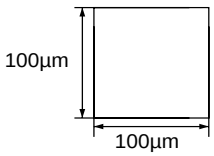
PAD LAYOUT AND COORDINATES (SED1511D0A)



Sectional dimensions



Size of pad opening



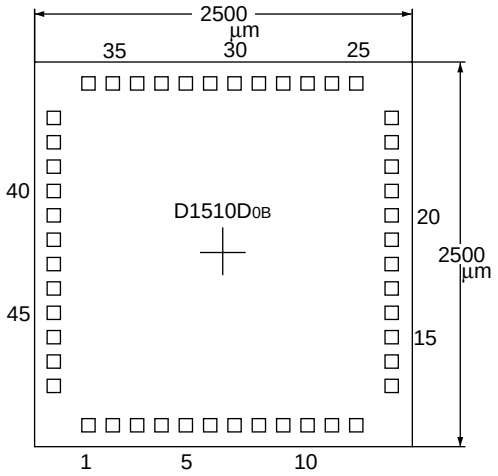
Pad coordinates

Unit: µm

No.	Pin name	X coordinate	Y coordinate	No.	Pin name	X coordinate	Y coordinate
1	OSC1	-898	-1091	25	Seg 8	898	1091
2	OSC2	-738	-1091	26	Seg 9	738	1091
3	V1	-578	-1091	27	Seg 10	578	1091
4	V2	-418	-1091	28	Seg 11	418	1091
5	V3	-258	-1091	29	Seg 12	258	1091
6	V_{SS}	-98	-1091	30	Seg 13	98	1091
7	V_{DD}	63	-1091	31	Seg 14	-63	1091
8	CK	223	-1091	32	Seg 15	-223	1091
9	SI	383	-1091	33	Seg 16	-383	1091
10	NC	543	-1091	34	Seg 17	-543	1091
11	NC	703	-1091	35	Seg 18	-703	1091
12	COM0	863	-1091	36	Seg 19	-863	1091
13	COM1	1091	-898	37	Seg 20	-1091	898
14	COM2	1091	-738	38	Seg 21	-1091	578
15	COM3	1091	-578	39	Seg 22	-1091	578
16	VREG	1091	-418	41	Seg 24	-1091	418
17	Seg 0	1091	-258	42	Seg 25	-1091	258
18	Seg 1	1091	-98	43	Seg 26	-1091	98
19	Seg 2	1091	63	43	Seg 26	-1091	-223
20	Seg 3	1091	224	44	Seg 27	-1091	-223
21	Seg 4	1091	383	45	Seg 28	-1091	-383
22	Seg 5	1091	543	46	Seg 29	-1091	-543
23	Seg 6	1091	703	47	Seg 30	-1091	-703
24	Seg 7	1091	863	48	Seg 31	-1091	-863

Origin: Center of the chip
Chip size: 2,500 × 2,500

PAD LAYOUT AND COORDINATES (SED1510D0B)



Chip size: 2500µm × 2500µm
Chip pitch: 525µm
Bump size: 87µm × 87µm (Typ.)
Bump height: 23µm (Typ.)

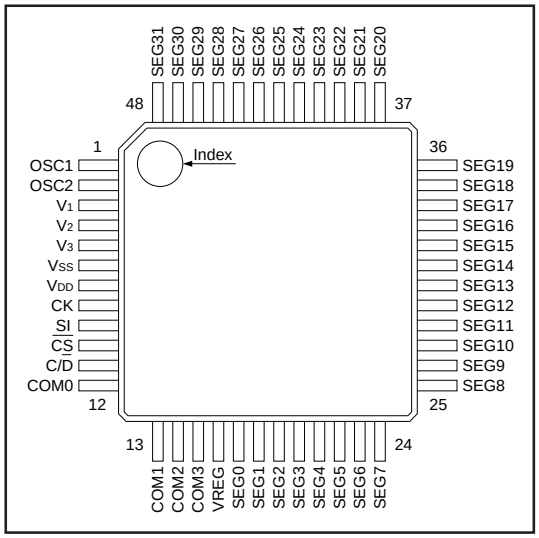
Pad coordinates

Unit: µm

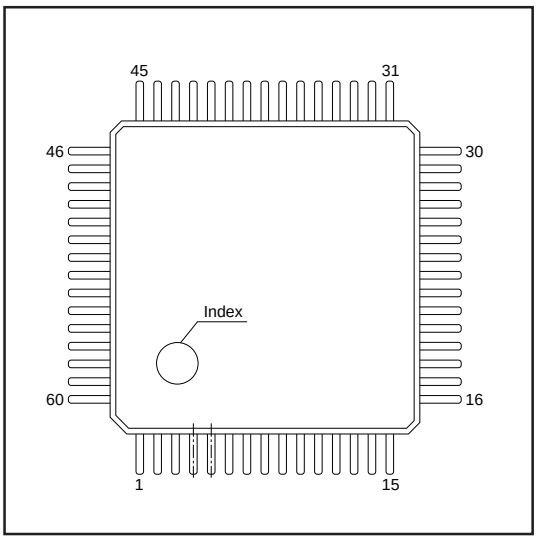
No.	Pin name	X coordinate	Y coordinate	No.	Pin name	X coordinate	Y coordinate
1	OSC1	-898	-1091	25	Seg 8	898	1091
2	OSC2	-738	-1091	26	Seg 9	738	1091
3	V1	-578	-1091	27	Seg 10	578	1091
4	V2	-418	-1091	28	Seg 11	418	1091
5	V3	-258	-1091	29	Seg 12	258	1091
6	VSS	-98	-1091	30	Seg 13	98	1091
7	VDD	63	-1091	31	Seg 14	-63	1091
8	CK	223	-1091	32	Seg 15	-223	1091
9	$\overline{SI}$	383	-1091	33	Seg 16	-383	1091
10	$\overline{CS}$	543	-1091	34	Seg 17	-543	1091
11	C/$\overline{D}$	703	-1091	35	Seg 18	-703	1091
12	COM0	863	-1091	36	Seg 19	-863	1091
13	COM1	1091	-898	37	Seg 20	-1091	898
14	COM2	1091	-738	38	Seg 21	-1091	738
15	COM3	1091	-578	39	Seg 22	-1091	578
16	VREG	1091	-418	40	Seg 23	-1091	418
17	Seg 0	1091	-258	41	Seg 24	-1091	258
18	Seg 1	1091	-98	42	Seg 25	-1091	98
19	Seg 2	1091	63	43	Seg 26	-1091	-63
20	Seg 3	1091	224	44	Seg 27	-1091	-223
21	Seg 4	1091	383	45	Seg 28	-1091	-383
22	Seg 5	1091	543	46	Seg 29	-1091	-543
23	Seg 6	1091	703	47	Seg 30	-1091	-703
24	Seg 7	1091	863	48	Seg 31	-1091	-863

Origin: Center of the chip
Chip size: 2,500 × 2,500

PINOUT (SED1510F0C)



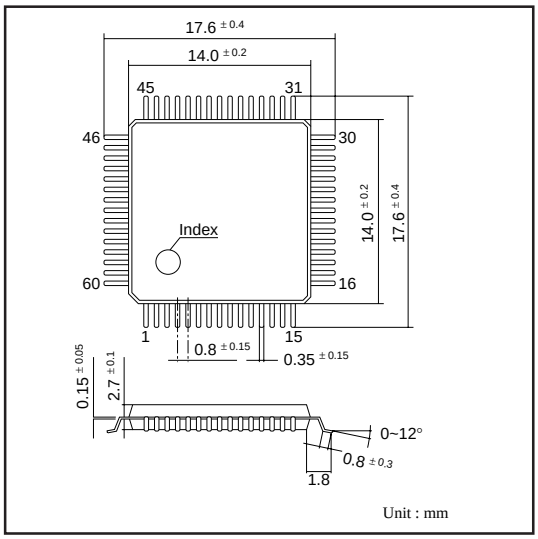
(SED1510F0E)



PIN DESCRIPTION

Number	Name	Descrlption
1	OSC1	Oscillator feedback resistor connection or external clock input
2	OSC2	Oscillator feedback resistor connection
3	V1	LCD driver voltage monitoring outputs
4	V2	
5	V3	LCD driver supply voltage
6	VSS	Negative supply
7	VDD	Positive supply
8	CK	Serial data clock input
9	SI	Serial data input
10	$\overline{CS}$	Active-LOW chip select input (SED1510 only)
11	C/$\overline{D}$	Command/data select input (SED1510 only)
12 to 15	COM0 to COM3	LCD common driver outputs
16	VREG	Regulated voltage monitor output
17 to 48	SEG0 to SEG31	LCD segment driver outputs

PIN ASSIGNMENT



No.	Name	No.	Name	No.	Name
1	N.C.	21	Seg0	41	Seg16
2	OSC1	22	Seg1	42	Seg17
3	OCS2	23	N.C.	43	Seg18
4	V1	24	Seg2	44	Seg19
5	V2	25	Seg3	45	N.C.
6	V3	26	Seg4	46	N.C.
7	VSS	27	Seg5	47	Seg20
8	N.C.	28	Seg6	48	Seg21
9	VDD	29	Seg7	49	Seg22
10	CK	30	N.C.	50	Seg23
11	$\overline{SI}$	31	N.C.	51	Seg24
12	$\overline{CS}$	32	Seg8	52	Seg25
13	C/$\overline{D}$	33	Seg9	53	N.C.
14	COM0	34	Seg10	54	Seg26
15	N.C.	35	Seg11	55	Seg27
16	N.C.	36	Seg12	56	Seg28
17	COM1	37	Seg13	57	Seg29
18	COM2	38	N.C.	58	Seg30
19	COM3	39	Seg14	59	Seg31
20	VREG	40	Seg15	60	N.C.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–7.0 to 0.3	V
LCD supply voltage range	V_3	–7.0 to 0.3	V
Input voltage range	V_I	V_{SS} –0.3 to 0.3	V
Output voltage range	V_O	V_{SS} –0.3 to 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opg}	–20 to 75	deg.C
Storage temperature range	T_{stg}	–65 to 150	deg.C
Soldering temperature (10 sec at leads)	T_{sol}	260	deg.C
Heat resistance		400 • 10	°C•Min

Note: All voltages shown are specified on a V_{DD} = 0 V basis.

DC Electrical Characteristics

V_{DD} = 0V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 deg.C unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Supply voltage	V_{SS}		–6.0	—	–0.9	V
LCD supply voltages	V_1		—	1/3 × V3	—	V
	V_2		—	2/3 × V3	—	
	V_3		–6.0	—	–1.8	
Quiescent supply current	I_{DDQ}	V_{SS} = –6.0 V, V_I = V_{DD}	—	0.05	1.0	µA
Supply current	I_{DD1}	Display mode, R_f = 680 KΩ, V_{SS} = –5.0 V	—	20.0	30.0	µA
	I_{DD2}	Input mode, V_{SS} = –5.0 V, f_{ck} = 200 kHz	—	100	250	
LOW-level input voltage	V_{IL}		V_{SS}	—	0.8 V_{SS}	V
HIGH-level input voltage	V_{IH}		0.2 V_{SS}	—	V_{DD}	V
Input leakage current	I_{LI}	$V_{SS} \le V_I \le V_{DD}$	—	0.05	2.0	µA
SEG0 to SEG31 and COM0 to COM3 LOW-level output voltage	V_{OL}	I_{OL} = 0.1 mA	—	—	V_{SS}+ 0.4	V
SEG0 to SEG31 and COM0 to COM3 HIGH-level output voltage	V_{OH}	I_{OH} = –0.1 mA	–0.4	—	—	V
Output leakage current	I_{LO}	$V_{SS} \le V_O \le V_{DD}$	—	0.05	5.0	µA
Oscillator frequency	f_{OSC}	V_{SS} = –0.5 V, R_f = 680 ±2% kΩ	—	18	—	kHz
		V_{SS} = –3.0 V, R_f =680 ±2% kΩ	—	16	—	
SEG0 to SEG31 and COM0 to COM3 ON resistance *1	R_{ON}	V_3 = –5.0 V, I ΔVON I = 0.1 V, Ta = 25 deg C	—	5.0	7.5	kΩ
		V_3 = –0.3 V, I ΔVON I = 0.1 V, Ta = 25 deg.C	—	10.0	50.	
Oscillation start time *2	T_{STA}		—	—	100	ns

*1 The internal power impedance is not included in the LCD driver on resistance (R_{ON}).

*2 This indicates the time until the timing generating circuit (CR oscillating circuit) starts oscillating and SI/CK input can be accepted after SED1511 power on.

AC Electrical Characteristics

V_{DD} = 0 V, V_{SS} = –5.0 ±0.5 V, Ta = –20 to 75 deg. C

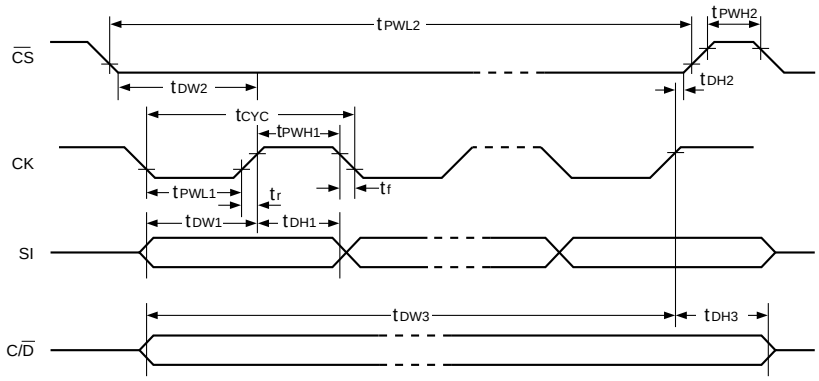
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		900	—	—	ns
CK LOW-level pulsewidth	t_{PWL1}		400	—	—	ns
CK HIGH-level pulsewidth	t_{PWH1}		400	—	—	ns
SI to CK setup time	t_{DW1}		100	—	—	ns
CK to SI hold time	t_{DH1}		200	—	—	ns
$\overline{CS}$ LOW-level puisewidth *2	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	7200*1	—	—	ns
$\overline{CS}$ HIGH-level pulsewidth *2	t_{PWH2}		400	—	—	ns
$\overline{CS}$ to CK setup time *2	t_{DW2}	Referenced to the rising edge of the first CK cycle.	100	—	—	ns
CK to $\overline{CS}$ hold time *2	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	200	—	—	ns
C/$\overline{D}$ to CK setup time *2	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	9	—	—	µs
CK to C/$\overline{D}$ hold time *2	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	1	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

*1 $t_{CYC} \times 8$ *2 SED1510 only

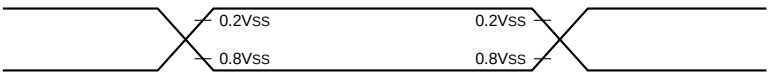
V_{DD} = 0 V, V_{SS} = –6.0 to –1.5 V, Ta = –20 to 75 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CK period	t_{CYC}		10	—	—	µs
CK LOW-level puisewidth	t_{PWL1}		4.5	—	—	µs
CK HIGH-level pulsewidth	t_{PWH1}		4.5	—	—	µs
SI to CK setup time	t_{DW1}		1.2	—	—	µs
CK to SI hold time	t_{DH1}		2.3	—	—	µs
$\overline{CS}$ LOW-level pulsewidth *2	t_{PWL2}	$t_{PWL2} \geq 8t_{CYC}$	80*1	—	—	µs
$\overline{CS}$ HIGH-level pulsewidth *2	t_{PWH2}		4.5	—	—	µs
$\overline{CS}$ to CK setup time *2	t_{DW2}	Referenced to the rising edge of the first CK cycle.	1.2	—	—	µs
CK to $\overline{CS}$ hold time *2	t_{DH2}	Referenced to the rising edge of the eighth CK cycle.	2.3	—	—	µs
C/$\overline{D}$ to CK setup time *2	t_{DW3}	Referenced to the rising edge of the eighth CK cycle.	100	—	—	µs
CK to C/$\overline{D}$ hold time *2	t_{DH3}	Referenced to the rising edge of the eighth CK cycle.	11	—	—	µs
Rise time	t_r		—	—	50	ns
Fall time	t_f		—	—	50	ns

*1 $t_{CYC} \times 8$ *2 SED1510 only



Timing measurement

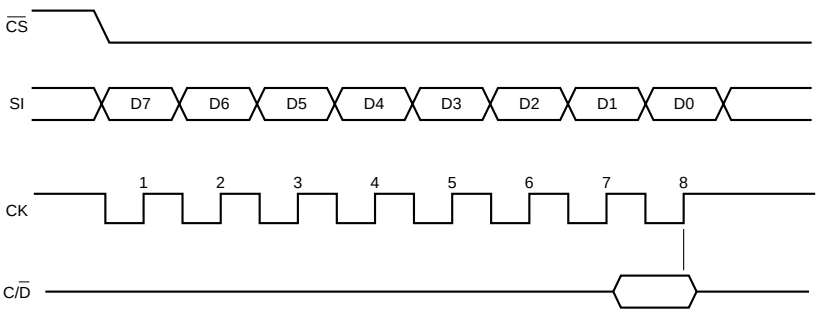


FUNCTIONAL DESCRIPTION

Command/Data Register

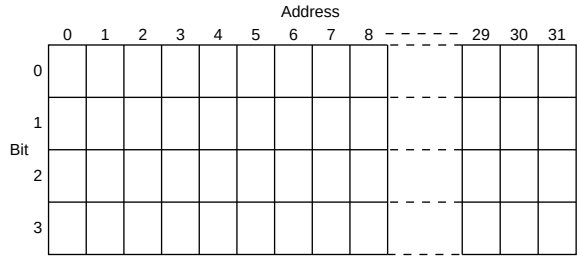
The command/data register comprises an 8-bit shift register and a 3-bit CK counter. The counter is reset and re-enabled on the falling edge of $\overline{CS}$. In the SED1511, SI input can be performed any time. The CK counter is initialized when the built-in timing generating circuit (CR oscillating circuit) starts oscillating. The counter is incremented, and the serial input data is shifted into the register on the rising edge of CK. The data is input msb-first as shown in the following figure.

C/$\overline{D}$ is sampled, and the register data is latched into either the display data memory or the command decoder on every eighth rising edge of CK. C/$\overline{D}$ should be set HIGH when a command is input, and LOW, when display data is input.

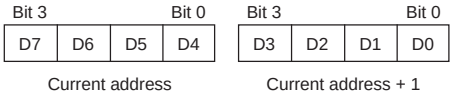


Display Data Memory

The format of the 32 × 4-bit memory is shown in the following figure.



Each 8-bit display data byte loaded from the command/data register is stored in two consecutive addresses as shown in the following figure. The upper four bits are stored at the location specified by the address counter, and the lower four bits, at the next location. The address counter is automatically incremented by two.



A single 4-bit word can be written to memory using the Data Memory Write command as shown in the following figure. The lower four bits are stored at the location specified by the address counter. The address counter is automatically incremented by one.

specified by the address counter. The address counter is automatically incremented by one.

1	0	0	X	D3	D2	D1	D0

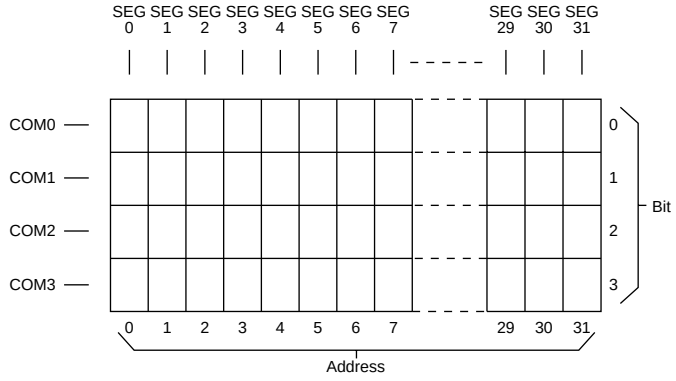
Note

× = don't care

The display data memory address of the SED1511 is automatically incremented by 2 when 8-bit display data is stored.

Address 0 is automatically set when the built-in timing generating circuit (CR oscillating circuit) starts oscillating after power on.

Display memory data is output on SEG0 to SEG31 in synchronization with the COM0 to COM3 output scan. The correspondence between memory location and display position is shown in the following figure. When the data is 0, the segment is OFF, and when 1, ON.

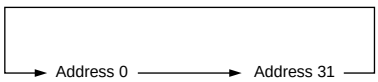


Address Counter

The 5-bit address counter is used to address display data memory. It is set by the Address Set command, and automatically increments when data is stored in the memory. The counter automatically resets to 0 when it increments past 31 as shown in the following figure.

◊ SED1511; after the power supply is turned on, the enclosed timing generating circuit (CR oscillating circait) starts oscillating and the address is automatically set to 0.

◊ SED1511; after the displayed data 8bit is stored, the set address automatically goes to +2.

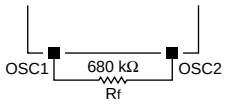


Address Decoder

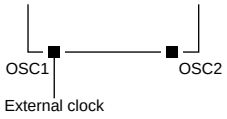
The address decoder sets addresses 0 to 31 of the display data memory where the display data of address counter is written.

Timing Generator

A low-power oscillator can be constructed using an external feedback resistor as shown in the following figure.



Alternatively, an 18 kHz external clock can be input on OSC1, and OSC2 left open, as shown in the following figure.



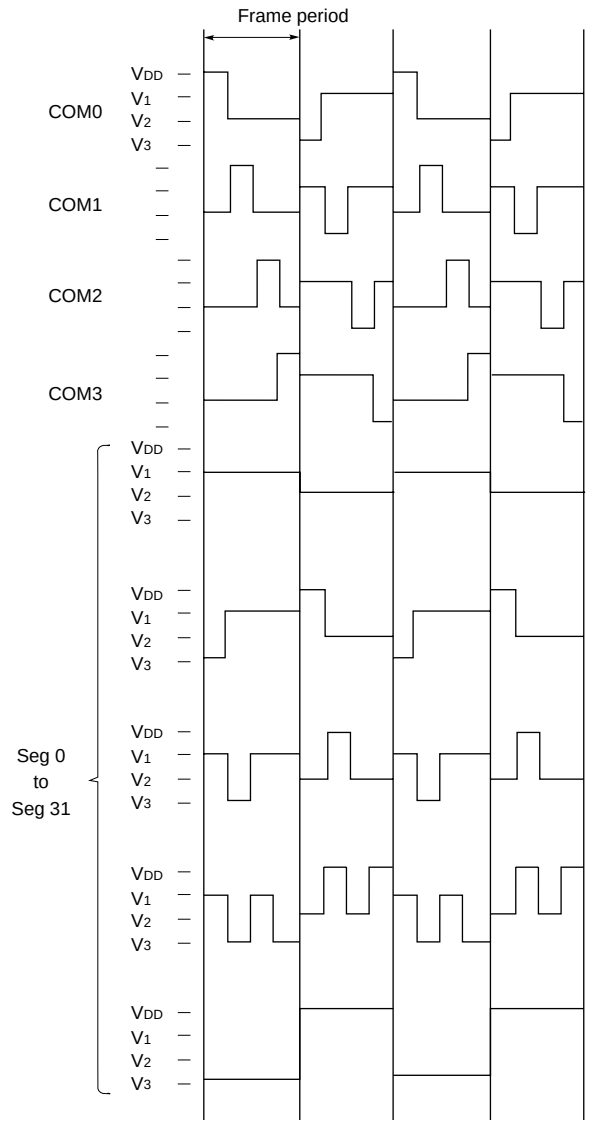
Common Counter

The timing generator clock signal is frequency-divided by the common counter to generate both the common drive timing and the alternating frame timing.

Segment and Common Drivers

The 32 segment drivers and the four common drivers are 4-level outputs that switch between V_{DD} and the V1, V2 and V3 LCD driver voltage levels.

The output states are determined by the display data values and the common counter as shown in the following figure. The outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.



COM0	COM1	COM2	COM3	
0	0	0	0	All segments are OFF.
1	0	0	0	Segments connected to COM0 are ON.
0	1	0	0	Segments connected to COM1 are ON.
0	1	0	1	Segments connected to COM1 or COM3 are ON.
1	1	1	1	All segments are ON.

Commands

The SED1510F0C samples C/$\overline{D}$ on every eighth rising edge of CK. If C/$\overline{D}$ is HIGH, the command/data register contents are latched into the command decoder. The command decoder executes the following six commands.

Address Set

Set the address counter to the value specified by D0 to D4.

0	0	0	D4	D3	D2	D1	D0

Display ON

Turn all LCD segments ON. The display memory data is not affected.

0	0	1	×	×	×	×	×

Note: × = don't care

Display OFF

Turn all LCD segments OFF. The display memory data is not affected.

0	1	0	×	×	×	×	×

Note: × = don't care

Display Start

Return to normal display mode. The display memory data is output to the display.

0	1	1	×	×	×	×	×

Note: × = don't care

Memory Write

Store the data D0 to D3 at the location specified by the address counter. The address counter is automatically incremented by one. The other display memory locations are not affected.

1	0	0	×	D3	D2	D1	D0

Note: × = don't care

Reset

Reset the SED1510F0C. The SED1510F0C then enters normal operating mode, and the display turns OFF.

1	1	0	×	×	×	×	×

Note: × = don't care

APPLICATION NOTE

Supply Voltages

In addition to V_{DD}, there are three LCD supply voltages: V_1 , V_2 and V_3. V_3 is supplied externally, whereas V_1 and V_2 are generated internally. V_1, V_2 and V_3 are given by the following equations.

$V_1 = V_{DD} - 1/3V_{LCD}$

$V_2 = V_{DD} - 2/3V_{LCD}$

$V_3 = V_{DD} - V_{LCD}$

where V_{LCD} is the LCD drive voltage. The voltages must be such that

$V_{DD} \geq V_1 \geq V_2 \geq V_3$

LCD supply voltage connections when the LCD drive supply is connected to V_{SS} are shown in figure 1, and the connections when the drive supply is independent of V_{SS}, in Figure 2.

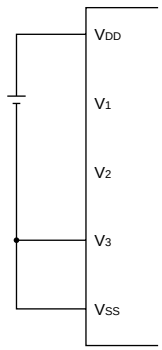


Figure 1. LCD drive supply connected to V_{SS}

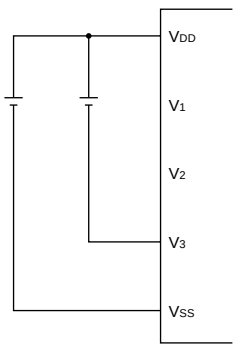
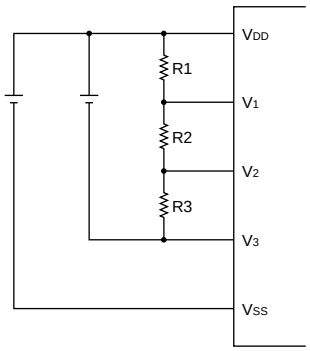


Figure 2. LCD drive supply not connected to V_{SS}

When there is a lot of distortion in the LCD drive waveforms, connect bleeder resistors as shown in the following figure.



2. SED1520 Series

Contents

OVERVIEW

The SED1520 family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The SED1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The SED1520 which is able to drive two lines of twelve characters each.
- The SED1521 which is able to drive 80 segments for extention.
- The SED1522 which is able to drive one line of thirteen characters each.

FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 µW at 2 kHz external clock
- Wide range of supply voltages
  V_{DD} – V_{SS}: –2.4 to –7.0 V
  V_{DD} – V5: –3.5 to –13.0 V
- Low-power CMOS

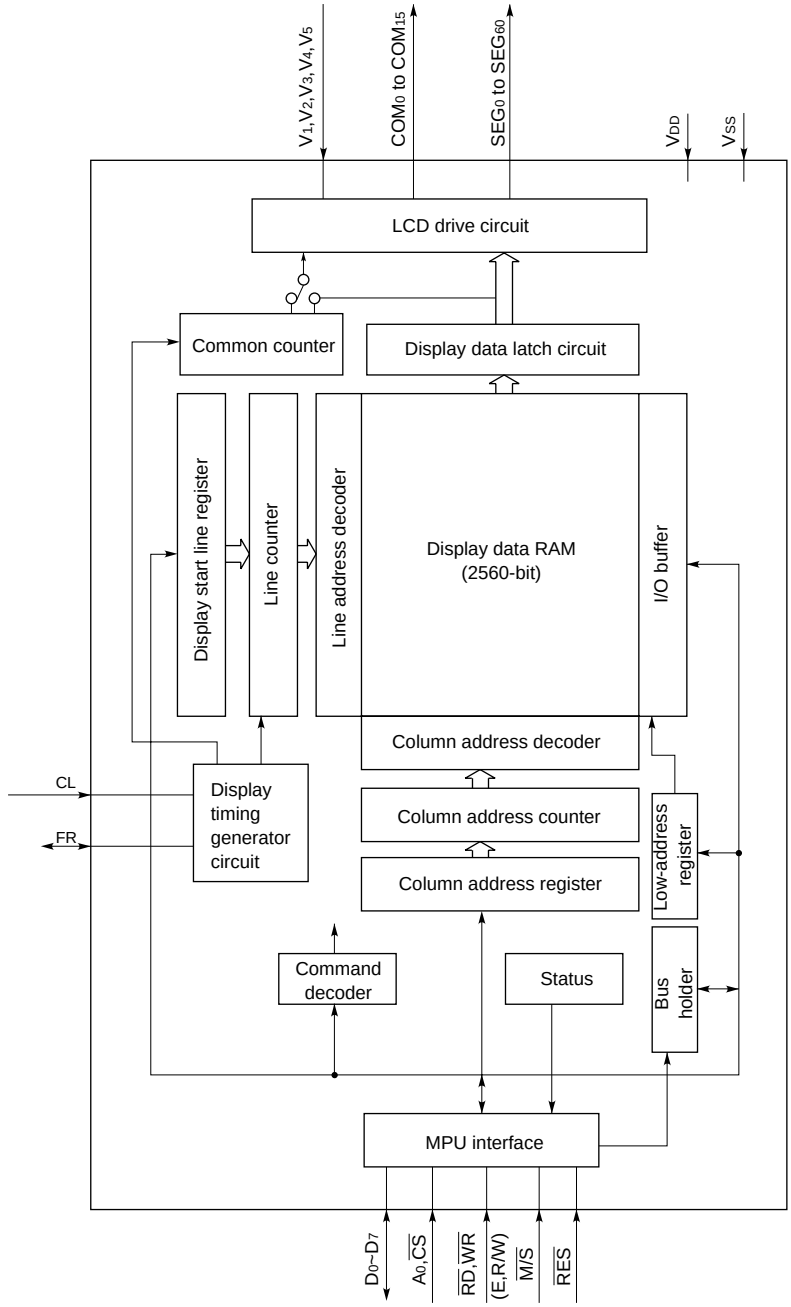
Line-up

Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
SED1520∗0∗	18 kHz	18 kHz	SED1520∗0∗, SED1521∗0∗	61	16	1/16, 1/32
SED1521∗0∗	—	18 kHz	SED1520∗0∗, SED1522∗0∗	80	0	1/8 to 1/32
SED1522∗0∗	18 kHz	18 kHz	SED1522∗0∗, SED1521∗0∗	69	8	1/8, 1/16
SED1520∗A∗	—	2 kHz	SED1520∗A∗, SED1521∗A∗	61	16	1/16, 1/32
SED1521∗A∗	—	2 kHz	SED1520∗A∗, SED1522∗A∗	80	0	1/8 to 1/32
SED1522∗A∗	—	2 kHz	SED1522∗A∗, SED1521∗A∗	69	8	1/8, 1/16

- Package code (For example SED1520)
  SED1520T
  SED1520F∗∗: PKG ─┬─ SED1520F∗A (QFP5-100pin)
  └─ SED1520F∗C (QFP15-100pin)
  SED1520D∗∗: Chip ─┬─ SED1520D∗A (Al-pad)
  └─ SED1520D∗B (Au-bump)

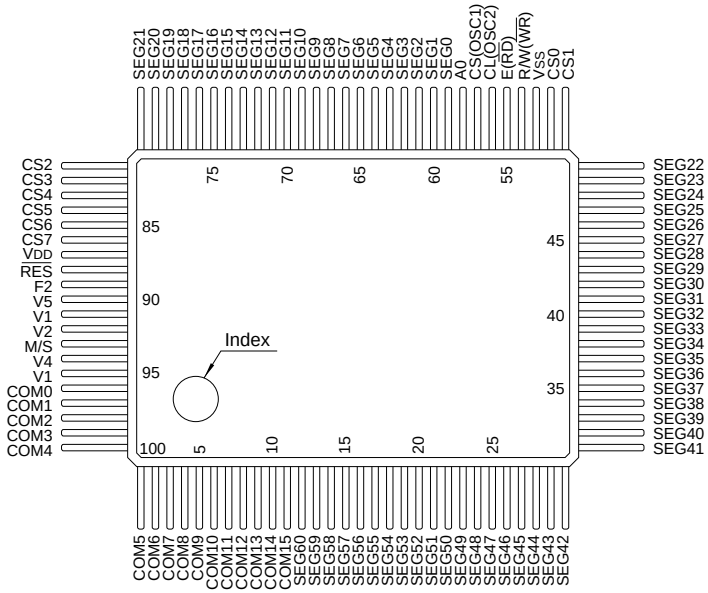
BLOCK DIAGRAM

An example of SED1520∗AA:

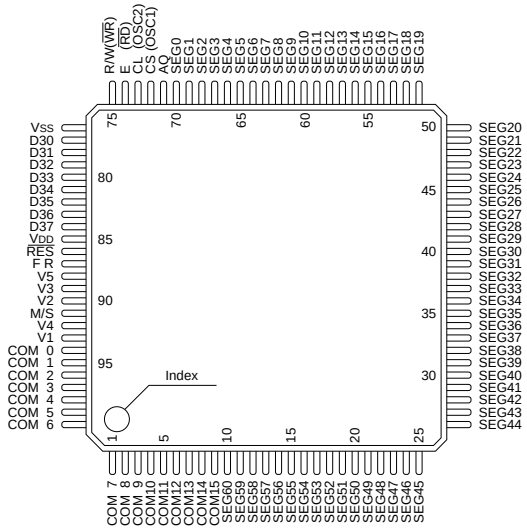


PACKAGE OUTLINE

QFP5



QFP15



Note: This is an example of SED1520F pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
SED1520F0A	OSC1	OSC2	COM0 to COM15*	M/S	V4	V1
SED1521F0A	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522F0A	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
SED1520FAA	CS	CL	COM0 to COM15*	M/S	V4	V1
SED1521FAA	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1522FAA	CS	CL	COM0 to 7, SEG68 to 61	M/S	V4	V1

SED1520: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.

SED1522: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

PAD

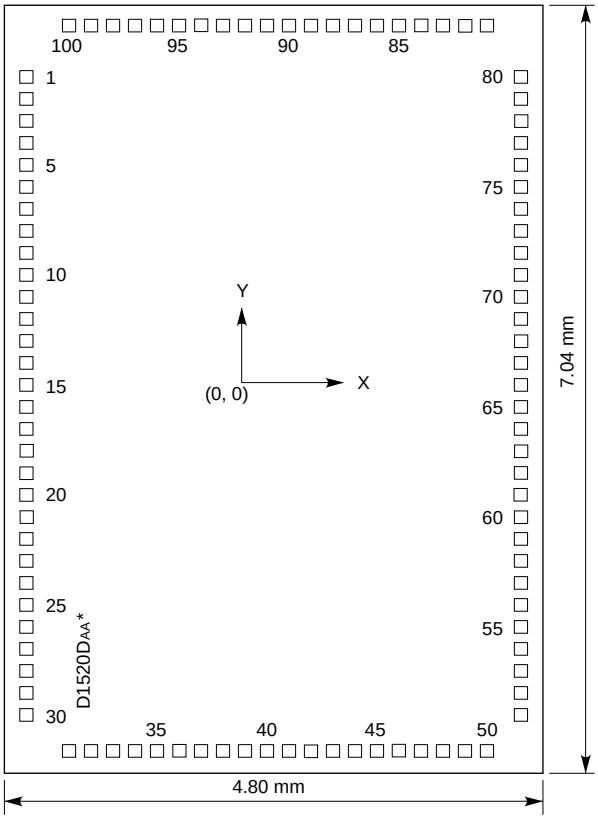
Pad Arrangement

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 µm

Chip specifications of gold bump package

Chip size: 4.80×7.04×0.525 mm
Bump pitch: 199 µm (Min.)
Bump height: 22.5 µm (Typ.)
Bump size: 132×111 µm (±20 µm) for mushroom model
116×92 µm (±4 µm) for vertical model



Note: An example of SED1520DAA die numbers is given. These numbers are the same as the bump package.

PAD ARRANGEMENT

An example of SED1520DA∗ pin names is given. The asterisk (∗) can be A for AL pad package or B for gold bump package.

SED1520DAB Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	CS	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V_5	2499	6884
91	V_3	2300	6884
92	V_2	2100	6884
93	M/S	1901	6884
94	V_4	1701	6884
95	V_1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

The other SED1520 series packages have the different pin names as shown.

Package/Pad No.	74	75	96 to 100, 1 to 11	93	94	95
SED1520D0*	OSC1	OSC2	COM0 to COM15 *	M/S	V_4	V_1
SED1522D0*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
SED1522DA*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
SED1521D0*	$\overline{CS}$	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
SED1521DA*	$\overline{CS}$	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

PIN DESCRIPTION

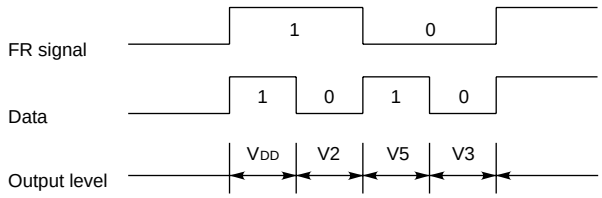
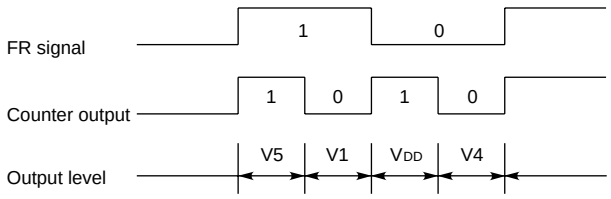
(1) Power Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⌐└┘⌐ the 68-series MPU is initialized, and when it goes ┘⌐└ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be ORed with the $\overline{CS}$ signals and entered.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active low. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator, this is used as an output pin of the oscillator amp and an Rf oscillator resistor is connected to it.
FR	Input/output. This is an I/P pin of LCD AC signals, and connected to the M terminal of common driver. I/O selection • Common oscillator built-in model: Output if M/S is 1; Input if M/S is 0. • Dedicate segment model: Input
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{DD}, V_2, V_3 and V_5 is selected by the combination of display RAM contents and RF signal. 
COMn	Output. The output pin for LCD common (low) driving. A single level of V_{DD}, V_1, V_4 and V_5 is selected by the combination of common counter output and RF signal. The slave LSI has the reverse common output scan sequence than the master LSI. 
M/S	Input. The master or slave LSI operation select pin for the SED1520 or SED1522. Connected to V_{DD} (to select the master LSI operation mode) or V_{SS} (to select the slave LSI operation mode). When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 ($\overline{CS}$), and OSC2 (CL) pins are changed.

	M/S	FR	COM output	OSC1	OSC2
SED1520F0A	V_{DD}	Output	COM0 to COM15	Input	Output
	V_{SS}	Input	COM31 to COM16	NC	Input
SED1522F0A	V_{DD}	Output	COM0 to COM7	Input	Output
	V_{SS}	Input	COM15 to COM8	NC	Input

* The slave driver has the reverse common output scan sequence than the master driver.

BLOCK DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type
   The SED1520 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).
   When the $\overline{CS}$ signal is high, the SED1520 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
Active low	68-series	↑	↑	↑	↑	↑
Active high	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

Data transfer

The SED1520 and SED1521 drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.
In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.
This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

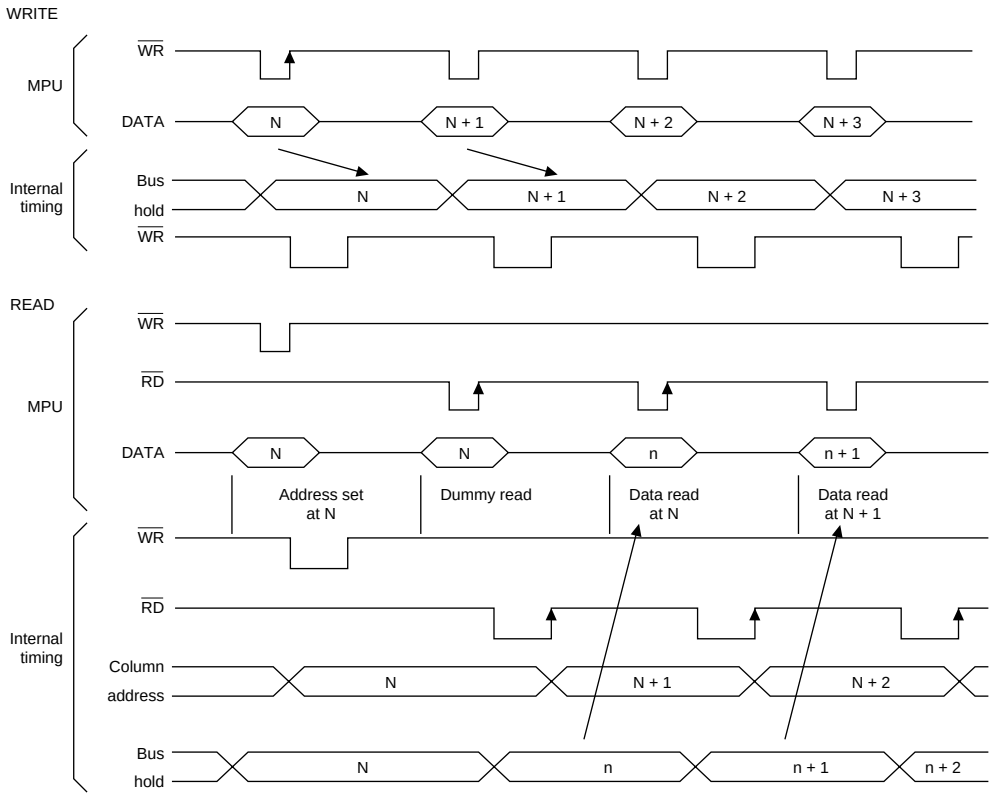


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

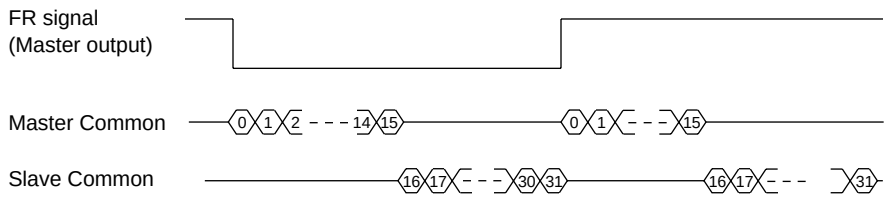
Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

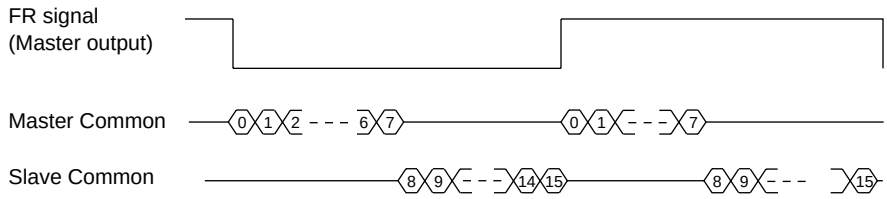
Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for SED1520) or 1/8 or 1/16 duty (for SED1522) can be selected by the Duty Select command. If the 1/32 duty is selected for the SED1520 and 1/16 duty is selected for the SED1522, the 1/32 and 1/16 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

SED1520



SED1522



Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

LCD Driver Circuit

The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

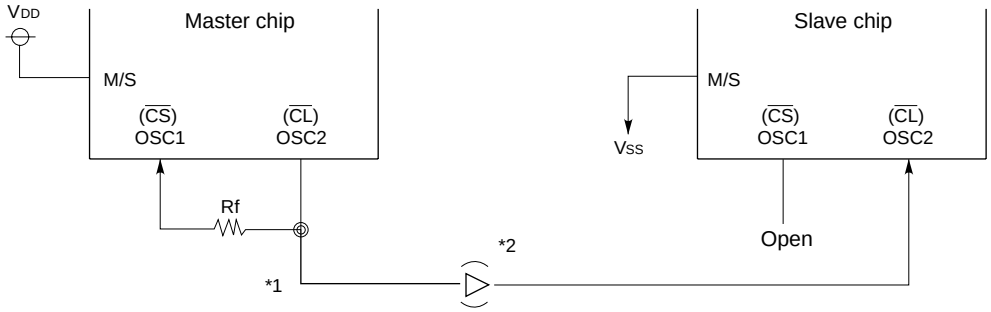
Display Timing Generator

This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. CL is used to lock the line counter to the system line scan rate. If a system uses both SED1520s or SED1522 and SED1521s they must have the same CL frequency rating.

Oscillator Circuit (SED1520*0A Only)

A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of SED1520 and SED1522 series models have a built-in oscillator and others use an external clock. This difference must be checked before use.
Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, enter the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

- MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.
*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave MPU chips.

- MPU driven with an external clock

Reset Circuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.

- Initialization status
  1. Display is off.
  2. Display start line register is set to line 1.
  3. Static drive is turned off.
  4. Column address counter is set to address 0.
  5. Page address register is set to page 3.
  6. 1/32 duty (SED1520) or 1/16 duty (SED1522) is selected.
  7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
  8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command is issued, initialization

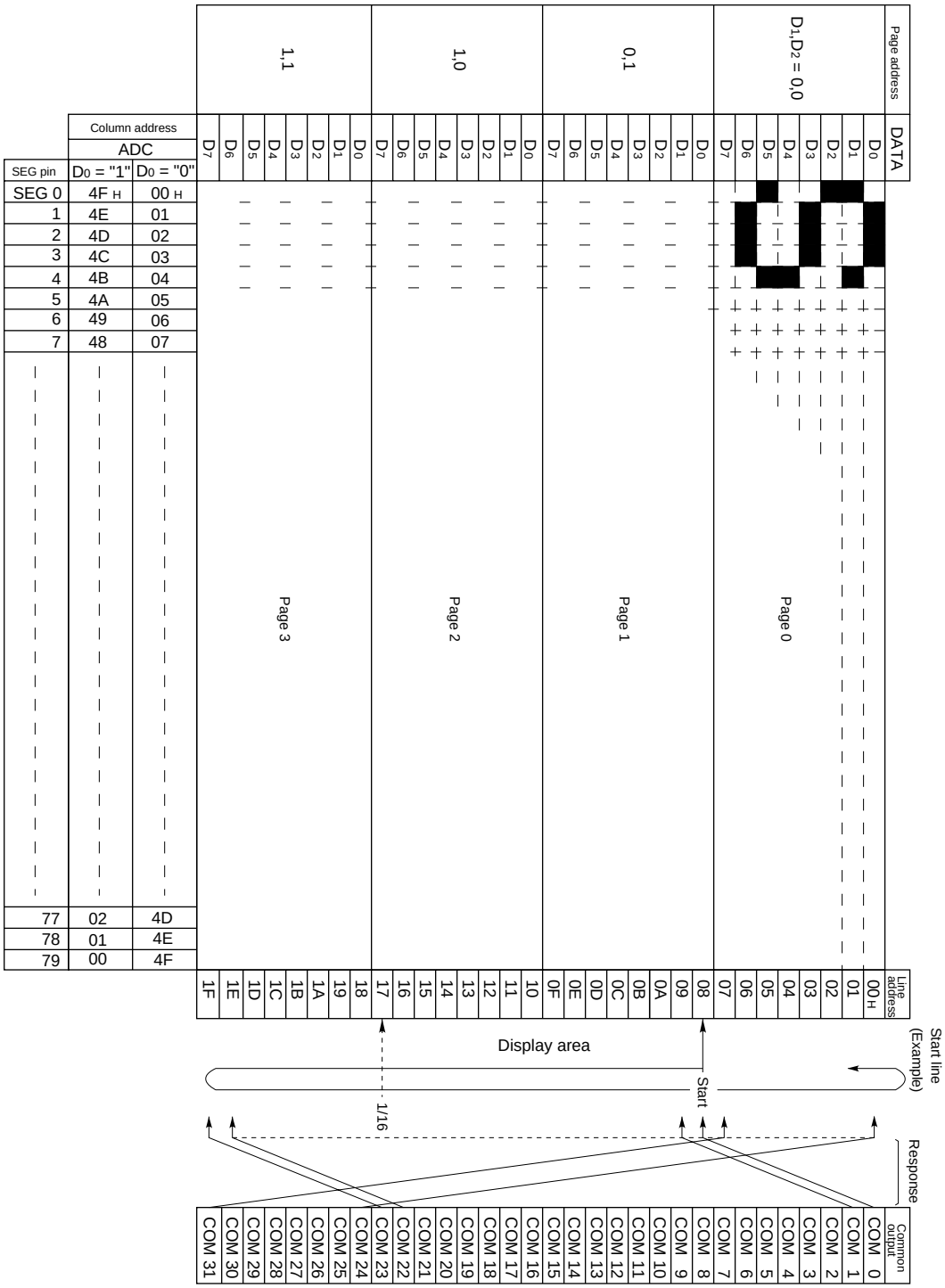


Figure 2 Display Data RAM Addressing

1/5 bias, 1/16 duty
1/6 bias, 1/32 duty

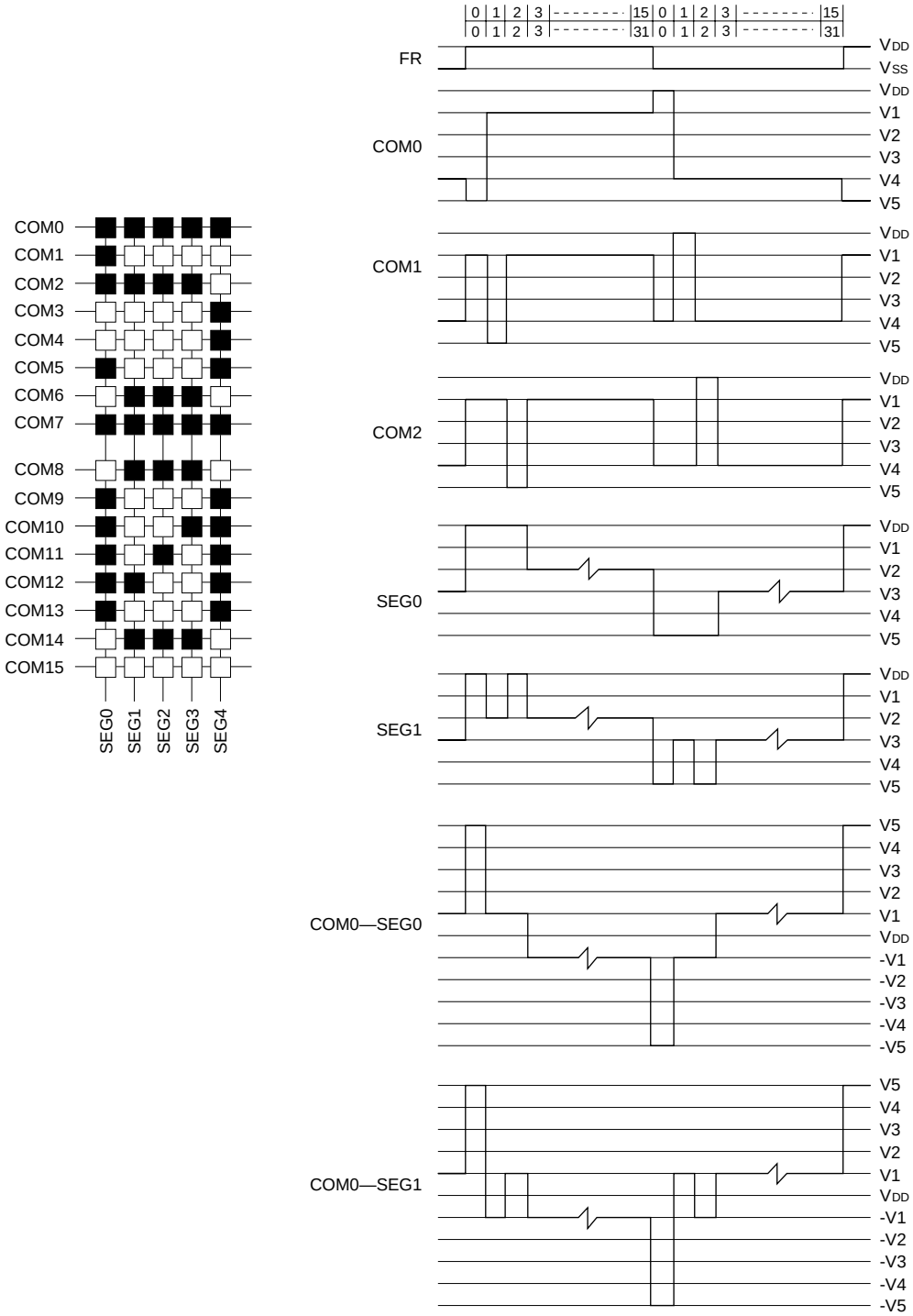


Figure 4 LCD drive waveforms example

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The SED1520 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

This command loads the display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

This command loads the page address register.

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the SED1520F and SED1522F. It is invalid for the SED1521F which performs passive operation. The duty cycle of the SED1521F is determined by the externally generated FR signal.

	SED1520	SED1522
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the SED1520F$_{0A}$, SED1522F$_{0A}$ (having a built-in oscillator) and the SED1521F$_{0A}$ continuously, set the duty as follows:

		SED1521F$_{0A}$
SED1520F$_{0A}$	1/32	1/32
	1/16	1/16
SED1522F$_{0A}$	1/16	1/32
	1/8	1/16

Read-Modify-Write

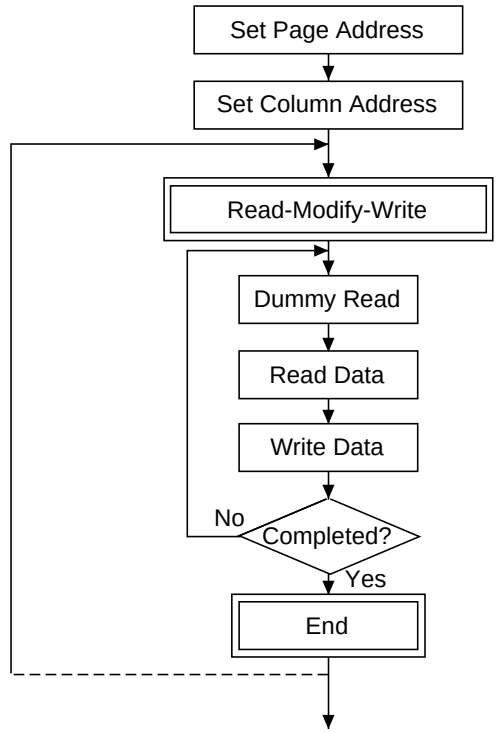
A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

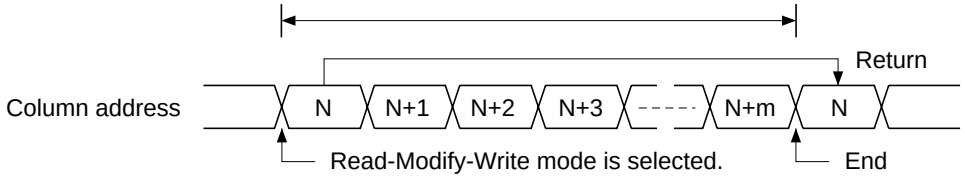
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

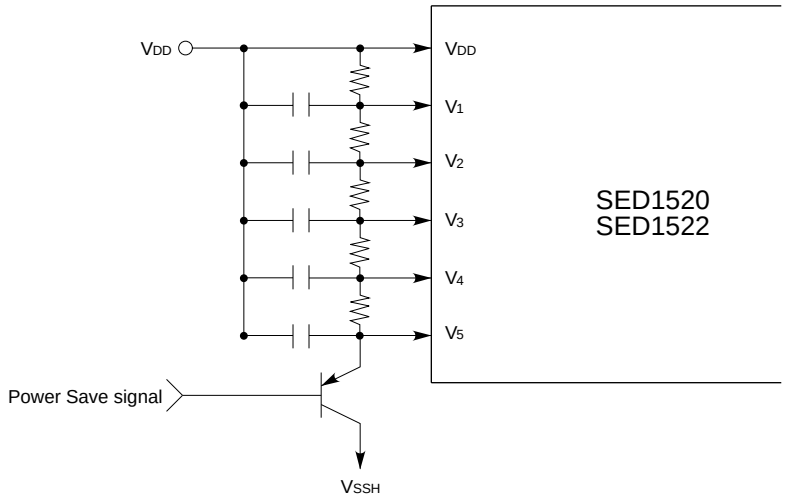
This command clears
- the display start line register.
- and set page address register to 3 page.

  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–8.0 to +0.3	V
Supply voltage (2)	V_5	–16.5 to +0.3	V
Supply voltage (3)	V_1, V_4, V_2, V_3	V5 to +0.3	V
Input voltage	V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	–40 to +85	deg. C
Storage temperature	T_{stg}	–65 to +150	deg. C
Soldering temperature time at lead	T_{sol}	260, 10	deg. C, sec

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_5			–13.0	—	–3.5	V	V_5 See note 10.
	Allowable				–13.0	—	—		
	Allowable	V_1, V_2			0.6×V_5	—	V_{DD}	V	V_1, V_2
	Allowable	V_3, V_4			V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2 & 3.
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		
		V_{IHT}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		See note 2 & 3.
		V_{IHC}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		
Low-level input voltage		V_{ILT}			V_{SS}		V_{SS}+0.8		See note 2 & 3.
		V_{ILC}			V_{SS}		0.8×V_{SS}		
		V_{ILT}	V_{SS} = –3 V		V_{SS}		0.85×V_{SS}		See note 2 & 3.
		V_{ILC}	V_{SS} = –3 V		V_{SS}		0.8×V_{SS}		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	OSC2 See note 4 & 5.
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		
		V_{OHT}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}			V	See note 4 & 5. OSC2
		V_{OHC1}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}				
		V_{OHC2}	V_{SS} = –3 V	I_{OH} = –50 µA	0.2×V_{SS}				

(continued)

DC Characteristics (Cont'd)

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Low-level output voltage	V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	OSC2 See note 4 & 5.
	V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		
	V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		
	V_{OLT}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}	V	See note 4 & 5. OSC2
	V_{OLC1}	V_{SS} = –3 V	I_{OL} = 2 mA			0.8×V_{SS}		
	V_{OLC2}	V_{SS} = –3 V	I_{OL} = 50 µA			0.8×V_{SS}		
Input leakage current	I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current	I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistance	R_{ON}	Ta = 25 deg. C	V_5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V_5 = –3.5 V	—	10.0	50.0		
Static current dissipation	I_{DDQ}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	I_{DD} (1)	During display V_5 = –5.0 V	f_{CL} = 2 kHz	—	2.0	5.0	µA	V_{DD} See note 12, 13 & 14.
			R_f = 1 MΩ	—	9.5	15.0		
			f_{CL} = 18 kHz	—	5.0	10.0		
		During display V_5 = –5 V V_{SS} = –3 V	f_{CL} = 2 kHz		1.5	4.5	µA	V_{DD} See note 12 & 13.
			Rf = 1 MΩ		6.0	12.0		
	I_{DD} (2)	During access t_{cyc} = 200 kHz		—	300	500	µA	See note 8.
		V_{SS} = –3V, During access t_{cyc} = 200 kHz			150	300		
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	R_f = 1.0 MΩ ±2%, V_{SS} = –5.0 V		15	18	21	kHz	See note 9.
		R_f = 1.0 MΩ ±2%, V_{SS} = –3.0 V		11	16	21		
Reset time	t_R			1.0	—		µS	$\overline{RES}$ See note 15.

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write acess at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V_1, …, V_4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. SED1520*$_{A*}$ and SED1521*$_{A*}$ and SED1522*$_{A*}$ only. Does not include transient currents due to stray and panel capacitances.
13. SED1520*$_{0*}$ and SED1522*$_{0*}$ only. Does not include transient currents due to stray and panel capacitances.
14. SED1521*$_{0*}$ only. Does not include transient currents due to stray and panel capacitances.
15. t_R (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the SED1520 series enters the normal operation status after this t_R.

Relationship between f_{OSC}, f_{FR} and R_f, and operating bounds on V_{SS} and V5

*9 • Relationship between oscillation frequency, frames and Rf
(SED1520F0A), (SED1522F0A)

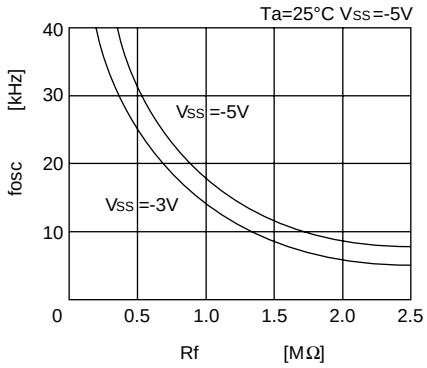


Figure 5 (a)

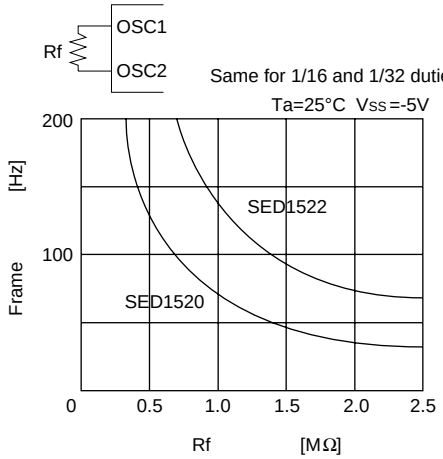


Figure 5 (b)

• Relationship between external clocks (f_{CL}) and frames
(SED1520FAA) , (SED1522FAA)

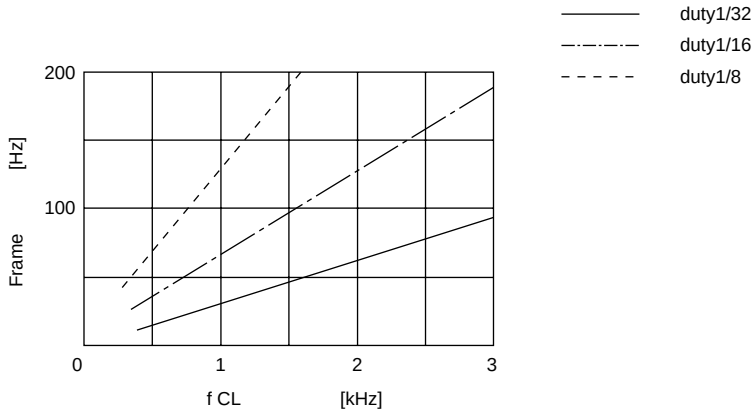


Figure 5 (c)

*10 • Operating voltage range of V_{SS} and V5 systems

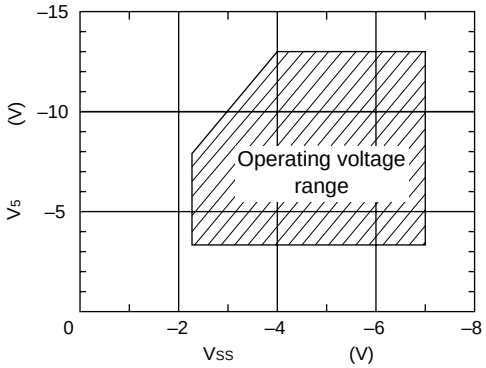
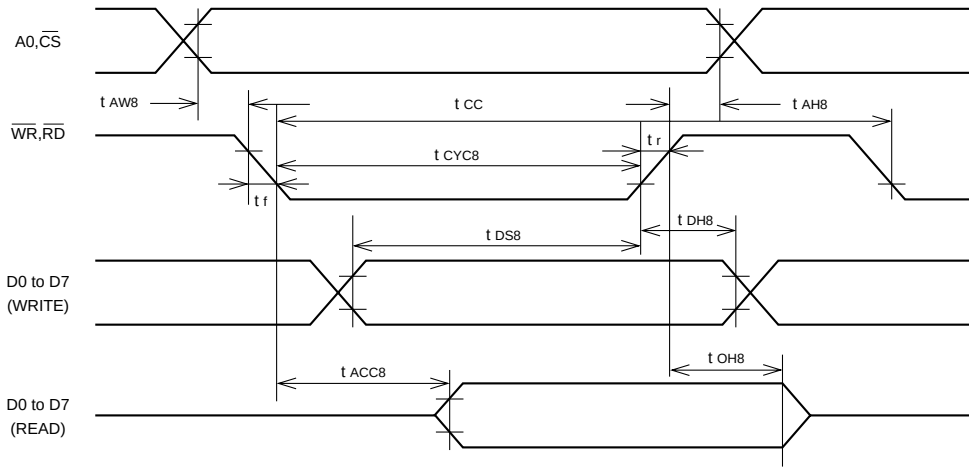


Figure 6

AC Characteristics

- MPU Bus Read/Write I (80-family MPU)



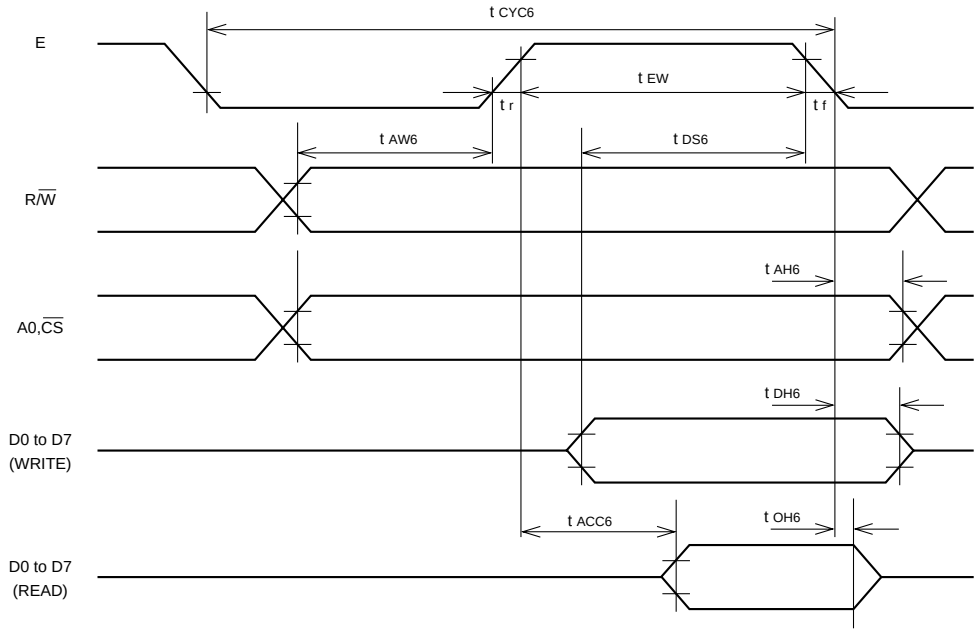
Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		10	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		20	—	ns	
System cycle time	t_{CYC8}		1000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	t_{CC}		200	—	ns	
Data setup time	t_{DS8}		80	—	ns	D0 to D7
Data hold time	t_{DH8}		10	—	ns	
$\overline{RD}$ access time	t_{ACC8}	C_L = 100 pF	—	90	ns	
Output disable time	t_{CH8}		10	60	ns	
Rise and fall time	t_r, t_f	—	—	15	ns	—

(V_{SS} = –2.7 to –4.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}	—	20	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		40	—	ns	
System cycle time	t_{CYC8}	—	2000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulse width	t_{CC}		400	—	ns	
Data setup time	t_{DS8}	—	160	—	ns	D0 to D7
Data hold time	t_{DH8}		20	—	ns	
$\overline{RD}$ access time	t_{ACC8}	C_L = 100 pF	—	180	ns	
Output disable time	t_{CH8}		20	120	ns	
Rise and fall time	t_r, t_f	—	—	15	ns	—

• MPU Bus Read/Write II (68-family MPU)



Ta = –20 to 75 deg. C, V_{SS} = –5 V ±10 unless stated otherwise

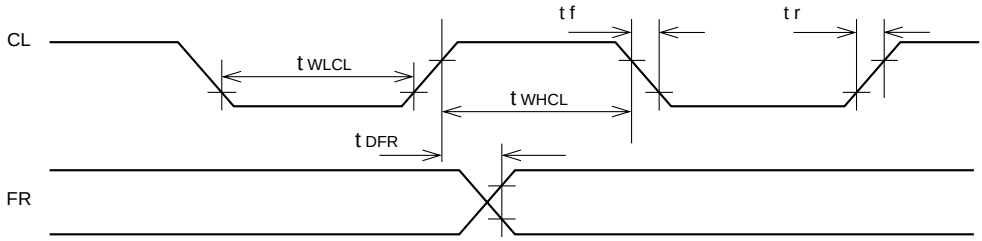
Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		t_{CYC6}		1000	—	ns	A0, CS, R/W
Address setup time		t_{AW6}		20	—	ns	
Address hold time		t_{AH6}		10	—	ns	
Data setup time		t_{DS6}		80	—	ns	D0 to D7
Data hold time		t_{DH6}		10	—	ns	
Output disable time		t_{OH6}	C_L = 100 pF	10	60	ns	
Access time		t_{ACC6}		—	90	ns	
Enable pulsewidth	Read	t_{EW}		100	—	ns	E
	Write			80	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

(V_{SS} = –2.7 to – 4.5 V, Ta = –20 to +75°C)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time*1		t_{CYC6}	—	2000	—	ns	A0, CS, R/W
Address setup time		t_{AW6}	—	40	—	ns	
Address hold time		t_{AH6}		20	—	ns	
Data setup time		t_{DS6}	—	160	—	ns	D0 to D7
Data hold time		t_{DH6}		20	—	ns	
Output disable time		t_{OH6}	C_L = 100 pF	20	120	ns	
Access time		t_{ACC6}		—	180	ns	
Enable pulse width	Read	t_{EW}	—	200	—	ns	E
	Write			160	—	ns	
Rise and fall time		t_r, t_f	—	—	15	ns	—

Notes: 1. t_{CYC6} is the cycle time of CS. E = H, not the cycle time of E.

- Display Control Signal Timing



Input

Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulsewidth	t_{WLCL}		35	—	—	µs	CL
High-level pulsewidth	t_{WHCL}		35	—	—	µs	
Rise time	t_r		—	30	150	ns	
Fall time	t_f		—	30	150	ns	
FR delay time	t_{DFR}		–2.0	0.2	2.0	µs	FR

V_{SS} = –2.7 to –4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	t_{WLCL}	—	70	—	—	µs	CL
High-level pulse width	t_{WHCL}	—	70	—	—	µs	
Rise time	t_r	—	—	60	300	ns	
Fall time	t_f	—	—	60	300	ns	
FR delay time	t_{DFR}	—	–4.0	0.4	4.0	µs	FR

Note: The listed input t_{DFR} applies to the SED1520 and SED1521 and SED1522 in slave mode.

Output

Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	C_L = 100 pF	—	0.2	0.4	µs	FR

V_{SS} = –2.7 to –4.5 V, Ta = –20 to +75°C

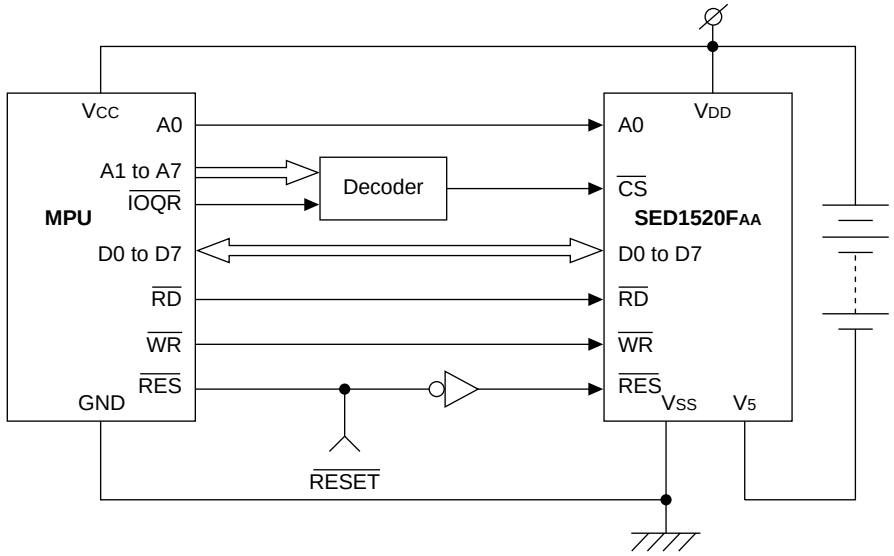
Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	C_L = 100 pF	—	0.4	0.8	µs	FR

Notes: 1. The listed output t_{DFR} applies to the SED1520 and SED1522 in master mode.

APPLICATION NOTES

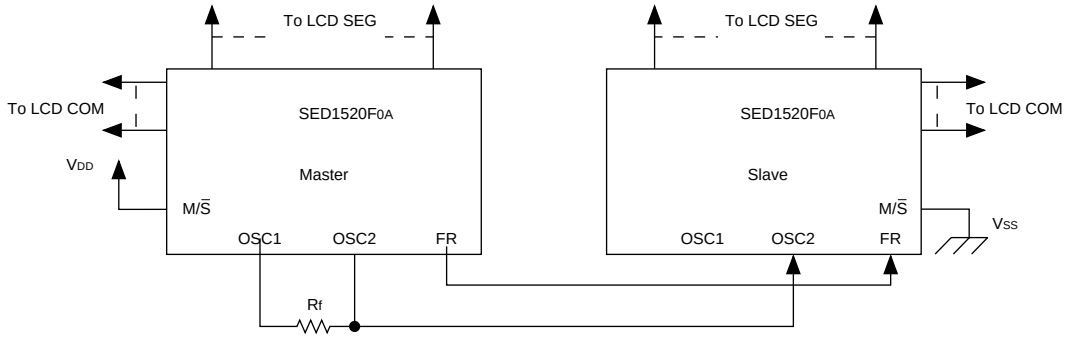
MPU Interface Configuration

80 Family MPU

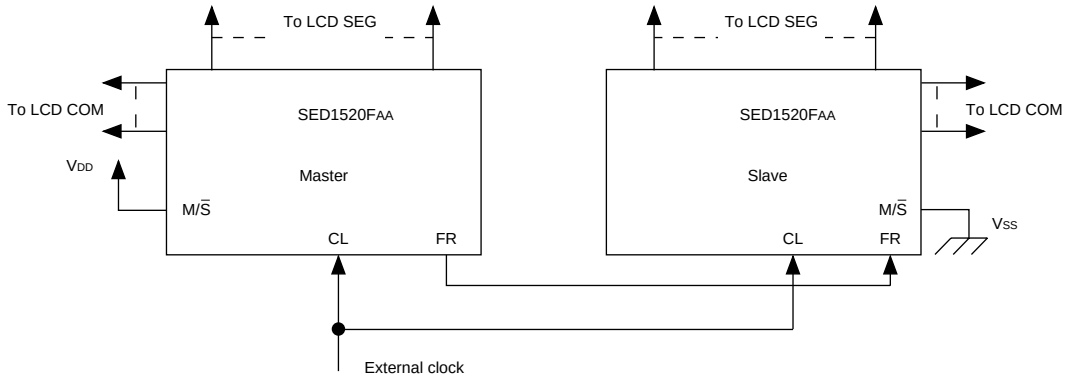


LCD Drive Interface Configuration

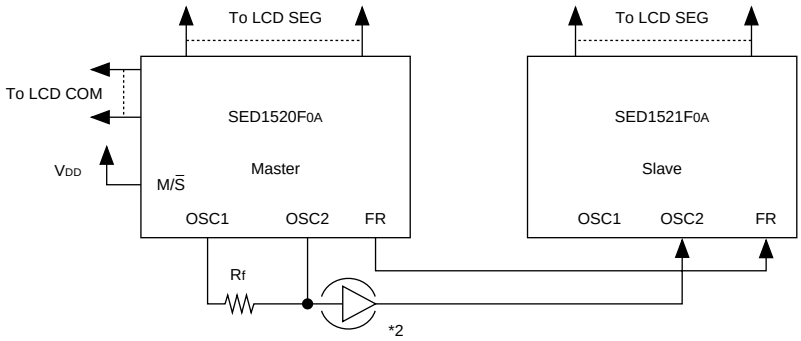
SED1520F0A–SED1520F0A
SED1522F0A–SED1522F0A



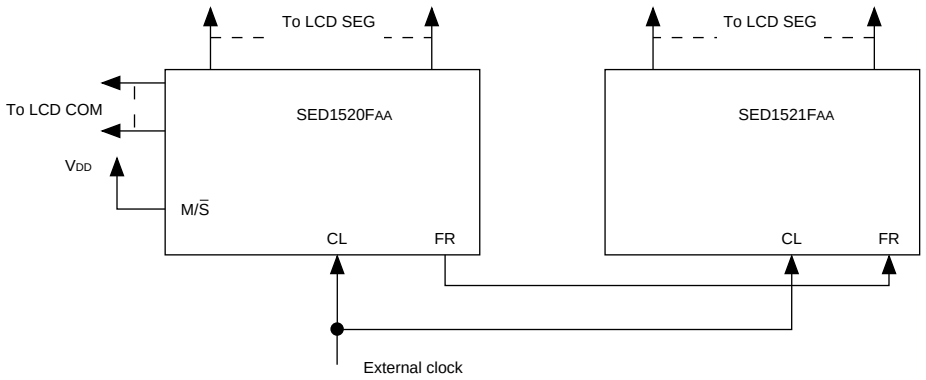
SED1520FAA–SED1520FAA
SED1522FAA–SED1522FAA



SED1520F0A)–SED1521F0A (See note 1)
SED1522F0A



SED1520FAA–SED1521FAA

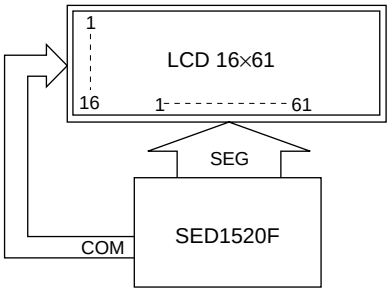


Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

LCD Panel Wiring Example (The full-dot LCD panel displays a character in 6×8 dots.)

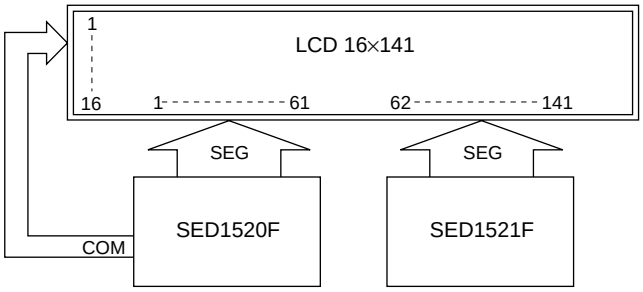
1/16 duty:

- 10 characters × 2 lines



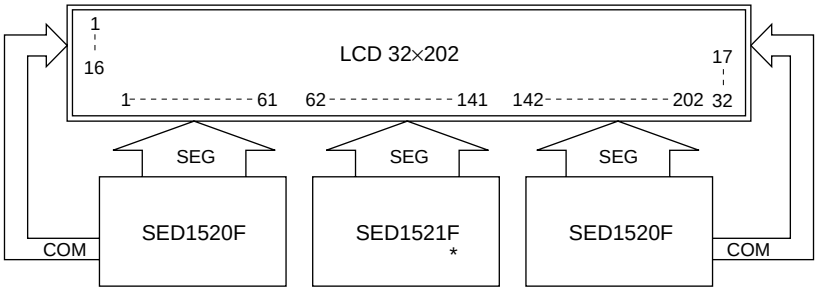
1/16 duty:

- 23 characters × 2 lines



1/32 duty:

- 33 characters × 4 lines

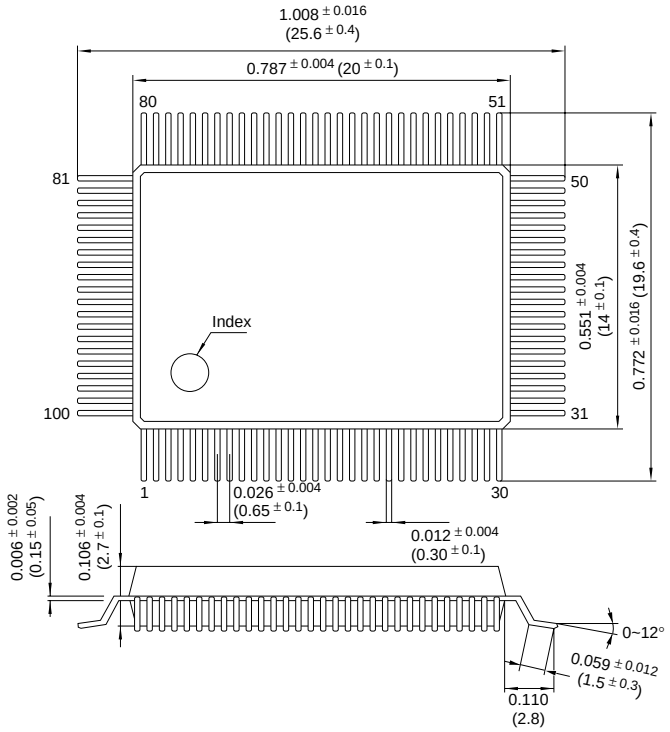


* The SED1521F can be omitted (the 32×122-dot display mode is selected).

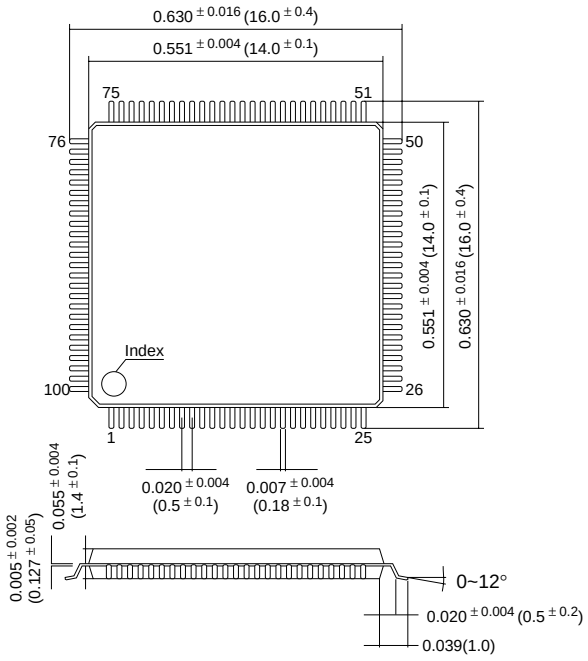
Note: A combination of AB or AA type chip (that uses internal clocks) and 0B or 0A type chip (that uses external clocks) is NOT allowed.

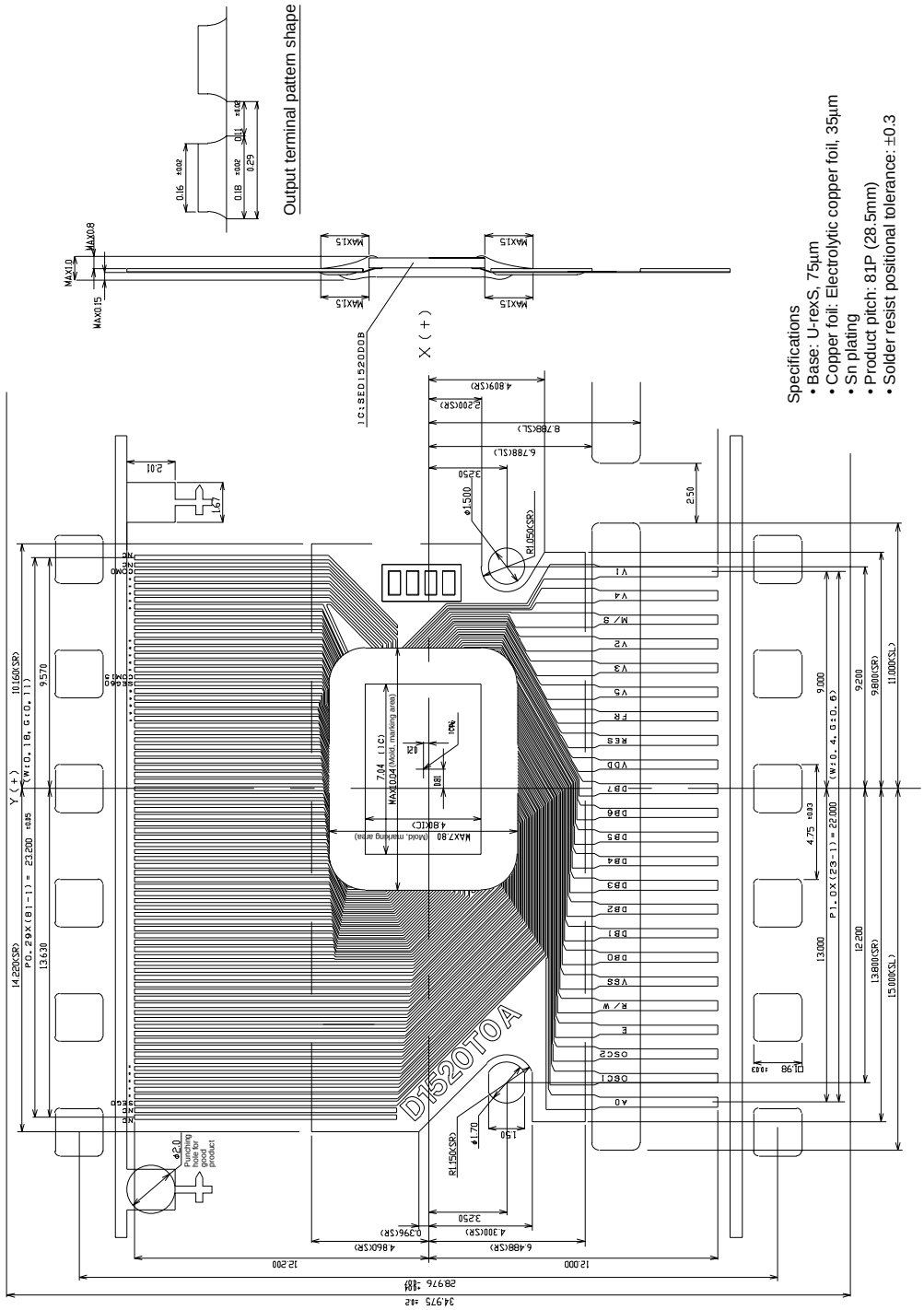
Package Dimensions

• Plastic QFP5–100 pin
Dimensions: inches (mm)



• Plastic QFP15–100 pin




Output terminal pattern shape
Specifications
• Base: U-rexS, 75µm
• Copper foil: Electrolytic copper foil, 35µm
• Sn plating
• Product pitch: 81P (28.5mm)
• Solder resist positional tolerance: ±0.3
D1520T0A
Y (+)
X (+)

3. SED152A Series

Contents

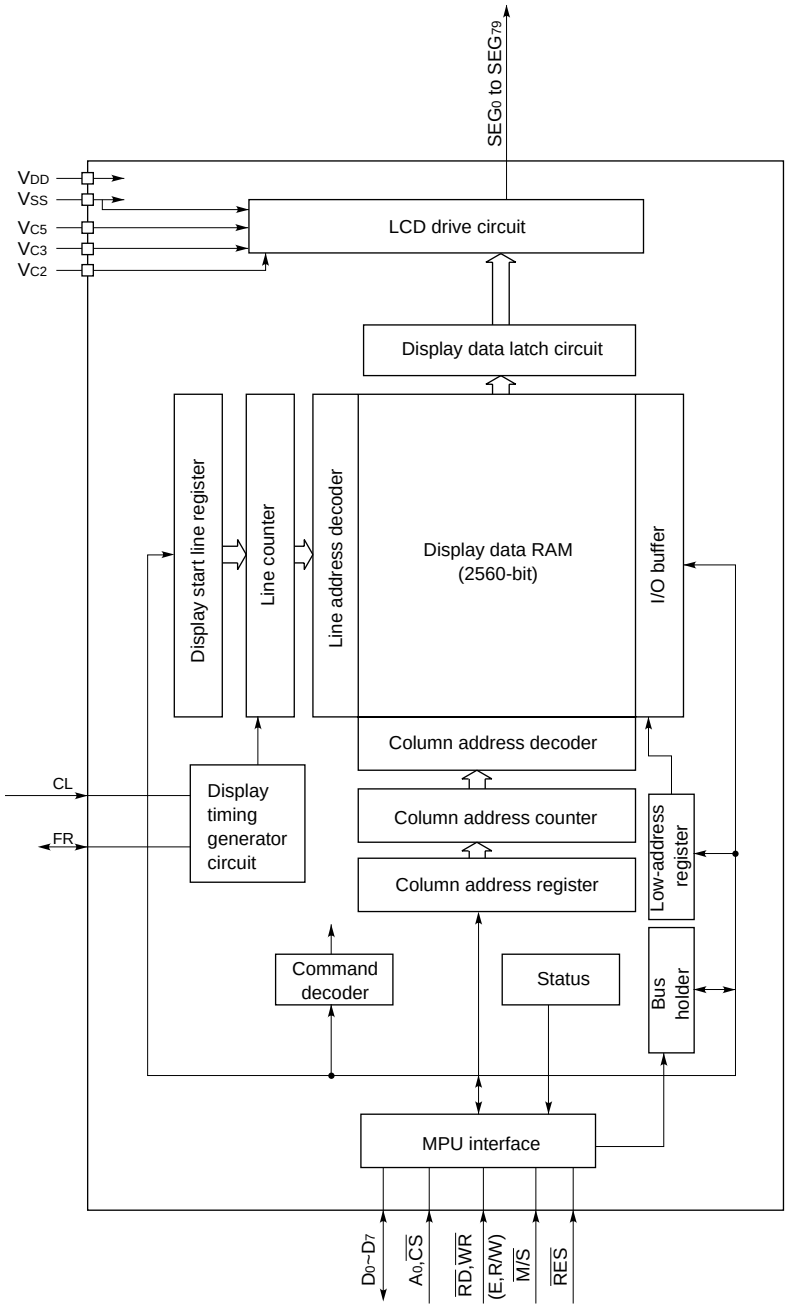
OVERVIEW

The SED152A family of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The SED1520 family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- 32 × 80 bit RAM
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  $V_{DD} - V_{SS}$: 2.4V to 6.0 V
  $V_{C5} - V_{SS}$: 3.5V to 6.0 V
- Low-power CMOS
- Al-pad chip

BLOCK DIAGRAM

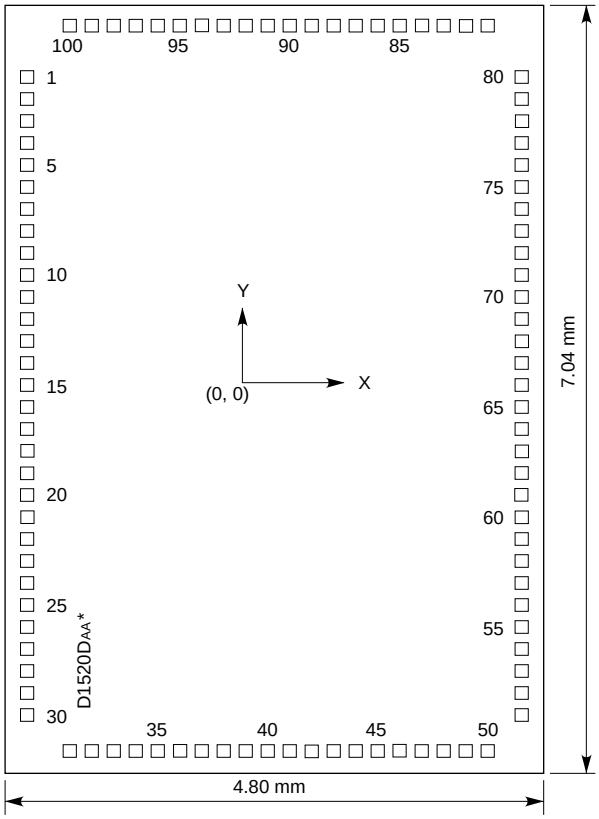


PAD

Pad Arrangement

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 µm



PAD ARRANGEMENT

SED152AD Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{CS}$	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{DD}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{SS}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	VC2	2499	6884
91	VC3	2300	6884
92	VC5	2100	6884
93	SEG79	1901	6884
94	SEG78	1701	6884
95	SEG77	1502	6884
96	SEG76	1302	6884
97	SEG75	1103	6884
98	SEG74	903	6884
99	SEG73	704	6884
100	SEG72	504	6884

PIN DESCRIPTION

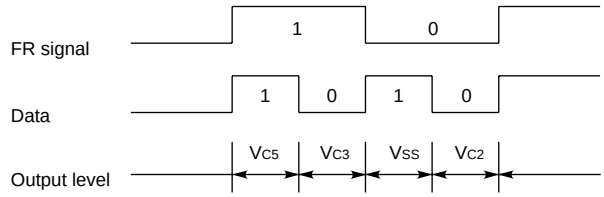
(1) Power Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_{C5}, V_{C3}, V_{C2}	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$

(2) System Bus Connection Pins

D7 to D0 *1	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. Low level (0): D0 to D7 are display control data. High level (1): D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⎺⎽⎺ the 68-series MPU is initialized, and when it goes ⎽⎺⎽ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. An address bus signal is usually decoded by use of chip select signal.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active low. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$) $\overline{WR}$ (R/$\overline{W}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is high) or write control signals (if low). • If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.
FR	Input. This is an input pin of LCD AC signals, and connected to the FR pin of common driver.
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{C5}, V_{C3}, V_{C2}, V_{SS} is selected by the combination of display RAM contents and FR signal. 

BLOCK DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type
   The SED152A series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low $\overline{RES}$ signal level after reset (see Table 1).
   When the $\overline{CS}$ signal is high, the SED152A series is disconnected from the MPU bus and set to stand by. (However, the reset signal is entered regardless of the internal setup status.)

Table 1

$\overline{RES}$ signal input level	MPU type	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	80-series	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7
Active ⎍⎍⎍	68-series	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7

Data transfer

The SED152A drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.
In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.
This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	80 MPU		68 MPU	Function
A0	$\overline{RD}$	$\overline{WR}$	R/$\overline{W}$	
1	0	1	1	Read display data
1	1	0	0	Write display data
0	0	1	1	Read status
0	1	0	0	Write to internal register (command)

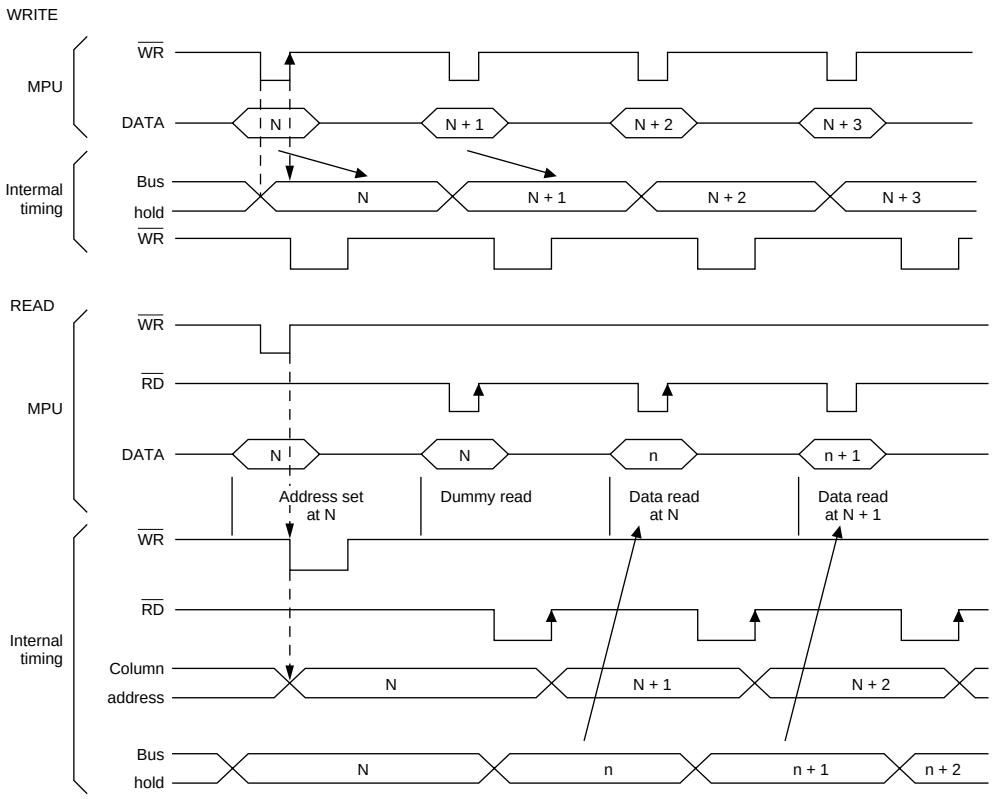


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1520 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

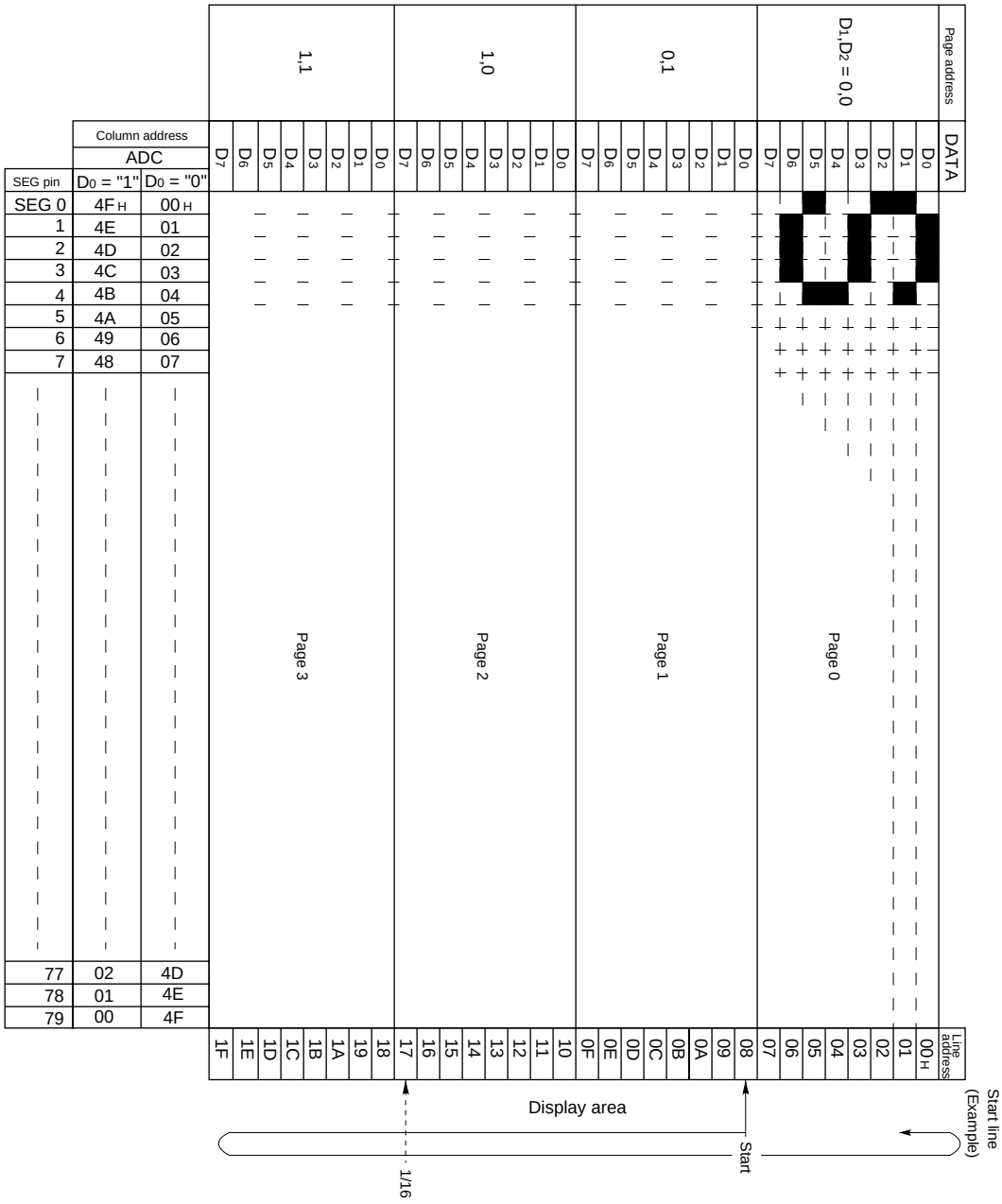
The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 3. The contents of the page register are set by the Set Page Register command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 3.

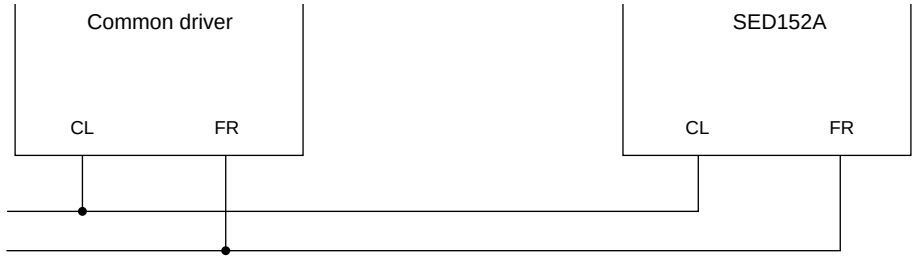


SEG pin	Column address ADC D_0 = "1"	D_0 = "0"
SEG 0	4F H	00 H
1	4E	01
2	4D	02
3	4C	03
4	4B	04
5	4A	05
6	49	06
7	48	07
77	02	4D
78	01	4E
79	00	4F

Figure 2 Display Data RAM Addressing

Display Timing Generation Circuit

The master clock CL and the frame signal FR generate internal timing. The master clock CL causes the line counter to operate, which synchronizes with the line counter. Therefore, the master clock CL and the frame signal FR input signals of the same phases as those of the CR and FR signals of the common driver, respectively.



Display Data Latch Circuit

The display data latch circuit is a latch that temporarily memorizes the display data to be output to the liquid crystal drive circuit from the display data RAM for each common period. Display ON/OFF and Display All Lamps ON/OFF commands control the data in this latch. Therefore, data in the display data RAM are never to be modified.

Liquid Crystal Drive Circuit

This circuit comprises 80 sets of multiplexers to generate four-value level for the liquid crystal drive. Various combinations of display data in the display data latch and the FR signals output the liquid crystal waveforms as shown in Fig. 3.

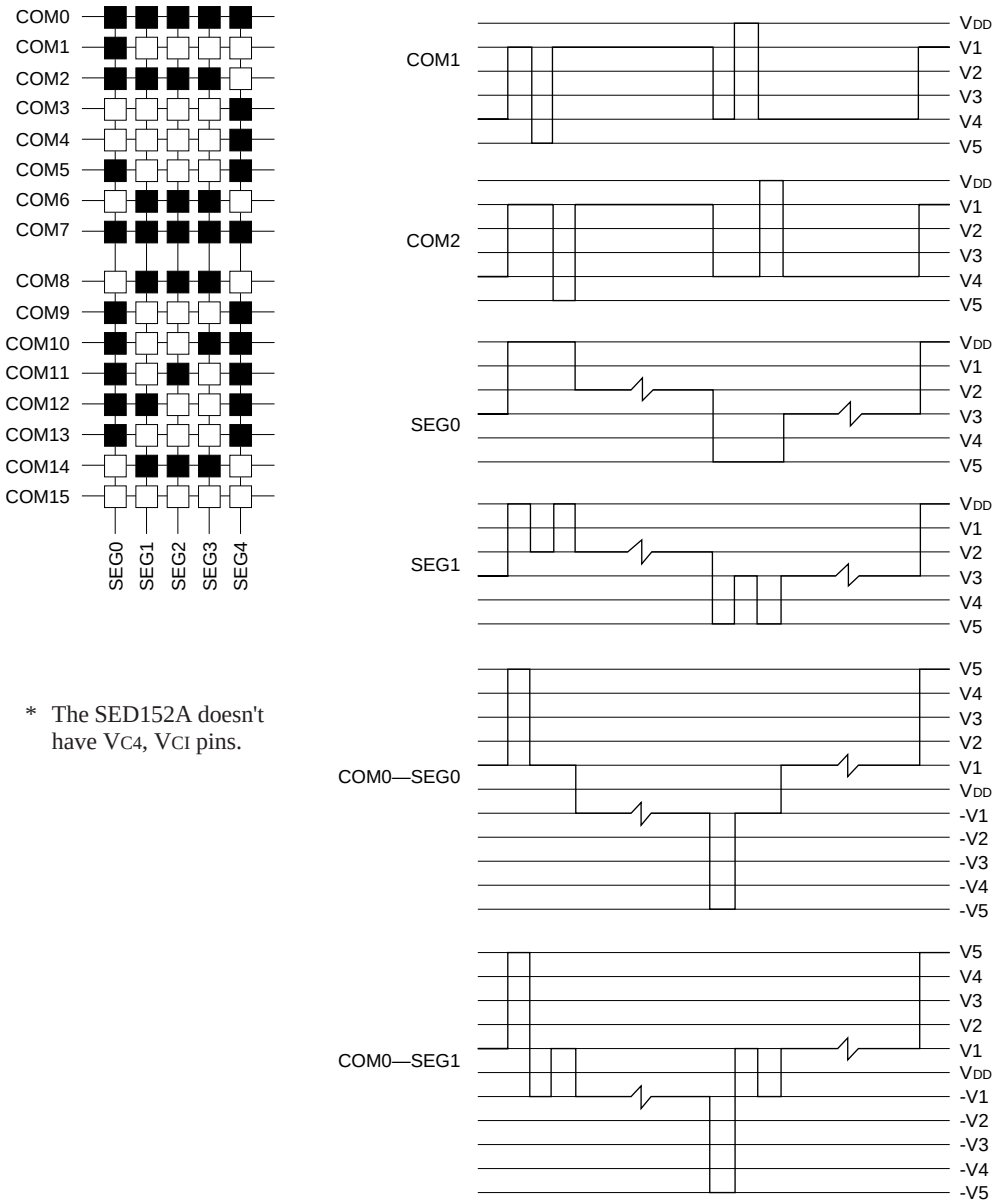
Reset Circuit

This circuit detects the $\overline{RES}$ input rise or fall edge and performs initialization.
$\overline{RES}$ input is level-sensed, then, as shown in Table 1, the MPU interface mode is selected.

When connecting to MPU, the output port of MPU is used and the reset signal is input through software. Otherwise, the circuit is connected to the reset terminal of MPU and the ⎍ reset signal via the inverter is input for 80-system MPU, and the ⎴ reset signal for the 68-system MPU.
$\overline{RES}$ input causes initialization of SEDI52A, and initialization of the MPU is performed at the same time. Failure of initialization by the $\overline{RES}$ terminal upon applying power may lead to a status that cannot be released.
If the reset command is used, items 2 and 5 of the following initial settings are to be executed:

Status in Initial Setting

1. Display OFF
2. To set the display start line register on the first line.
3. Display All Lamps OFF
4. To set the column address counter to address 0.
5. To set the page address counter to the third page.
6. ADC select: normal rotation (ADC command = "0", ADC status flag "1")
7. Read/Modify/Write OFF



* The SED152A doesn't have V_{C4}, V_{CI} pins.

Figure 4 LCD drive waveforms example

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
All-display ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The SED152A identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

This command loads the display start line register.

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

This command loads the page address register.

A_1	A_0	Page Address
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	(E) $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

This command loads the column address register.

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

All Display ON/OFF

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: All display on
D=0: All display off

Read-Modify-Write

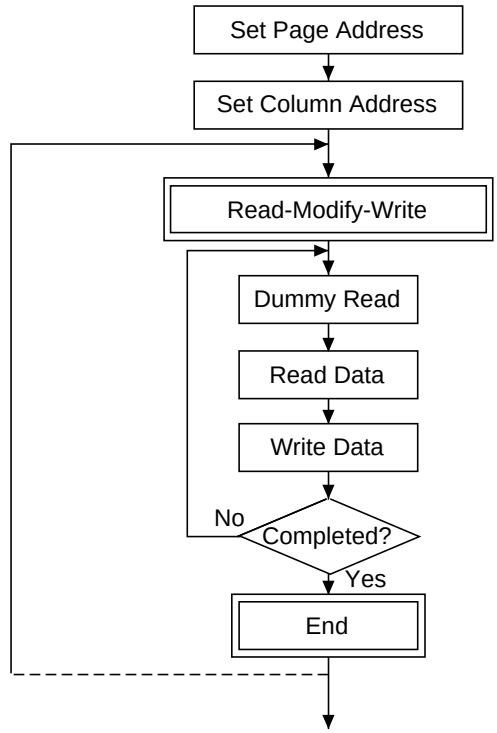
A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

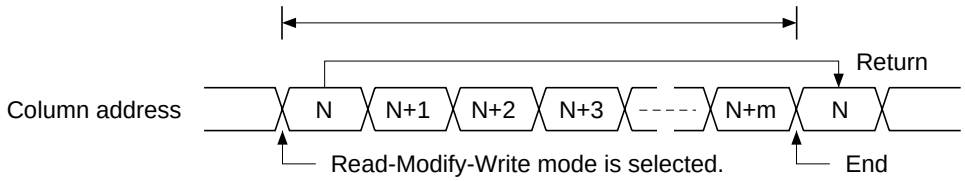
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

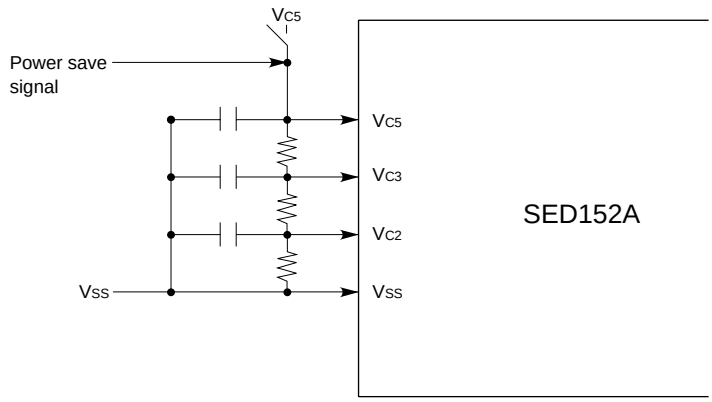
A_0	(E) $\overline{RD}$	(R/$\overline{W}$) $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.
  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to +7.0	V
Supply voltage (2)	V_{C5}	–0.3 to +7.0	V
Supply voltage (3)	V_{C3}, V_{C2}	–0.3 to V_{C5}+3	V
Input voltage	V_{IN}	–0.3 to V_{DD} +0.3	V
Output voltage	V_O	–0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	–40 to +85	deg. C
Storage temperature	T_{stg}	–55 to +125	deg. C

Notes: 1. All voltages are specified relative to V_{SS} = 0 V.
2. The following relation must be always hold
$V_{C5} \geq V_{C3} \geq V_{C2} \geq V_{SS}$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{DD}			4.5	5.0	5.5	V	V_{DD} *1
	Allowable				2.4	—	6.0		
Operating voltage (2)	Allowable	V_{C5}			3.5	—	6.0	V	V_{C5} *2
	Allowable	V_{C3}			0.5×V_{C5}	—	V_{C5}	V	V_{C3}
	Allowable	V_{C2}			V_{SS}	—	0.5×V_{C5}	V	V_{C2}
High-level input voltage		V_{IH}			0.8×V_{DD}	—	V_{DD}	V	*3
		V_{IL}			V_{SS}	—	0.2×V_{DD}	V	*3
		V_{OH1}	I_{OH} = –1 mA		0.8×V_{DD}	—	V_{DD}	V	*4
		V_{OH2}	V_{DD} = –2.7 V I_{OH} = –0.5mA		0.8×V_{DD}	—	V_{DD}	V	*4
Low-level input voltage		V_{OL1}	I_{OL} = 1 mA		V_{SS}		0.2×V_{DD}	V	*4
		V_{OL2}	V_{DD} = 2.7 V I_{OL} = 0.5 mA		V_{SS}		0.2×V_{DD}	V	*4
Input leakage current		I_{L1}			–1.0	—	1.0	µA	*5
Output leakage current		I_{L2}			–3.0	—	3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25 deg. C	V5 = 6.0 V	—	1.3	3.0	kΩ	SEG0 to 79, *7
				V5 = 3.5 V	—	2.5	6.0		

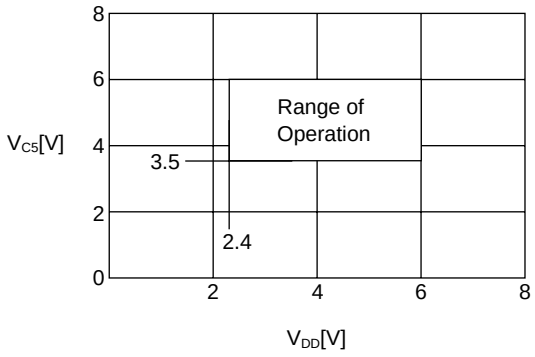
(continued)

DC Characteristics (Cont'd)

Ta = –20 to 75 deg. C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition	Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Static current dissipation		I_{SSQ}	$\overline{CS}$ = CL = FR = V_{DD}	—	0.01	1.0	µA	V_{SS}
Dynamic current dissipation	During display	I_{SS} (1)	V_{DD} = 5 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	2.0	5.0	µA	V_{SS} *8
			V_{DD} = 3.0 V V_{C5} = 5 V Ta = 25°C f_{CL} = 2 KHz	—	1.5	4.5	µA	V_{SS} *8
	During access	I_{SS} (2)	V_{DD} = 5 V t_{cyc} = 200 KHz	—	300	500	µA	V_{SS} *9
			V_{DD} = 3.0 V t_{cyc} = 200 KHz	—	150	300		
Input pin capacitance		C_{IN}	Ta = 25 deg. C, f = 1 MHz	—	5.0	8.0	pF	All input pins

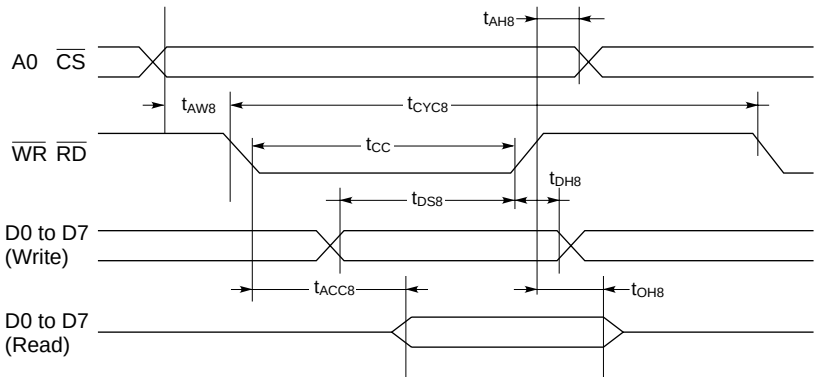
Notes: 1. Although this equipment is capable of withstanding a wide range of operating voltage, it is not designed for withstanding a sudden voltage change while accessing the MPU.
2. Ranges of Operating Voltage for V_{DD} and V_{C5} Systems



3. D0 to D7, A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$, (E), $\overline{WR}$, (R/$\overline{W}$), C_L, and FR terminals.
4. D0 to D7 terminals.
5. A0, $\overline{RES}$, $\overline{CS}$, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), and C_L terminals.
6. FR, D0 to D7 (in high impedance status) terminals.
7. These are resistance values obtained when voltage of 0.1 V is applied between the output terminals (SEG) and the respective power terminals (V_{C3}, V_{C2}). These are defined within the range of the operating voltage.
8. This is current consumed by a single IC, not including current required by the LCD panel capacity or by the wiring capacity.
9. This indicates current consumption at the time the pattern of vertical stripes is always wrapped in by the tcyc. Current consumption while accessing roughly proportionate to the tcyc for access. If not accessed, only I_{SS1} is relevant.

Timing Characteristics

• System Bus Read/Write Characteristic 1 (80-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 $\overline{CS}$	t_{AH8} t_{AW8}	—	10 20	— —	ns ns
System cycle time		$\overline{WR}$ $\overline{RD}$	t_{CYC8}	—	1000	—	ns
Control pulse width	Write		t_{CC}	—	100	—	ns
	Read				200	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	80 10	— —	ns ns
$\overline{RD}$ access time Output disable time			t_{ACC8} t_{OH8}	 C_L = 100 pF	— 10	180 90	ns ns

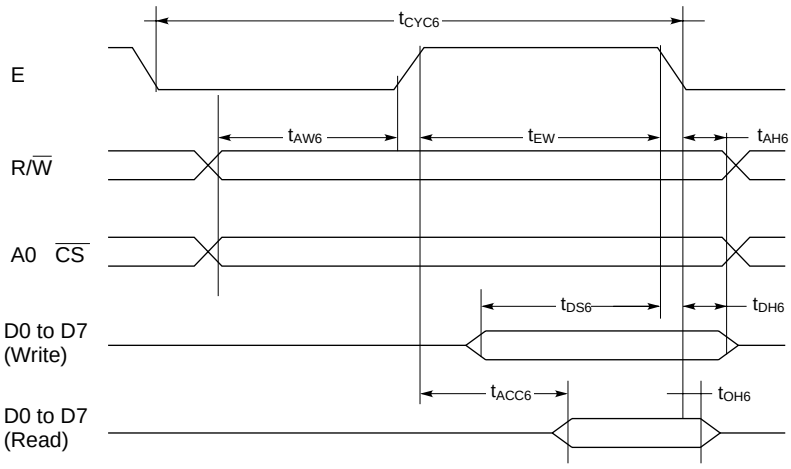
(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time Address set-up time		A0 $\overline{CS}$	t_{AH8} t_{AW8}	—	20 40	— —	ns ns
System cycle time		$\overline{WR}$ $\overline{RD}$	t_{CYC8}	—	2000	—	ns
Control pulse width	Write		t_{CC}	—	200	—	ns
	Read				400	—	ns
Data set-up time Data hold time		D0 to D7	t_{DS8} t_{DH8}	—	160 20	— —	ns ns
$\overline{RD}$ access time Output disable time			t_{ACC8} t_{OH8}	 C_L = 100 pF	— 20	360 180	ns ns

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• System Bus Read/Write Characteristic 2 (68-system MPU)



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	tCYC6	—	1000	—	ns
Address set-up time Address hold time			tAW6 tAH6	—	20 10	— —	ns ns
Data set-up time Data hold time		D0 to D7	tDS6 tDH6	—	80 10	— —	ns ns
Output disable time Access time			tOH6 tACC6	CL = 100 pF	10	90 180	ns ns
Enable pulse width	Write	E	tEW	—	100	—	ns
	Read				200	—	ns

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

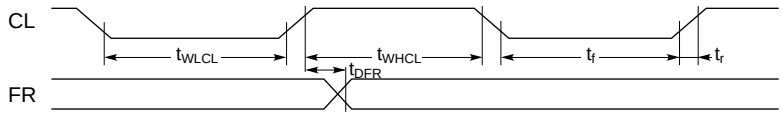
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time *1		A0 CS R/W	tCYC6	—	2000	—	ns
Address set-up time Address hold time			tAW6 tAH6	—	40 20	— —	ns ns
Data set-up time Data hold time		D0 to D7	tDS6 tDH6	—	160 20	— —	ns ns
Output disable time Access time			tOH6 tACC6	CL = 100 pF	20	180 360	ns ns
Enable pulse width	Write	E	tEW	—	200	—	ns
	Read				400	—	ns

Notes: 1 "tCYC6" represents the cycle of signal E when CS = "L". If CS = "H" → "L", it is necessary to secure tCYC6 after CS = "L" is attained.

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.

* All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Display Control Input Timing



(V_{DD} = 5.0 V ± 10%, Ta = –40 to 85°C)

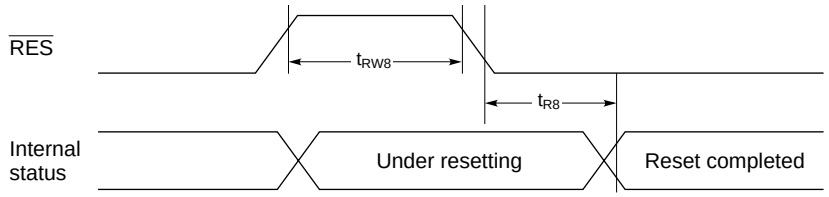
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	35	—	—	µs
High-level pulse width		tWHCL	—	35	—	—	µs
Rise time		tr	—	—	30	150	ns
Fall time		tf	—	—	30	150	ns
FR delay time	FR	tDFR	—	–2.0	0.2	2.0	µs

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low-level pulse width	CL	tWLCL	—	70	—	—	µs
High-level pulse width		tWHCL	—	70	—	—	µs
Rise time		tr	—	—	60	300	ns
Fall time		tf	—	—	60	300	ns
FR delay time	FR	tDFR	—	–4.0	0.4	4.0	µs

Note: All timings are defined based on the standards of 20% and 80% of V_{DD}.

• Reset Input Timing (80-system MPU)



(VDD = 5.0 V ± 10%, Ta = –40 to 85°C)

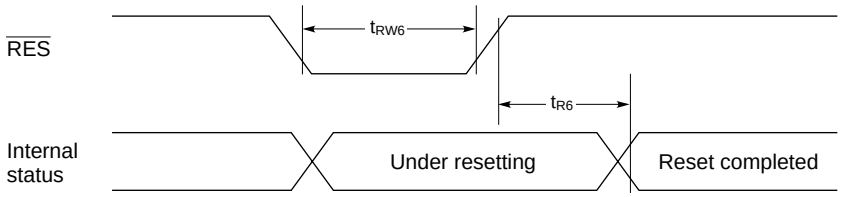
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		tR8		2.0	—	—	µs
Reset "H" pulse width	RES	tRW8		1.0	—	—	µs

(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		tR8		4.0	—	—	µs
Reset "H" pulse width	RES	tRW8		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of VDD.

• Reset Input Timing (68-system MPU)



(VDD = 5.0 V ± 10%, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		tR6		2.0	—	—	µs
Reset "L" pulse width	RES	tRW6		1.0	—	—	µs

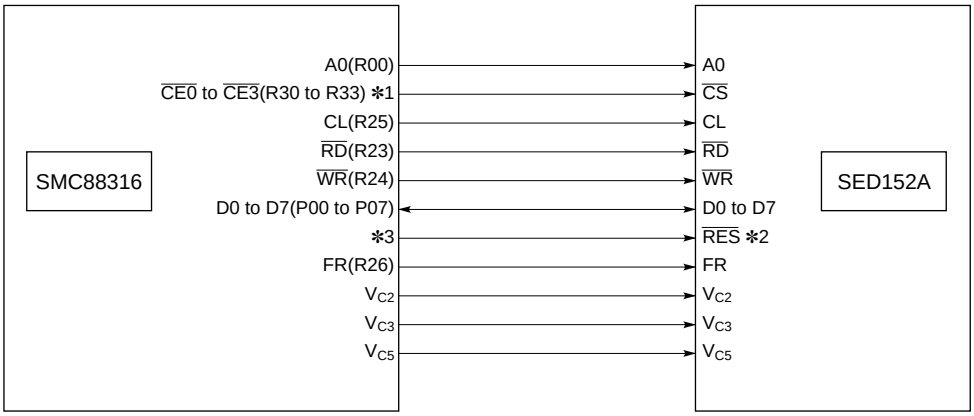
(VDD = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		tR6		4.0	—	—	µs
Reset "L" pulse width	RES	tRW6		2.0	—	—	µs

Note: * The rise time (tr) and fall time (tf) of the input signal are defined within 15 ns. Tr and tf are to define the AC timing of the input waveform, and operates without any problem even when a signal beyond the specification (15 ns) is input. However, it should be noted that the bigger tr and and tf are, the lower the margin for noise becomes.
* All timings are defined based on the standards of 10% and 90% of VDD.

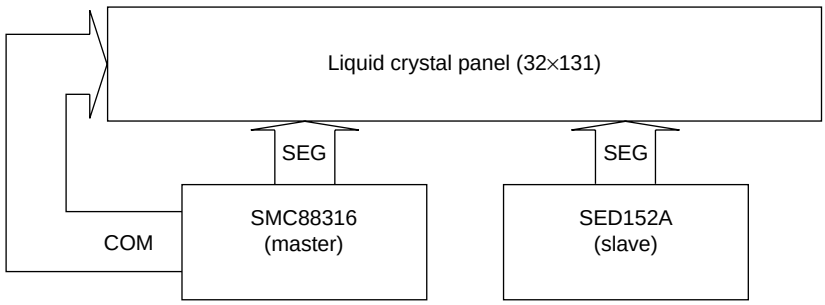
CONNECTION EXAMPLE

MPU Interface (MPU example: SMC88316)



Notes: 1 See SMC88316 technical Manual for the signals of SMC88316.
2 The reset input for 80-system MPU interface of SED152A is the opposite phase of that for the reset input of SMC83315.
3 For the reset input of SED152A, we recommend that you use the output port of SMC88316 and send the reset signals through software.

EXAMPLE OF CONNECTIONS TO LIQUID CRYSTAL PANEL



4. SED1526 Series

Contents

OVERVIEW

The SED1526 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's). It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip display RAM. It can generate an LCD drive signal independent from microprocessor clock.
As the SED1526 series features the very low power dissipation and wide operating voltage range, it can easily realize a powerful but compact display unit having a small battery.
A single chip of SED1526 series can drive a 17×80-pixel or 33×64-pixel LCD panel.

(Note: The SED1526 series are not designed to have EMI resistance.)

FEATURES

- Direct data display using the display RAM. When RAM data bit is 0, it is not displayed; when 1, it is displayed.
- Large 80×33-bit RAM capacity
- On-chip LCD driver circuit (97 segment and common drivers)
- High-speed, 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800
- Supported serial interface
- Rich command functions (upward compatible to SED 1520 Series); they are Read/Write Display Data, Display On/Off Switching, Set Page Address, Set Initial Display Line, Set Column Address, Read Status, Static Drive On/Off Switching, Select Duty, Duty+1, Read-Modify-Write, Select Segment Driver Direction, Power Save, Reset, Set Power Control, Set Electronic Controls, Clock Stop.
- On-chip CR oscillator circuit
- On-chip LCD power circuit (The on-chip and external LCD power supplies are software selectable.)
- Very low power consumption
- Flexible power voltages; 2.4 to 6.0 V (V_{DD}-V_{SS}) and -13.0 to -4.0 V (V_{DD}-V5)
- -40 to +85°C wide operating temperature range
- CMOS process
- 128-pin QFP5 package with aluminum pad or gold bump

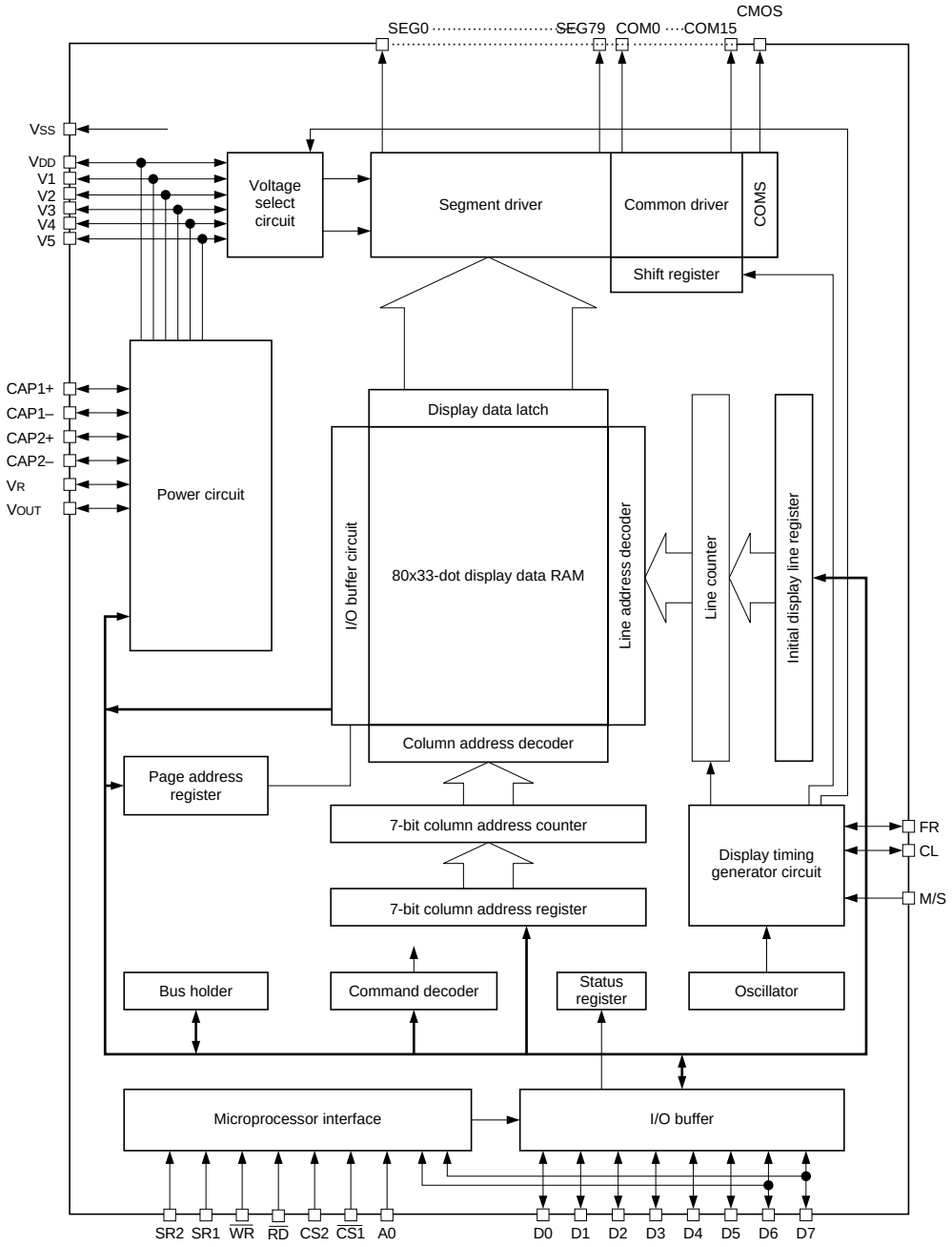
Series Specifications (for 128-pin flat package)

Model	Operating clock (Internal OSC)	Duty	Segment driver	Common driver	V_{REG} type	CMOS pin positions
SED1526F0A	20 kHz	1/8, 1/9, 1/16, 1/17	80	17	Type 1	Type A
SED1526FAA	20 kHz	1/8, 1/9, 1/16, 1/17	80	17	Type 1	Type B
SED1526FEA	20 kHz	1/8, 1/9, 1/16, 1/17	80	17	Type 2	Type A
SED1528F0A	20 kHz	1/32, 1/33	64	33	Type 1	Type A

Type 1 V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: 0.17% /°C
Type 2 V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: 0.00% /°C
Refer to No. P3 (Package pin layout), No. P4 (PAD layout) and No. P5 (PAD coordinates).

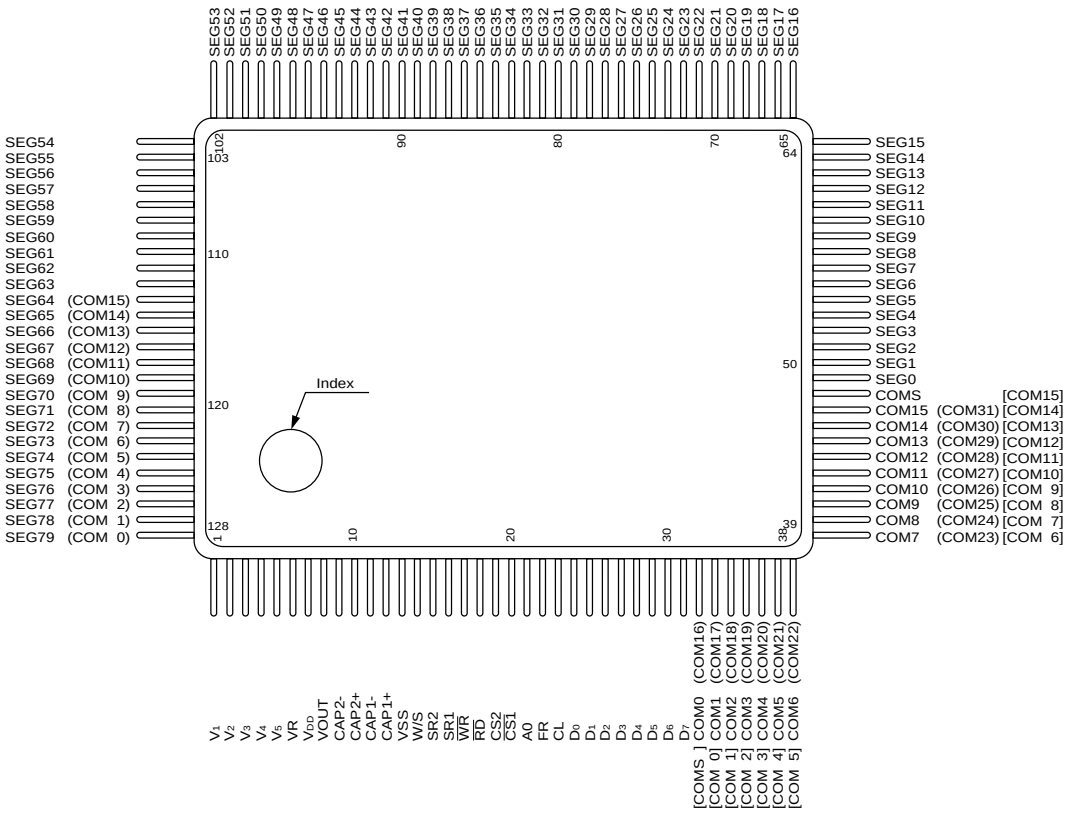
An SED1526 series package has one of following subcodes according to its package type (an example of SED1526):
SED1526F0A: 128-pin QFP5 flat package
SED1526D0*: Bear chip
SED1526D0A having aluminum pad
SED1526D0B having gold bump
SED1526T**: TCP

BLOCK DIAGRAM (SED1526*0*)

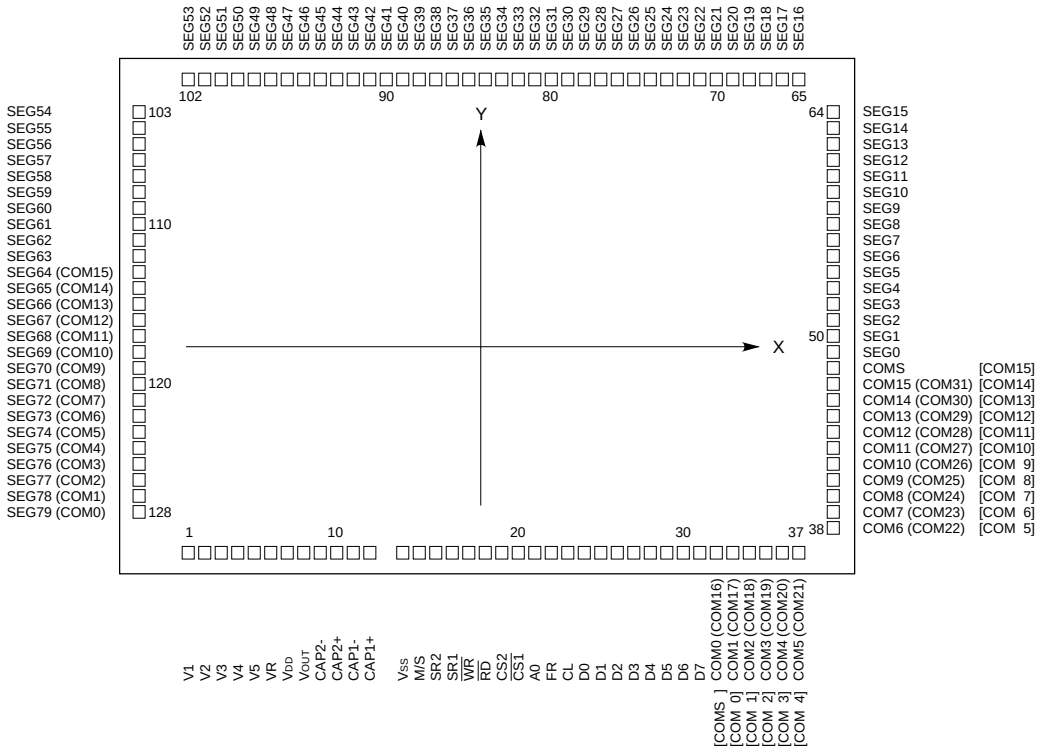


PIN ASSIGNMENT

Package Pin Assignment



Pad Layout



* Pin names in ( ) apply to SED1528.
* Pin names in [ ] apply to SED1526D$_A$* (CMOS pin = Type B).

Aluminum pad chip
- Chip size 5.92 mm × 4.68 mm
- Chip thickness 0.4 mm
- Pad opening 90.2 μm × 90.2 μm
- Pad pitch 130 μm (Min)

Gold bump chip (reference)
- Chip size 5.92 mm × 4.68 mm
- Chip thickness 0.4 mm
- Bump size 81.7 μm × 81.7 μm
- Bump height 22.5 μm

Pad Coordinates

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_1	–2767	–2106	65	SEG16	2516	2185
2	V_2	–2637	–2106	66	SEG17	2367	2185
3	V_3	–2507	–2106	67	SEG18	2218	2185
4	V_4	–2377	–2106	68	SEG19	2088	2185
5	V_5	–2246	–2106	69	SEG20	1957	2185
6	V_R	–2116	–2149	70	SEG21	1827	2185
7	V_{DD}	–1985	–2176	71	SEG22	1697	2185
8	V_{OUT}	–1857	–2176	72	SEG23	1567	2185
9	CAP2–	–1727	–2176	73	SEG24	1437	2185
10	CAP2+	–1522	–2176	74	SEG25	1307	2185
11	CAP1–	–1318	–2176	75	SEG26	1177	2185
12	CAP1+	–1113	–2176	76	SEG27	1046	2185
13	V_{SS}	–553	–2166	77	SEG28	916	2185
14	M/S	–356	–2185	78	SEG29	786	2185
15	SR2	–226	–2185	79	SEG30	656	2185
16	SR1	–95	–2185	80	SEG31	526	2185
17	WR	35	–2185	81	SEG32	396	2185
18	RD	165	–2185	82	SEG33	266	2185
19	CS2	295	–2185	83	SEG34	135	2185
20	CS1	425	–2185	84	SEG35	5	2185
21	A0	555	–2185	85	SEG36	–125	2185
22	FR	719	–2185	86	SEG37	–255	2185
23	CL	849	–2185	87	SEG38	–385	2185
24	D0	979	–2185	88	SEG39	–515	2185
25	D1	1109	–2185	89	SEG40	–646	2185
26	D2	1239	–2185	90	SEG41	–776	2185
27	D3	1369	–2185	91	SEG42	–906	2185
28	D4	1500	–2185	92	SEG43	–1036	2185
29	D5	1630	–2185	93	SEG44	–1166	2185
30	D6	1760	–2185	94	SEG45	–1296	2185
31	D7	1890	–2185	95	SEG46	–1426	2185
32	COM0 (COM16) [CMOS]	2069	–2185	96	SEG47	–1557	2185
33	COM1 (COM17) [COM0]	2199	–2185	97	SEG48	–1687	2185
34	COM2 (COM18) [COM1]	2329	–2185	98	SEG49	–1817	2185
35	COM3 (COM19) [COM2]	2459	–2185	99	SEG50	–1947	2185
36	COM4 (COM20) [COM3]	2589	–2185	100	SEG51	–2077	2185
37	COM5 (COM21) [COM4]	2719	–2185	101	SEG52	–2226	2185
38	COM6 (COM22) [COM5]	2802	–1654	102	SEG53	–2375	2185
39	COM7 (COM23) [COM6]	2802	–1524	103	SEG54	–2802	1932
40	COM8 (COM24) [COM7]	2802	–1393	104	SEG55	–2802	1802
41	COM9 (COM25) [COM8]	2802	–1263	105	SEG56	–2802	1672
42	COM10 (COM26) [COM9]	2802	–1133	106	SEG57	–2802	1541
43	COM11 (COM27) [COM10]	2802	–1003	107	SEG58	–2802	1411
44	COM12 (COM28) [COM11]	2802	–873	108	SEG59	–2802	1281
45	COM13 (COM29) [COM12]	2802	–743	109	SEG60	–2802	1151
46	COM14 (COM30) [COM13]	2802	–612	110	SEG61	–2802	1021
47	COM15 (COM31) [COM14]	2802	–482	111	SEG62	–2802	891
48	COMS [COM15]	2802	–352	112	SEG63	–2802	760
49	SEG0	2802	–193	113	SEG64 (COM15)	–2802	599
50	SEG1	2802	–63	114	SEG65 (COM14)	–2802	469
51	SEG2	2802	67	115	SEG66 (COM13)	–2802	339
52	SEG3	2802	197	116	SEG67 (COM12)	–2802	209
53	SEG4	2802	327	117	SEG68 (COM11)	–2802	78
54	SEG5	2802	457	118	SEG69 (COM10)	–2802	–52
55	SEG6	2802	588	119	SEG70 (COM9)	–2802	–182
56	SEG7	2802	718	120	SEG71 (COM8)	–2802	–312
57	SEG8	2802	848	121	SEG72 (COM7)	–2802	–442
58	SEG9	2802	978	122	SEG73 (COM6)	–2802	–572
59	SEG10	2802	1108	123	SEG74 (COM5)	–2802	–703
60	SEG11	2802	1238	124	SEG75 (COM4)	–2802	–833
61	SEG12	2802	1368	125	SEG76 (COM3)	–2802	–963
62	SEG13	2802	1499	126	SEG77 (COM2)	–2802	–1093
63	SEG14	2802	1629	127	SEG78 (COM1)	–2802	–1223
64	SEG15	2802	1759	128	SEG79 (COM0)	–2802	–1353

* Pin names in ( ) apply to SED1528.
* Pin names in [ ] apply to SED1526D$_A$* (CMOS pin = Type B).

PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5VDC power supply. Common to microprocessor power supply pin V_{CC}.	1
V_{SS}	Supply	Ground	1
V_1, V_2 V_3, V_4 V_5	Supply	LCD driver supply voltages. The Set Power Control command can switch the on-chip and external power supply modes of these pins. When external mode selects, the voltage determined by LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ When master mode selects, these voltages are generated on the chip: SED1526: V1 = 1/5 V_5, V2 = 2/5 V_5, V3 = 3/5 V_5, V4 = 4/5 V_5 SED1528: V1 = 1/7 V_5, V2 = 2/7 V_5, V3 = 5/7 V_5, V4 = 6/7 V_5	5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
V_R	I	Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	Data input/outputs. The 8-bit bidirectional data buses to be connected to the standard 4/8-bit microprocessor data buses. When the serial interface selects, D7 is serial data input (SI) and D6 is serial clock input (SCL).	8
A0	I	Control/display data flag input. It is connected to the LSB of microprocessor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is low and CS2 is high.	2
$\overline{RD}$ (E)	I	• Read enable input. When interfacing to an 8080-series microprocessor and when its $\overline{RD}$ is low, the SED1526 series data bus output is enabled. • When interfacing to an 6800-series microprocessor and when its R/$\overline{W}$ Enable (E) is high, the SED1526 series R/$\overline{W}$ input is enabled.	1
$\overline{WR}$ (R/$\overline{W}$)		• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active low. • When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is high and it will be write mode when R/$\overline{W}$ is low. R/$\overline{W}$ = "1" : Read R/$\overline{W}$ = "0" : Write	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SR1,
SR2</td><td>I</td><td>Microprocessor interface select, and parallel/serial data input select.
<table>
<tr><th>SR1</th><th>SR2</th><th>Type</th></tr>
<tr><td>0</td><td>1</td><td>8080 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>1</td><td>6800 microprocessor bus (parallel input)</td></tr>
<tr><td>1</td><td>0</td><td>Serial input</td></tr>
<tr><td>0</td><td>0</td><td>Reset</td></tr>
</table>
* In serial mode, no data can be read from RAM and D0 to D5 are HZ. $\overline{RD}$ and $\overline{WR}$ must be high or low.
When set for the 68 family MPU, the SR1 and SR2 timing must match or SR1 must rise first.</td><td>2</td></tr>
</table>

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>M/S</td><td>I</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Normally “1”.</td><td>1</td></tr>
<tr><td>SEGn</td><td>O</td><td>LCD segment driver output. V_{DD}, V_2, V_3, or V_5 can select according to the display RAM and FR signal.
<table>
<tr><th>RAM data</th><th>FR signal</th><th>Output voltage of SEGn</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_{DD}</td></tr>
<tr><td>0</td><td>V_5</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V_2</td></tr>
<tr><td>0</td><td>V_3</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td>80 (SED1526)
or 64 (SED1528)</td></tr>
<tr><td>COMn</td><td>O</td><td>LCD common driver output. V_{DD}, V_1, V_4, or V_5 can select according to IC internal scan signal and FR signal. The common scan sequence is reversed in slave mode.
<table>
<tr><th>Internal scan signal</th><th>FR signal</th><th>Output voltage of COMn</th></tr>
<tr><td rowspan="2">1</td><td>1</td><td>V_5</td></tr>
<tr><td>0</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">0</td><td>1</td><td>V_1</td></tr>
<tr><td>0</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table></td><td>16 (SED1526)
or 32 (SED1528)</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. COMS pin is equivalent to following COM output pin when Duty+1 command is running:
<table>
<tr><th rowspan="2"></th><th colspan="2">SED1526</th><th>SED1528</th></tr>
<tr><th>1/9 duty</th><th>1/17 duty</th><th>1/33 duty</th></tr>
<tr><td>Indicator COMS output</td><td>COM8</td><td>COM16</td><td>COM32</td></tr>
</table></td><td>1</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Microprocessor Interface

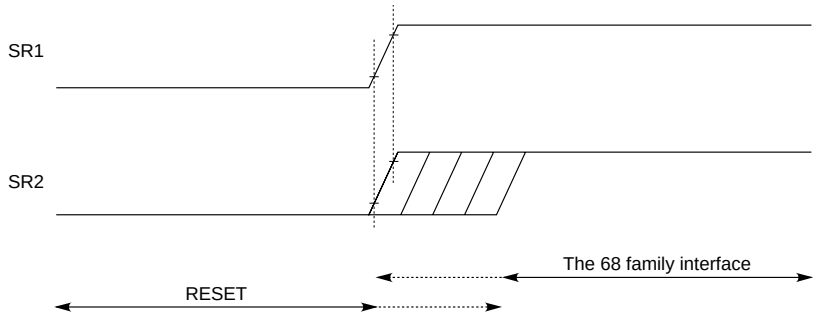
Parallel/Serial Interface

The SED1526 series can transfer data via 8-bit bidirectional data buses D0 to D7 or via serial data input D7 (SI). The 8-bit parallel data input or serial data input, 8080/6800-series microprocessor, and reset status can select according to SR1 and SR2.
No data can be read from RAM and no status can be read during serial data input. Also, $\overline{RD}$ and $\overline{WR}$ are high or low, and D0 to D5 are open.

Table 1

SR1	SR2	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	Data (D0 to D7)
0	1	8080 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
1	1	6800 microprocessor bus (parallel)	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
1	0	Serial input	$\overline{CS1}$	CS2	A0	0/1	0/1	D6 (SCL) and D7 (SI)
0	0	Reset	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	— — — — — — — —

* When set for the 68 family interface, the SR1 and SR2 timing must match or SR1 must rise first.



Data Bus Signals

The SED1526 series identifies the data bus signal according to A0, $\overline{RD}$, and $\overline{WR}$ (E, R/$\overline{W}$) signals.

Table 2

Common	6800 processor	8080 processor		Function
A0	$\overline{WR}$ (R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (commands)

Serial Interface (SR1 is high and SR2 is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.
When serial data input is enabled by SR1 and SR2, D7 (SI) receives serial data and D6 (SCL) receives serial clock. Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.
The serial data input is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.
Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

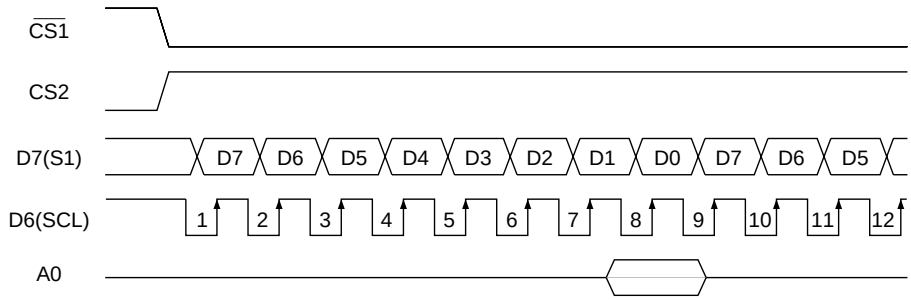


Figure 1

Chip Select Inputs

The SED1526 series can interface to microprocessor when $\overline{CS1}$ is low and CS2 is high.

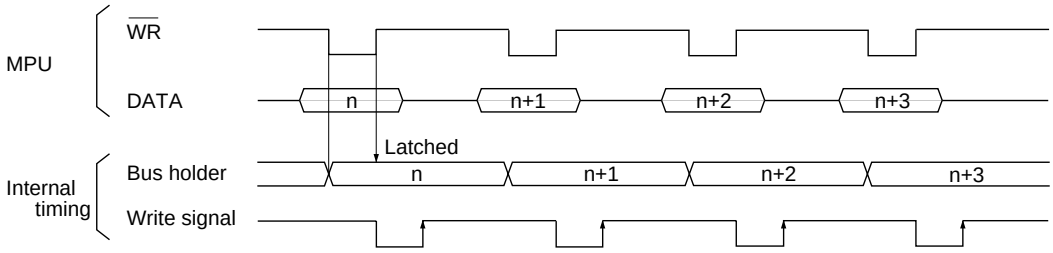
When these pins are set to any other combination, D0 to D7 are high impedance. A0, $\overline{RD}$, and $\overline{WR}$ input are disabled. However, the reset signal is entered regardless of $\overline{CS1}$ and CS2 setup. The internal IC status including LCD driver circuit is held until a reset signal is entered.

Access to Display Data RAM and Internal Registers

The SED1526 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.

When viewed from the microprocessor, the SED1526 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC} and t_{DS}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

•Write



•Read

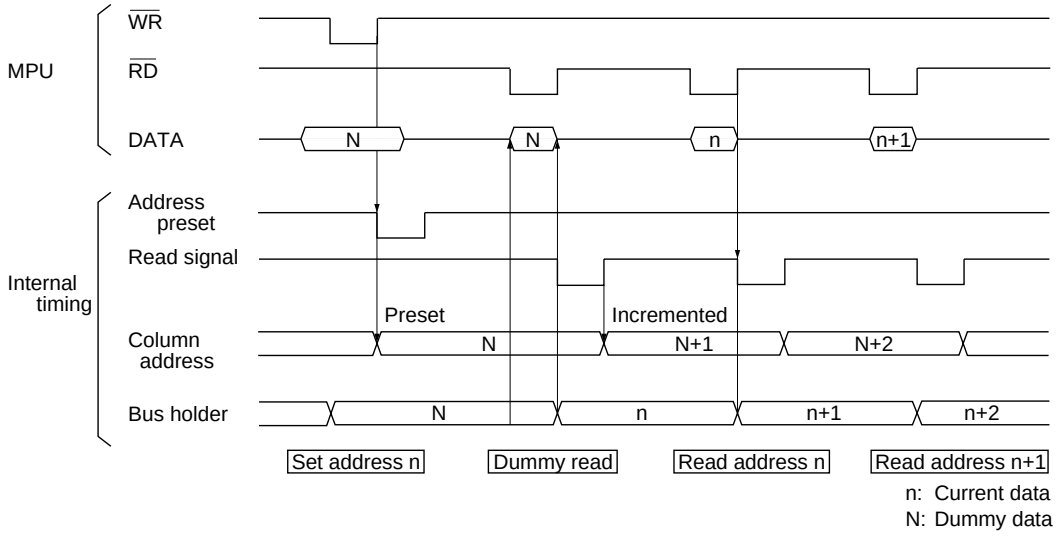


Figure 2

Busy Flag

The Busy flag is set when the SED1526 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 5-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by oscillator circuit output (in master mode) or CL input (in slave mode), and it generates a line address to allow 80-bit sequential data output from display RAM to LCD driver circuit.

Column Address Counter

This is a 7-bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 50H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 4 (D2 is high, but D0 and D1 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 33-column by 80-row (4-page by 8+1 bit) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1526's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

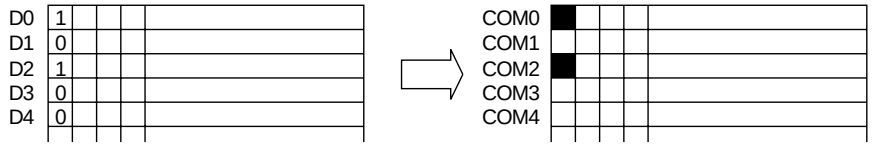


Figure 3

Relationship between display data RAM and addresses (if initial display line is 08):

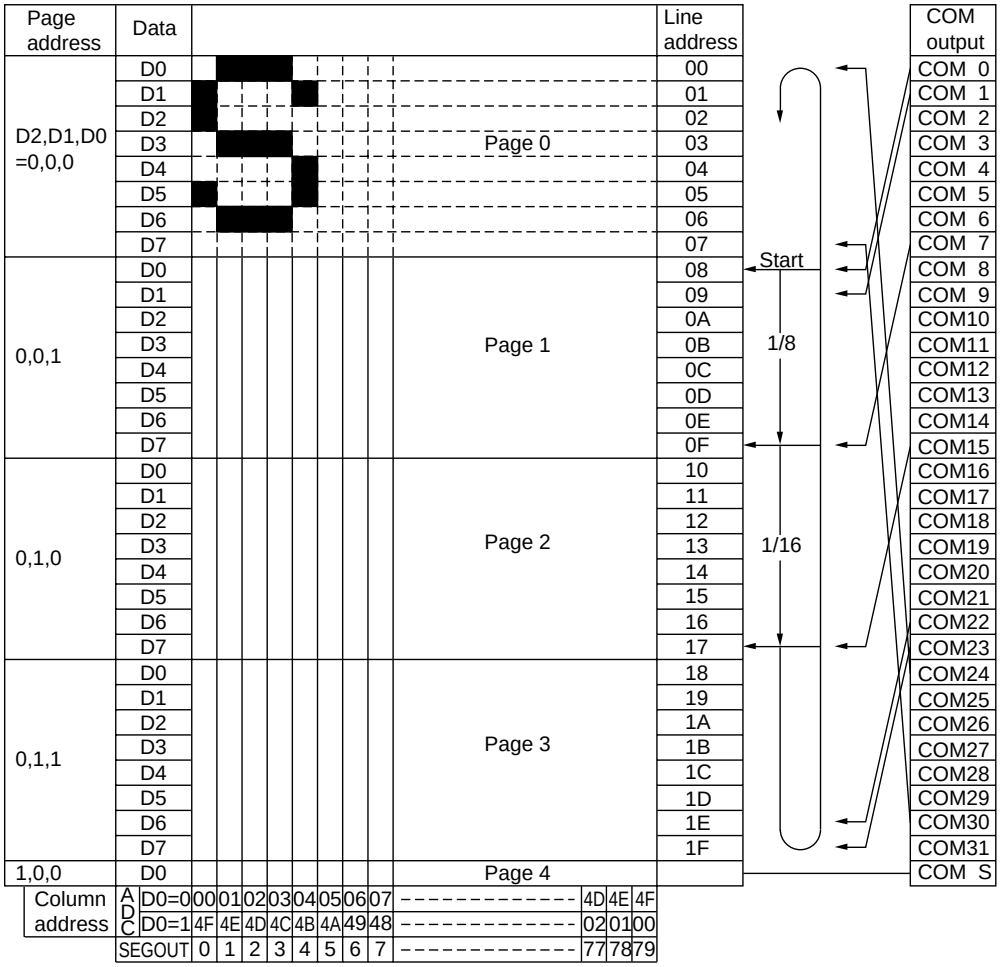


Figure 4

Display Timing Generator Circuit

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

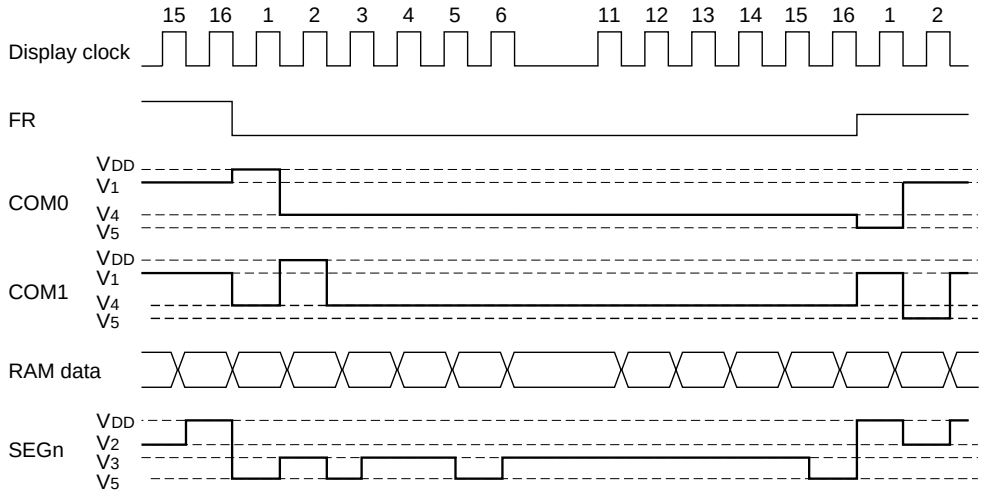
The line address counter, RAM, and latch circuit of the SED1526 series operate synchronous to the display clock (the oscillator circuit outp).mm The LCD drive signal is sent to LCD panel driver output pin SEGn.

The timing of LCD panel driver outputs is independent of the timing of RAM data input from microprocessor.

LCD AC Signal (FR)

The LCD AC signal, FR, is generated from the display clock. The FR controller generates dual-frame AC driver waveforms for LCD panel driver circuit.

- **Dual-frame AC driver waveforms**
  (If SED1526 is used in 1/16 duty)



Common timing Signals

The common timing generator circuit uses the display clock to generate common timing signal and FR frame signal. The Duty Select command can select 1/8 or 1/16 duty (SED1526). A combination of Select Duty and Duty+1 commands can select 1/9 or 1/17 duty (SED1526).

Display Data Latch Circuit

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display ON/OFF and Static Drive ON/OFF commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 96 segment outputs to generate four-level LCD panel drive signals. The circuit also has a pair of COM outputs for indicator display.
The COMn output has a shift register to sequentially output COM scan signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 6 gives an example of SEG and COM output waveforms.

Oscillation Circuit

This is a low power consumption CR oscillator having an oscillator resistor, and its output is used as the display timing signal source or as the clock for voltage boost circuit of LCD power supply.
The display clock output can be stopped by Clock Stop command to minimize the current consumption of LCD panel.

Power Supply Circuit

The power supply circuit produces voltage to drive LCD panel at low power consumption. The power circuit consists of three subcircuits: voltage tripler, voltage regulator, and voltage follower. The voltage tripler outputs V_{DD} -(V_{SS}×2) or -(V_{SS}×3) voltage at V_{OUT}. The regulator circuit generates V_5 voltage using external resistor. The voltage follower circuit changes the impedance of V_1 to V_4 that are generated from V_5 through division with internal resistors. (Details are explained later.)
SED1526 series can drive LCD panel using on-chip power circuit. However, the on-chip power circuit is intended to use for a small LCD panel and it is inappropriate to a large panel requiring multiple driver chips. As the large LCD panel has the dropped display quality due to large load capacity, it must use an external power source.
The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of on-chip power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]

D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
1 1 1	ON	ON	ON	—	Used	Used
1 0 0	ON	OFF	OFF	—	Used	OPEN
0 1 1	OFF	ON	ON	To V_{OUT}	OPEN	Used
0 0 0	OFF	OFF	OFF	To V_1 to V_5	OPEN	OPEN

To use the on-chip (internal) power supply only, set (D2,D1,D0)=(1,1,1).

To use the voltage booster circuit only, set (D2,D1,D0)=(1,0,0).

To use the voltage regulator and voltage follower, set (D2,D1,D0)=(0,1,1).

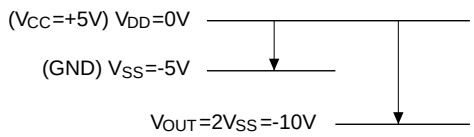
To use an external power supply only, set (D2,D1,D0)=(0,0,0).

Notes: 1. The voltage booster terminals are CAP1+, CAP1-, CAP2+, and CAP2-.
2. The above listed examples are the most practical use to control each circuit using control bits. Any other setup is unpractical and omitted in this manual.
3. The V/F circuit alone cannot be used. When this circuit is used, the V adjustment circuit must be set simultaneously.

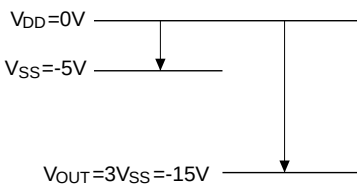
Voltage tripler

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2–, and between V_{SS} and V_{OUT}, the potential between V_{DD} and V_{SS} is boosted to triple toward negative side and it is output at V_{OUT}. For double boosting, remove only capacitor C1 between CAP2+ and CAP2-, open CAP2+, and jumper between CAP2- and V_{OUT}. The double boosted voltage appears at V_{OUT} (CAP2-).

The booster receives signals from oscillator circuit and, therefore, the oscillator must be active. The following shows the boosted potential.



Potential during double boosting

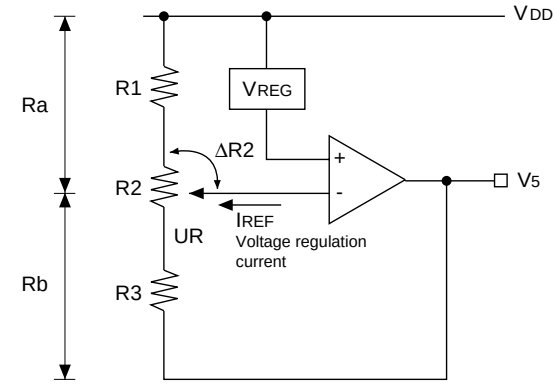


Potential during triple boosting

Voltage regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) drive voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V_5|<|V_{OUT}|$.

$$V_5=(1+\frac{Rb}{Ra})\cdot V_{REG}+I_{REF}\cdot Rb$$
$$=(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2})\cdot V_{REG}$$
$$+I_{REF}\cdot(R3+R2-\Delta R2)$$



where, V_{REG} is the constant voltage source of the IC, and it is constant (V_{REG} ≒ –3.1 V). (V_{REG}=Type1) $V_{REG}=V_{SS}$(V_{DD} basis) (V_{REG}=Type2)
I_{REF} is the voltage regulation current of the Electronic Volume Control Function, and I_{REF} ≒ 2.4 µA if the electronic volume control register (32-state) has (D4,D3,D2,D1,D0)=(1,1,1,1,1).
To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0) =(0,0,0,0,0)):

$$V_5 = (1 + \frac{R3 + R2 - \Delta R2}{R1 + \Delta R2}) \cdot V_{REG} \quad \text{..... ①}$$

(As I_{REF} = 0A)

- R1 + R2 + R3 = 6.0 MΩ ..... ②
  (Determined by the current passing between V_{DD} and V5)
- Variable voltage range by R2: –6.2 to –9.3 V
  (Determined by the LCD characteristics)
  ΔR2 = 0Ω, V_{REG} = –3.1 V
  To obtain V_5 = –9.3 V, from equation (1):
  R2 + R3 = 2 · R1 ..... ③
  ΔR2 = R2, V_{REG} = –3.1 V
  To obtain V_5 = –6.2 V, from equation (1):
  R1 + R2 = 1 · R1 ..... ④

From equations ②, ③ and ④: R1 = 2.0 MΩ
R2 = 1.0 MΩ
R3 = 3.0 MΩ

The voltage regulator circuit has a temperature gradient of approximately –0.17%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.
As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
When the V_{REG} = Type 2, similarly preset R1, R2 and R3 on the basis of $V_{REG} = V_{SS}$.

Voltage regulator circuit using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.

To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the voltage tripler off, the voltage must be supplied from V_{OUT} terminal.

When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra}) \cdot V_{REG} + I_{REF} \cdot Rb \quad \text{..... ⑤}$$

(Variable voltage range)

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF}=I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

(1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

(2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step (1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad [V_5 = (1 + Rb/Ra) \cdot V_{REG}]$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.
V_{REG} =–3.1V±0.4V (Type1) V_{REG} =–0.17%/°C
V_{REG} =V_{SS} (V_{DD} basis) (Type2) V_{REG} =–0.00%/°C
I_{REF} = –1.2 µA ± 40% (For 16 levels) I_{REF} = 0.011 µA/°C
I_{REF} = –2.4 µA ± 40% (For 32 levels) I_{REF} = 0.022 µA/°C
Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or by issuing the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage: V_5 = –6.2 V (Electronic volume control register values (D4,D3,D2,D1,D0)=(0,0,0,0,0))
V_5 minimum voltages: V_5 = –8.6 V (Electronic volume control register values (D4,D3,D2,D1,D0)=(1,1,1,1,1))
V_5 variable voltage range: 2.4 V
Variable voltage levels: 32 levels

(1) Determining the Rb:

$$Rb = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{2.4\ V}{2.4\ \mu A} \qquad \underline{Rb = 1.0\ M\Omega}$$

(2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5\ max}{V_{REG}} - 1} = \frac{1.0\ M\Omega}{\frac{-6.2\ V}{-3.1\ V} - 1} \qquad \underline{Ra = 1.0\ M\Omega}$$

According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

If Ta = 25°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1\ M\Omega) \times (-3.1\ V)$
= –6.2 V

V_5 min = V_5 max + Rb · I_{REF}
= –6.2 V + 1 MΩ × (–2.4 μA)
= –8.6 V

If Ta = –10°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1M\Omega) \times (-3.1\ V) \times \{1 + (-0.17\%/°C) \times (-10°C - 25°C)\}$
= –6.57 V

V_5 min = V_5 max + Rb · I_{REF}
= –6.57 V + 1MΩ × {–2.4 μA + (0.022 μA/°C) × (–10°C – 25°C)}
= –8.20 V

If Ta = 50°C:

V_5 max = $(1 + Rb/Ra) \cdot V_{REG}$
= $(1 + 1\ M\Omega/1\ M\Omega) \times (-3.1\ V) \times \{1 + (-0.17\%/°C) \times (50°C - 25°C)\}$
= –5.94 V

V_5 min = V_5 max + Rb · I_{REF}
= –5.94 V + 1MΩ × {–2.4 μA + (0.022 μA/°C) × (–50°C – 25°C)}
= –8.89 V

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.
When the V_{REG} = Type 2, it so becomes that $V_{REG} = V_{SS}$ and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with V_{REG} = Type 1.

Voltage generator for LCD (Voltage fullower)

The V_5 potential is divided using resistance within IC and V_1, V_2, V_3 and V_4 potentials are generated for LCD panel drive. These potentials are then converted in impedance by voltage follower, and sent to LCD driver circuit.
Because the LCD drive voltage has been fixed to each model, the display quality may drop in specific duty selected by Select Duty command. If it occurs, use an external power supply.

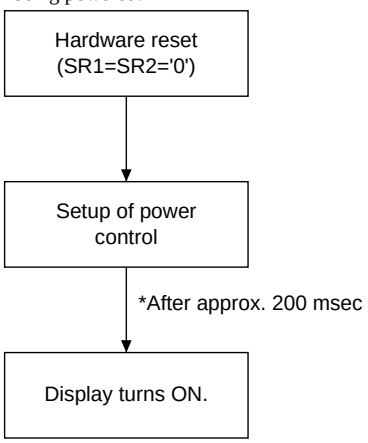
Model	LCD drive voltage
SED1526 SED1528	1/5 of bias voltage 1/7 of bias voltage

Subsection gives wiring examples and reference parts list when on-chip power supply is used and when not used.

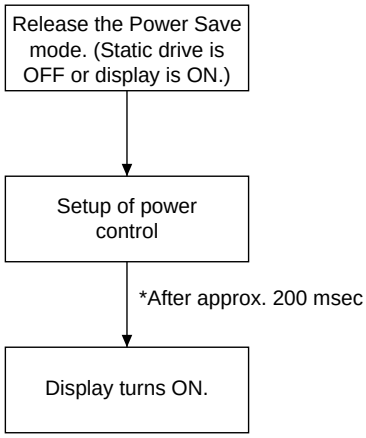
Command sequence for built-in power circuit startup

The built-in power circuit must follow the command sequence given below.

• To start the built-in power circuit when logic units are being powered:



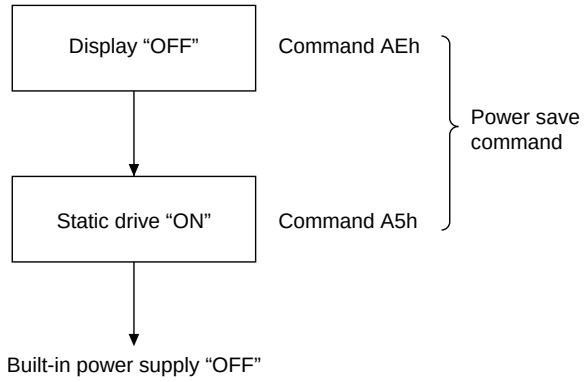
• To start the built-in power circuit after release of Power Save mode:



* When the Set Power Control command is issued, the V_{DD} level signal is output at both COM and SEG terminals for approximately 200 msec. Any other command can be entered during this period.

When turning off the built-in power circuit, observe the following command sequence to mainyain power save status.

When turning off the built-in power supply:



Reset Circuit

The SED1526 series chip parameters are initialized when both SR1 and SR2 are set to low.

○ **Initial parameter setup**

1. Display : Off
2. Duty cycle : 1/16 (SED1526)
3. ADC select : Normal (D0 ADC command is high and ADC status flag is set)
4. Read-modify-write : Off
5. Power Control register : 0
6. Initial Display Line register : Line 1
7. Column Address counter : Address 0
8. Page Address register : Page 0
9. Register data of serial interface : Cleared
10. Electronic control register : 0
11. Static drive : Off
12. Clock : Output

As explained in Section 10.2, the microprocessor should also be reset when SR1 and SR2 are reset. The SR1 and SR2 go low only when logical low pulses are entered at least 10 microseconds (refer to Section for AC characteristics). The normal reset signal appears 1 microsecond after the rising edge of this signal.
If the on-board LCD power circuit of the SED1526 series is not used, both SR1 and SR2 must be low when an external LCD power is supplied. If not low, the IC chip may be destroyed by surge current.
When reset, each register is cleared but the present setup of oscillator circuit and output terminals (FR, CL, D0 to D7) is not cleared.
As the SED1526 series does not have a Power-On Clear circuit, both SR1 and SR2 must go low when logic power applies. If not, any recovery may fail.
The Reset command can reset parameters 6 to 10 listed above.

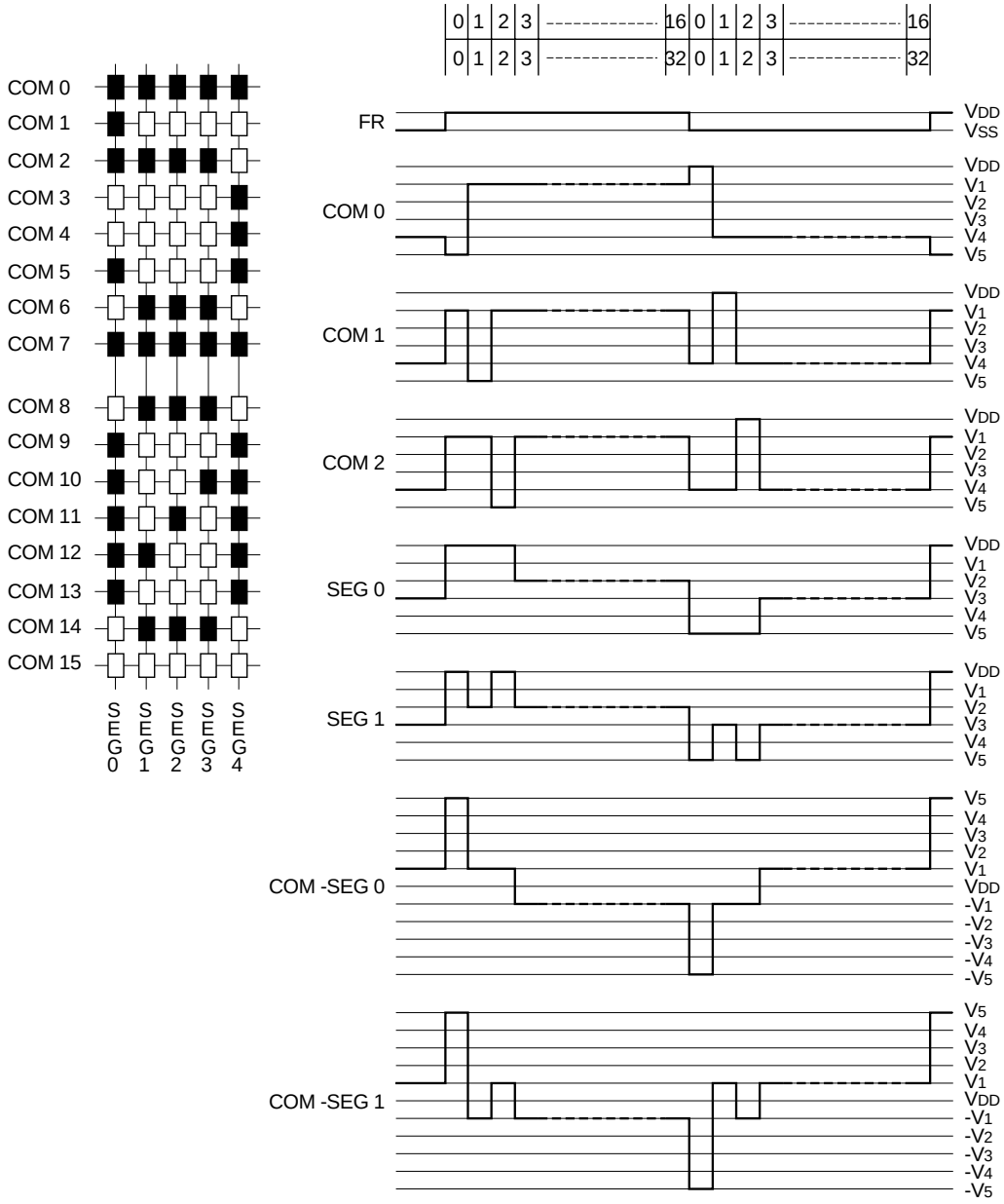


Figure 6

COMMANDS

Table 7 lists available commands. The SED1526 series uses a combination of A0, $\overline{RD}$ and $\overline{WR}$ (or R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only (any external clock is required), its processing speed is very high and its busy check is usually not required.

• Command set

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Initial Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	0	A4	A3	A2	A1	A0

← High-order bit

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
		:			:
1	1	1	1	0	3 0
1	1	1	1	1	3 1

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 4 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	A2	A1	A0

A2	A1	A0	Page Address
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

(4) Set Column Address
Specifies column address of display RAM. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 80 is accessed. The page address is not changed during this time.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	7 9

(5) Read Status

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	PS	0	0	0

BUSY: When high, the SED1526 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "79-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by SR1 and SR2 to go low or by Reset command. When low, the display is on. When high, the chip is being reset.

PS: When low, LCD panel is in Power Save mode.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data
Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select
Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Static Drive ON/OFF

Forcibly turns the entire display ON and makes all common outputs selectable regardless of RAM data contents. The RAM data is held.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D goes low, the static drive turns off. When D goes high, the static drive turns on.

The LCD panel enters Power Save mode if Static Drive ON command is issued when the display is off. Refer to the Power Save section for details.

(10) Select Duty

Selects the LCD driver duty. However, the bias of LCD driver voltage is fixed when on-chip power circuit is used (refer to Subsection).

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
SED1526	0	1/8
	1	1/16
SED1528	0	1/32
	1	1/32

(11) Duty+1

Increments the duty by 1. If 1/8 duty is set for the SED1526, for example, it is incremented to 1/9 duty. If 1/16 duty is set, it is incremented to 1/17 duty. The COMS terminal functions as COM8 or COM16. The display line of RAM area corresponding to page address 4, or D0, is always accessed.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
SED1526	0	1/8 or 1/16
	1	1/9 or 1/17
SED1528	0	1/32
	1	1/33

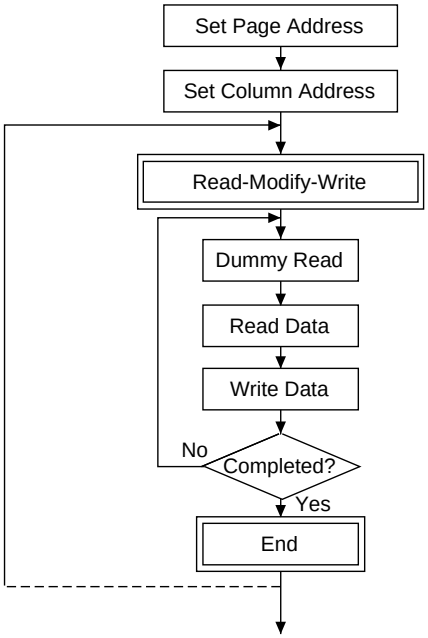
(12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

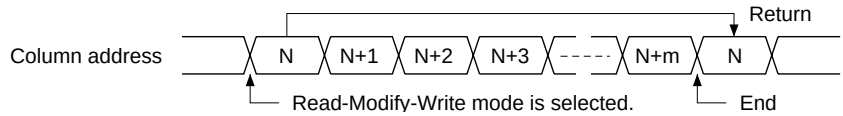
• Cursor display sequence



(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, register data of serial interface, and Electronic Control register to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only RES (that sets SR1 and SR2 to low) can initialize the supplies.

(15) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power supply functions can be used simultaneously. Refer to Power Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	D2	D1	D0

When D0 goes low, voltage follower turns off. When D0 goes high, it turns on.
When D1 goes low, voltage regulator turns off. When D1 goes high, it turns on.
When D2 goes low, voltage booster turns off. When D2 goes high, it turns on.

(16) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V_5 LCD drive voltage that is output by voltage regulator of on-chip power supply.
This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator Circuit section of FUNCTIONAL DESCRIPTION for details.
This command is valid only when voltage regulator circuit is turned on by Set Power Control command.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	0	D4	D3	D2	D1	D0

D4	D3	D2	D1	D0	| V_5 |
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		↓			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(17) Clock Stop

Stops clock output at CL to reduce current consumption.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	F4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

Clock outputs when D is low, but clock stops when D is high.

(18) Power Save (a combination with Static Drive command)

Sets LCD panel in power save mode if Static Drive ON is issued when the display is off. Power consumption drops power consumption level.
When LCD panel enters Power Save mode:

(a) Both oscillator and power supply stop.
(b) LCD driver stops, and segment and common driver have V_{DD} level output.
(c) External clock input is disabled, and clock output is set to low (at CL).
(d) Both display data and operation mode before issue of Power Save are held.
(As the power control register is cleared, the Set Power Control command must be issued again after the Power Save mode has been released.)
(e) All LCD driver voltages are fixed to V_{DD}.

The Power Save is released when the display is turned on or when Static Drive OFF is issued. If external voltage driver resistors are used to supply voltage to LCD panel, current passing through resistors must be cut off. An external power supply must be turned off if used; its voltage must be fixed to floating or V_{DD} level.

* When the SED1526 family is operating, the internal status data set by commands is held. However, the internal status may change due to an excessive ambient noise. The package and system noise generation must be suppressed or a noise protection design must be considered.
We recommend to periodically refresh the internal status data to prevent a spike noise and other interference.

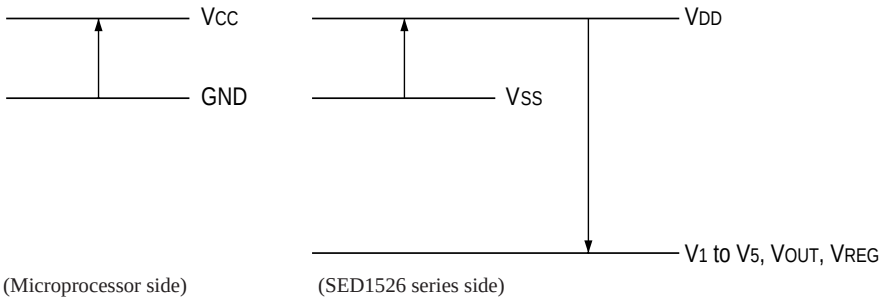
SED1526 Series Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	1	1	0	Initial display address					Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	1	Page address			Sets the display RAM page in Page Address register.
(4) Set Column Address	0	1	0	0	Column address							Sets RAM column address in Column register.
(5) Read Status	0	0	1	Status					0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Static Drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Normal indication when low, but full indication when high.
(10) Duty Select	0	1	0	1	0	1	0	1	0	0	0 1	Selects LCD driver duty of 1/8 (1/16) when low and 1/16 (1/32) when high.
(11) Duty+1	0	1	0	1	0	1	0	1	0	1	0 1	Selects normal LCD driver duty when low, and selects the duty added by 1 when high.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Power Control	0	1	0	1	0	1	1	0	Power control			Selects various power circuit functions.
(16) Set Electronic Control	0	1	0	1	0	0	Electronic control value					Sets V_5 output voltage to Electronic Control register.
(17) Clock Stop	0	1	0	1	1	1	0	0	1	1	0 1	Stops clock output at CL when low, and stops clock when high.
(18) Power Save	–	–	–	–	–	–	–	–	–	–	–	A combination of Display OFF and Static Drive ON commands.

Note: Do not use any other command, or the system malfunction may result.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple voltage conversion	V_{DD}	–0.3 to +6.0	
Driver supply voltage range (1)		V5	–18.0 to +0.3	V
Driver supply voltage range (2)		V1, V2, V3, V4	V5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		VO	–0.3 to V_{DD}+0.3	V
Allowable loss		P_D	250	mW
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	QFP • TCP	T_{STG}	–65 to +150	°C
	Bear chip		–55 to +125	
Soldering temperature and time		T_{SOLDER}	260-10 (at leads)	°C•sec



Notes: 1. V_1 to V_5, V_{OUT}, and V_{REG} voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ $V_{SS} \geq V_{OUT}$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.
4. The moisture resistance of the flat package may drop during soldering. Take care not to excessively heat the package resin during chip mounting.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 5 V ±10%, V_{SS} = 0 V, Ta = –40 to +85°C unless otherwise noted.

Item			Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)		Operational	V_{DD}		2.4		6.0	V	V_{DD} *1
Operating voltage (2)		Operational	V_5		–13.0		–4.0	V	V_5 *2
		Operational	V_1, V_2		$0.6 \times V_5$		V_{DD}	V	V_1, V_2
		Operational	V_3, V_4		V_5		$0.4 \times V_5$	V	V_3, V_4
CMOS	High-level input voltage		V_{IHC}		$0.7 \times V_{DD}$		V_{DD}	V	*3
				V_{DD} = 2.7 V	$0.8 \times V_{DD}$		V_{DD}		
	Low-level input voltage		V_{ILC}		V_{SS}		$0.3 \times V_{DD}$	V	*3
				V_{DD} = 2.7 V	V_{SS}		$0.2 \times V_{DD}$		
	High-level output voltage		V_{OHC}	I_{OH} = –1 mA	$0.8 \times V_{DD}$		V_{DD}	V	*4
				V_{DD} = 2.7 V, I_{OH} = –0.5 mA	$0.8 \times V_{DD}$		V_{DD}		
	Low-level output voltage		V_{OLC}	I_{OH} = 1 mA	V_{SS}		$0.2 \times V_{DD}$	V	*4
				V_{DD} = 2.7 V, I_{OL} = 0.5 mA	V_{SS}		$0.2 \times V_{DD}$		
Schmitt	High-level input voltage		V_{IHS}		$0.4 \times V_{DD}$		$0.8 \times V_{DD}$	V	*5
				V_{DD} = 2.7 V	$0.4 \times V_{DD}$		$0.8 \times V_{DD}$		
	Low-level input voltage		V_{ILS}		$0.2 \times V_{DD}$		$0.6 \times V_{DD}$	V	*5
				V_{DD} = 2.7 V	$0.2 \times V_{DD}$		$0.6 \times V_{DD}$		
Input leakage current			I_{LI}		–1.0		1.0	µA	*6
Output leakage current			I_{LO}		–3.0		3.0	µA	*7
LCD driver ON resistance			R_{ON}	Ta = 25°C V_5 = –0.5 V		15.0	30.0	KΩ	SEG0 to 79 COS0 to 15 COMS *9
Static current consumption			I_{DDQ}	$\overline{CS}$ = C_L = V_{DD}		0.05	3.0	µA	V_{DD}
Input pin capacity			C_{IN}	Ta = 25°C, f = 1 MHz		5.0	8.0	pF	Input pins
CL output frequency			f_{CL}	Ta = 25°C, V_{DD} = 2.7 to 5 V	2.4	2.9	3.7	kHz	*8

Dynamic current consumption (1) when the built-in power supply is OFF Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (1)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V	–	9.1	18	µA	*12
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V	–	12.0	24		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V	–	7.5	15		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V	–	9.5	19		

Dynamic current consumption (2) when the built-in power supply is ON Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	28	56	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	52	104		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	29	58		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	48	96		

Dynamic current consumption (1) when the built-in power supply is OFF Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (1)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V	–	9.1	18	µA	*12
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V	–	7.5	15		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V	–	12.0	24		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V	–	9.5	19		

Dynamic current consumption (2) when the built-in power supply is ON (Display all white) Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	31	62	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	44	88		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	37	74		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	55	110		

Dynamic current consumption (2) when the built-in power supply is ON (Display checker pattern) Ta = 25°C

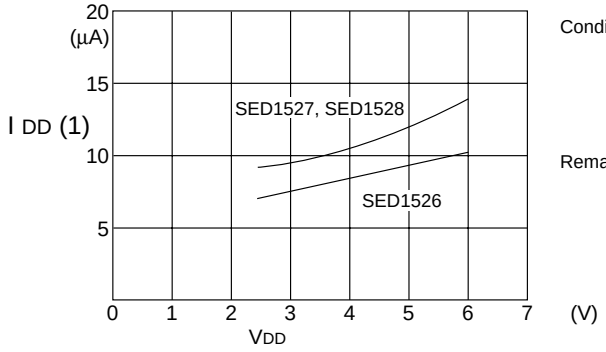
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
SED1526	I_{DD} (2)	V_{DD} = 5.0V, V_5–V_{DD} = –6.0V, dual boosting	–	34	68	µA	*13
		V_{DD} = 3.0V, V_5–V_{DD} = –6.0V, triple boosting	–	46	92		
SED1528		V_{DD} = 5.0V, V_5–V_{DD} = –8.0V, dual boosting	–	42	84		
		V_{DD} = 3.0V, V_5–V_{DD} = –8.0V, triple boosting	–	60	120		

Current consumption during Power Save mode V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power save mode	I_{DDS1}	SED1526, SED1528	—	3	6	µA	—

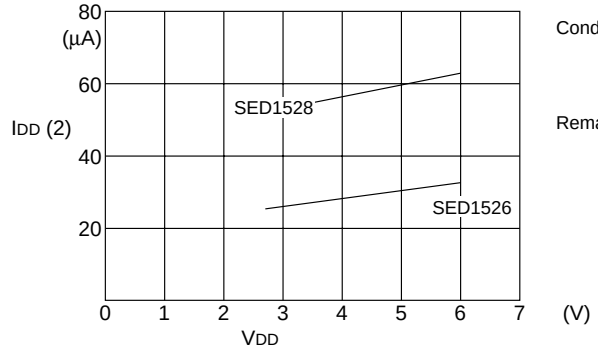
Typical current consumption characteristics (reference data)

- Dynamic current consumption (1) when LCD external power mode lamp is ON



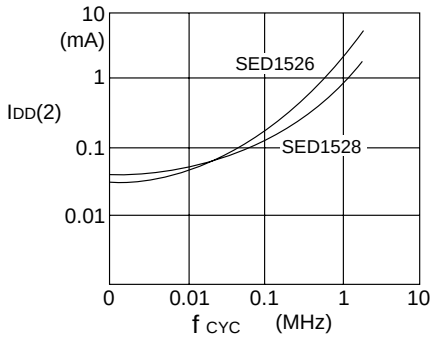
Conditions: The built-in power supply is OFF and an external power supply is used.
SED1526 V_5-V_{DD}=–6.0V
SED1528 V_5-V_{DD}=–8.0V
Ta=25°C
Remarks: *12

- Dynamic current consumption (2) when the LCD built-in power supply lamp is ON



Conditions: The built-in power supply is ON.
SED1526 V_5-V_{DD}=–6.0V dual boosting
SED1528 V_5-V_{DD}=–8.0V triple boosting
Ta=25°C
Remarks: *13

- Current consumption I_{DD} during access (2) during MPU access cycle



It shows the current consumption when a checker pattern is always written in f_{SYNC} timing.
When not accessed, only the current consumption of I_{DD} (2) occurs.

Conditions: SED1526 $V_5 - V_{DD}$ = –6.0 V, dual boosting
SED1528 $V_5 - V_{DD}$ = –8.0 V, triple boosting
Ta = 25°C

	Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Pins used
Built-in power circuit	Input voltage	V_{DD}	—	2.4	—	6.0	V	*10
	Booster output voltage	V_{OUT}	V_{DD} reference (during triple boosting)	–16.5	—	—	V	V_{OUT}
	Voltage regulator circuit operating voltage	V_{OUT}	V_{DD} reference	–16.5	—	–4.0	V	V_{OUT}
	Voltage follower operating voltage	V_5	V_{DD} reference	–13.0	—	–4.0	V	*11
	Reference voltage	V_{REG}	V_{DD} reference Ta = 25°C	–3.5	–3.1	–2.7	V	V_R

* See notes below.

*1 Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.
*2 The operating voltage range of the V_{DD} and V_5 systems (See Figure 9.)
The operating voltage range is applied if an external power supply is used.
*3 Pins D0 to D5, A0, $\overline{CS1}$, CS2, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), M/S, CL, and FR
*4 Pins D0 to D7, FR, and CL
*5 Pins SI (D7), SCL (D6), SR1, and SR2
*6 Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, SR1, and SR2
*7 Applied if pins D0 to D7, FR, and CL are high impedance.
*8 For the relationship between CL output frequency and frames, see Figure 7.
For the relationship between CL output frequency and power voltage, see Figure 8.
For the relationship between CL output frequency and temperature, see Figure 11.
*9 The resistance when the 0.1-volt voltage is applied between the SEG and COM output terminals and each power terminal (V_1, V_2, V_3 or V_4). It must be within operating voltage (2).
RON = 0.1 V/ΔI
where, ΔI is the current that flows between power supply and SEG or COM terminal when the 0.1-volt voltage is applied.
*10 If the triple voltage by the built-in power circuit are used the V_{DD} primary power must be used within the input voltage range.
*11 The V_5 voltage can be adjusted within the voltage follower operating range by use of voltage regulator.
*12 Applied if the built-in oscillation circuit is used and if not accessed by the MPU.
*13 Applied if the built-in oscillation circuit and the built-in power circuit are used, and if not accessed by the MPU.
The current flowing through the voltage regulator resistors (R1, R2 and R3) is not included.
When the built-in voltage booster is used, the current consumption for the V_{DD} power supply is shown.

- Relationship between CL output frequency and frames (SED 1526 series)

The relationship between CL output frequency (f_{CL}) and frame frequency (f_F) can be determined as follows:

	Duty	f_F
SED1526	1/9 1/17	8 • F_{OSC}/288 8 • f_{OSC}/272
SED1528	1/33	8 • f_{OSC}/264

Figure 7

("f_F" indicates the LCD current alternating cycle, but not the cycle of f F signals.)

- Relationship between CL output frequency and power voltage

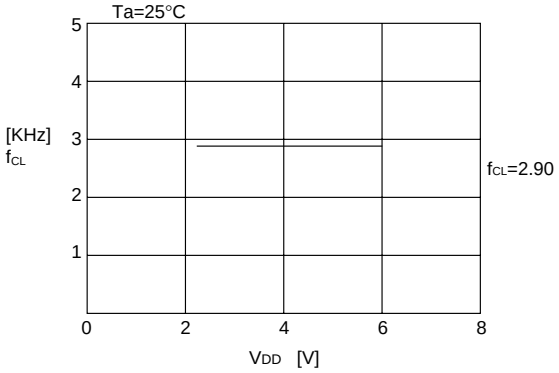
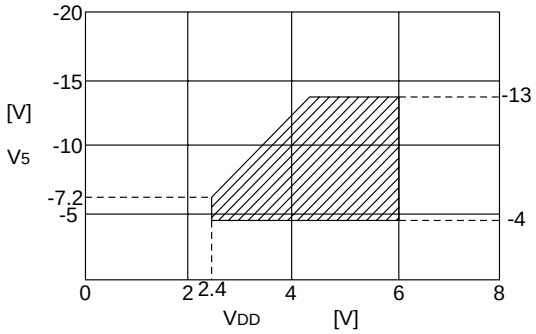
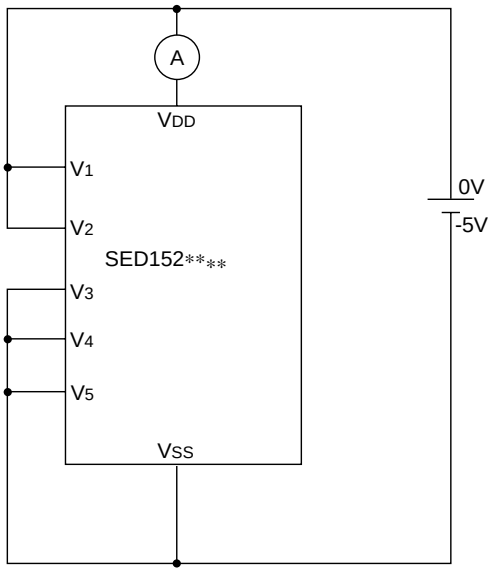


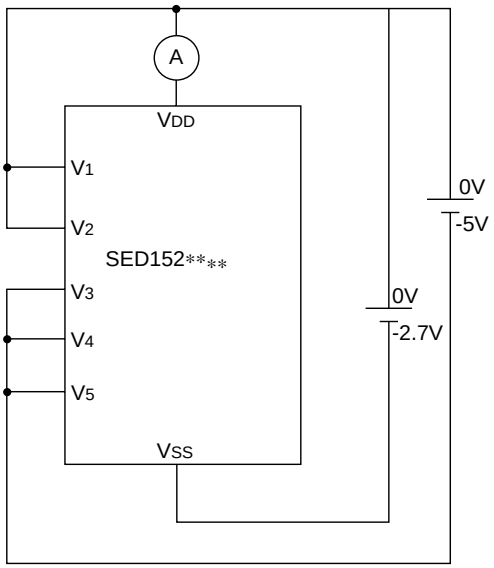
Figure 8

- Operating voltage range on V_{DD} and V_5

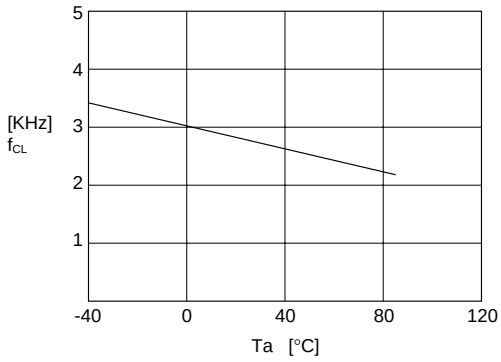


- I_{DD} measuring circuits





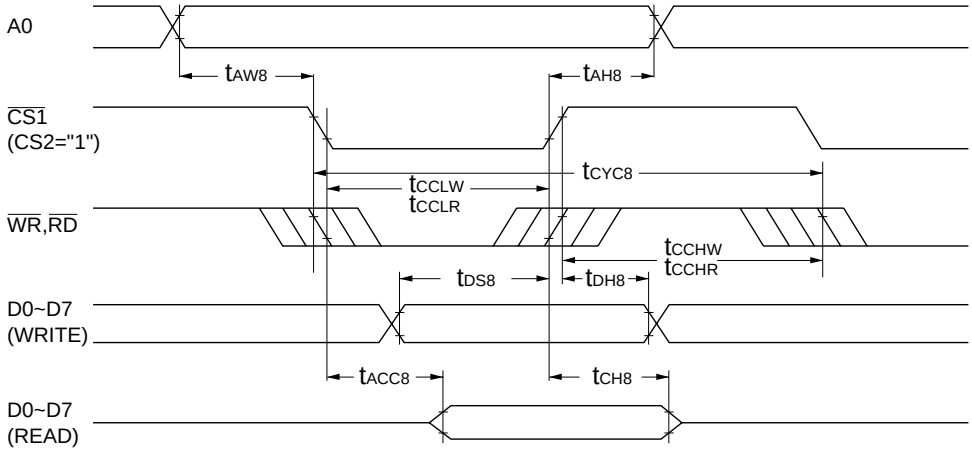
- Relationship between CL output frequency and temperature



AC Characteristics

(1) System buses

Read/write characteristics I (8080-series microprocessor)



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		5		ns
Address setup time		t_{AW8}		5		ns
System cycle time		t_{CYC8}		400		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		100		
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		75		
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		145		
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		145		
Data setup time		t_{DS8}		80		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF		80	ns
Output disable time		t_{CH8}		10	60	ns

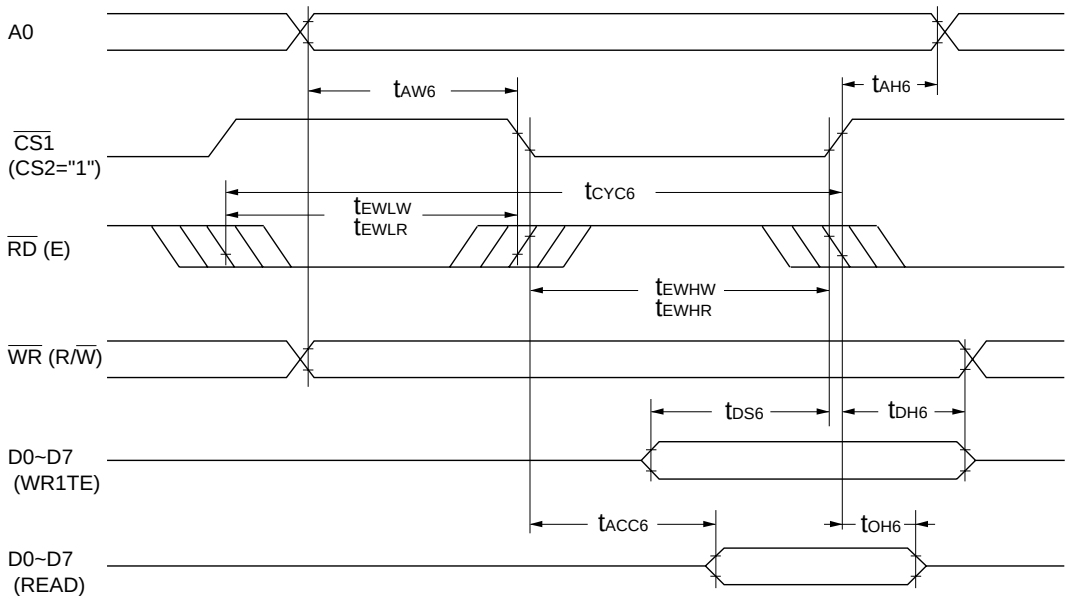
V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		10		ns
Address setup time		t_{AW8}		10		ns
System cycle time		t_{CYC8}		800		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		185		
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		185		
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		285		ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		285		ns
Data setup time		t_{DS8}		160		ns
Data hold time		t_{DH8}		20		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	CL=100pF		180	ns
Output disable time		t_{CH8}		20	120	ns

Notes: 1. t_{CCLW} and t_{CCLR} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{WR}$ or $\overline{RD}$ low.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

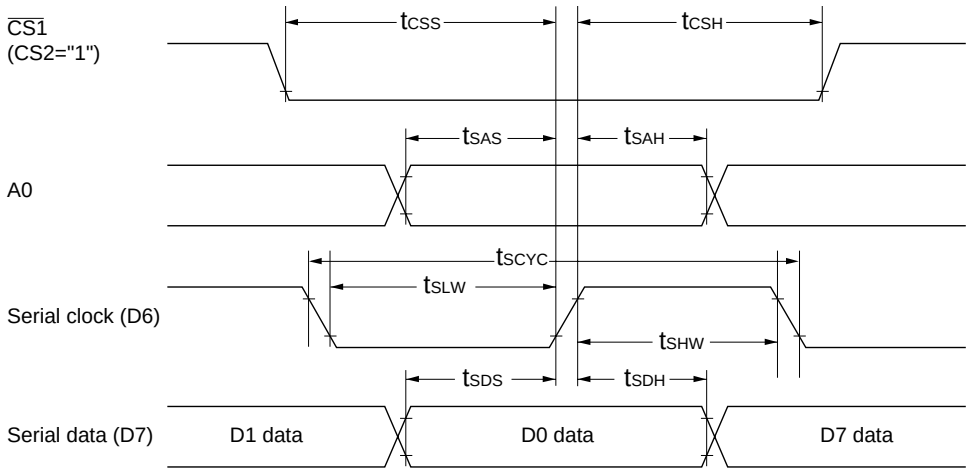
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		400		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		20 10		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 10		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	10	60 90	ns ns
Enable low pulse width	READ WRITE	$\overline{RD}$ (E)	t_{EWLR} t_{EWLW}		85 75		ns ns
Enable high pulse width	READ WRITE	$\overline{RD}$ (E)	t_{EWHR} t_{EWHW}		135 145		ns ns

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		800		ns
Address setup time Address hold time		$\overline{WR}$ (R/$\overline{W}$) A0	t_{AW6} t_{AH6}		40 20		ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		160 20		ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL=100pF	20	120 180	ns ns
Enable low pulse width	READ WRITE	$\overline{RD}$ (E)	t_{EWLR} t_{EWLW}		185 145		ns ns
Enable high pulse width	READ WRITE	$\overline{RD}$ (E)	t_{EWHR} t_{EWHW}		285 325		ns ns

Notes: 1. t_{EWHR} and t_{EWHW} are limited depending on the overlap time of $\overline{CS1}$ low (CS2 high) and $\overline{RD}$ (E) high.
2. The input signal rise and fall times must be within 15 nanoseconds.
3. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(3) Serial interface



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

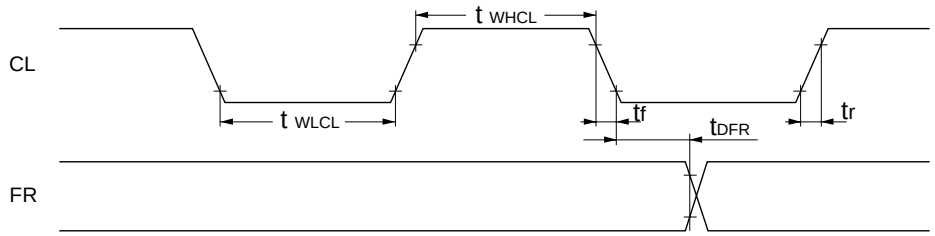
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	Serial clock	t_{SCYC}		500		ns
Serial clock H pulse width		t_{SHW}		150		ns
Serial clock L pulse width		t_{SLW}		150		ns
Address setup time	A0	t_{SAS}		120		ns
Address hold time		t_{SAH}		200		ns
Data setup time	Serial data	t_{SDS}		120		ns
Data hold time		t_{SDH}		120		ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS}		80		ns
		t_{CSH}		400		ns

V_{SS} = 0 V, V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	Serial clock	t_{SCYC}		1000		ns
Serial clock H pulse width		t_{SHW}		300		ns
Serial clock L pulse width		t_{SLW}		300		ns
Address setup time	A0	t_{SAS}		250		ns
Address hold time		t_{SAH}		400		ns
Data setup time	Serial data	t_{SDS}		250		ns
Data hold time		t_{SDH}		250		ns
$\overline{CS}$ serial clock time	$\overline{CS1}$ (CS2="1")	t_{CSS}		160		ns
		t_{CSH}		800		ns

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) Display control timing



V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	t_{WLCL}		35			µs
High level pulse width		t_{WHCL}		35			µs
Rise time		tr			30	120	ns
Fall time		tf			30	120	ns
FR delay time	FR	t_{DFR}		–1.0	0.2	1.0	µs

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level pulse width	CL	t_{WLCL}		70			µs
High level pulse width		t_{WHCL}		70			µs
Rise time		tr			60	240	ns
Fall time		tf			60	240	ns
FR delay time	FR	t_{DFR}		–2.0	0.4	2.0	µs

Output timing

V_{SS} = 0 V, V_{DD} = 5.0 V ±10%,Ta = –40 to +85°C

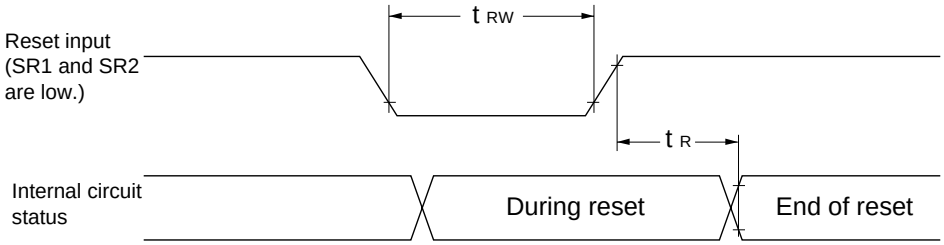
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.2	0.4	µs

V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	CL=100pF		0.4	0.8	µs

Notes: 1. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(5) Reset timing



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0			µs
Reset low pulse width	Reset input	t_{RW}		10			µs

V_{DD} = 2.7 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		3.0			µs
Reset low pulse width	Reset input	t_{RW}		30			µs

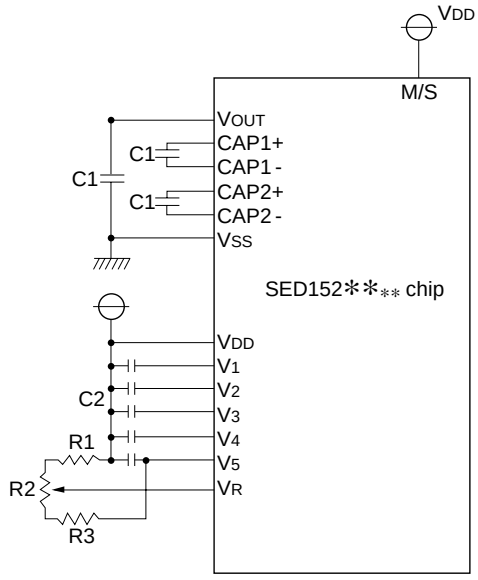
Notes: 1. t_R (reset time) represents the period from rising edge of reset input to end of internal circuit reset. The SED1526 series can operate normally after t_R.
2. t_{RW} specifies the minimum pulse width of reset input. The low pulse exceeding t_{RW} is required for reset.
3. The input signal rise and fall times must be within 15 nanoseconds.
4. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

EXTERNAL WIRINGS

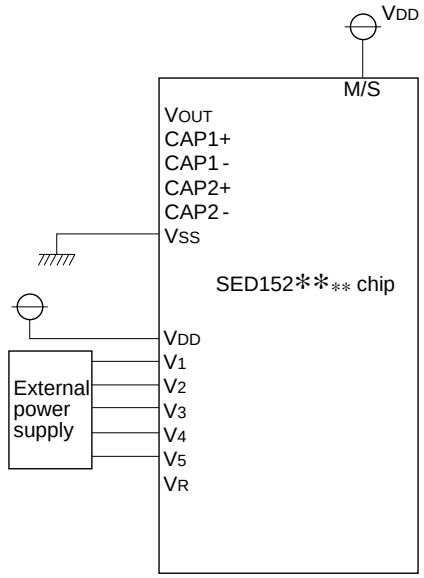
Power Supply and LCD Power Circuit

If a single SED1526 series chip is used and if on-board power supply is used and not used

If on-chip power supply is used



If on-chip power supply is NOT used



Parts list (Reference)

Variable V_5 (TBD)

C 1	0.1 to 1 µF
C 2	0.1 to 1 µF
R 1	2.0 MΩ
R 1	1.0 MΩ
R 1	3.0 MΩ

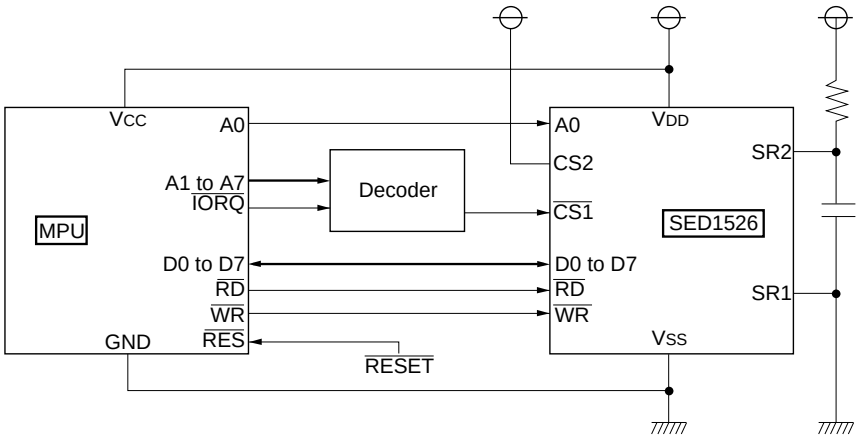
Note: Use jumper and shielded wires as the input impedance of VR terminal is high.

Microprocessor Interface

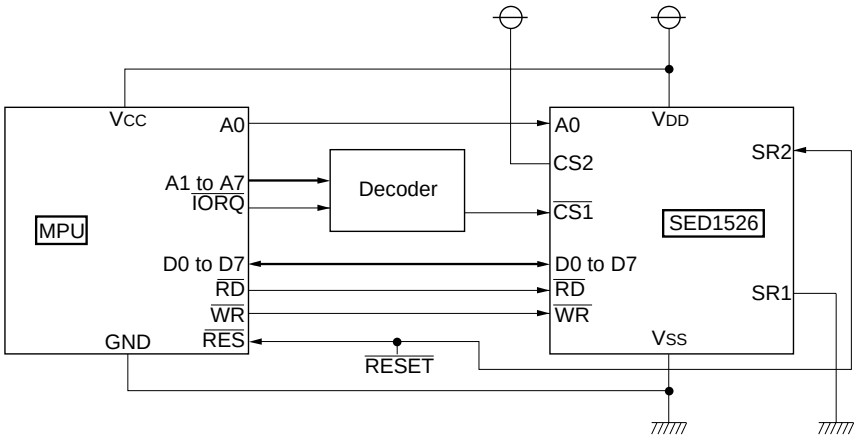
The SED1526 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them.

8080-series microprocessors

Wiring example 1:

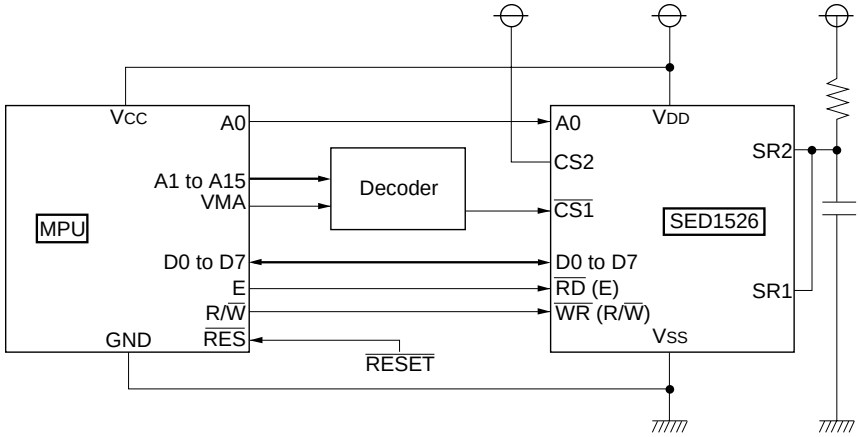


Wiring example 2:

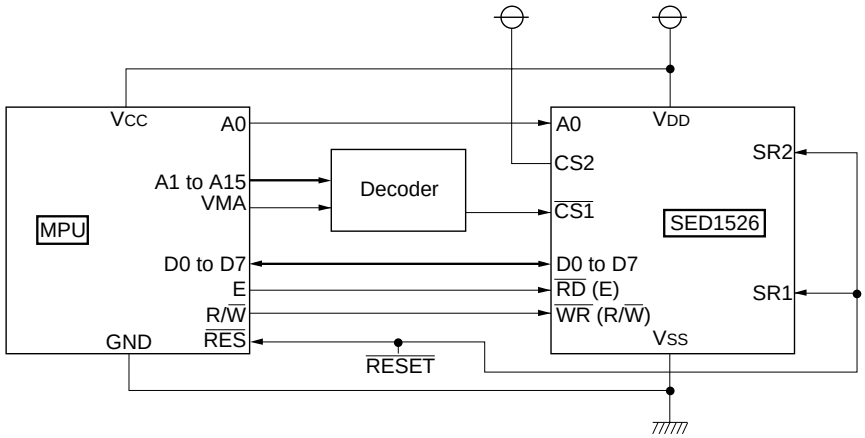


6800-series microprocessors

Wiring example 1:

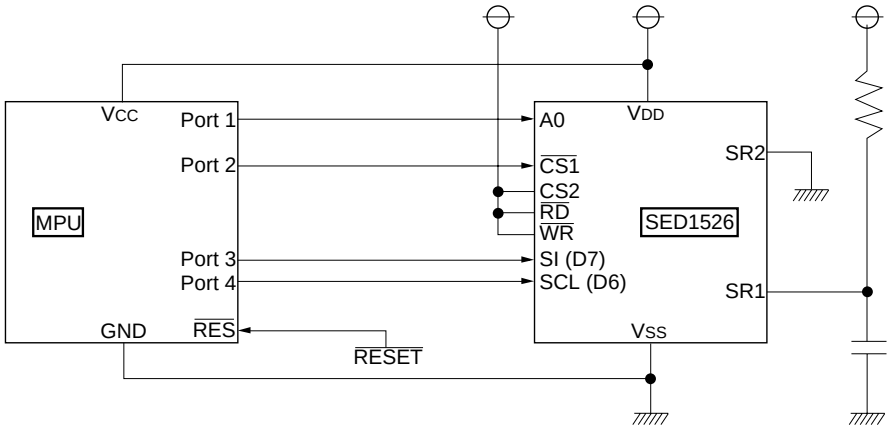


Wiring example 2:

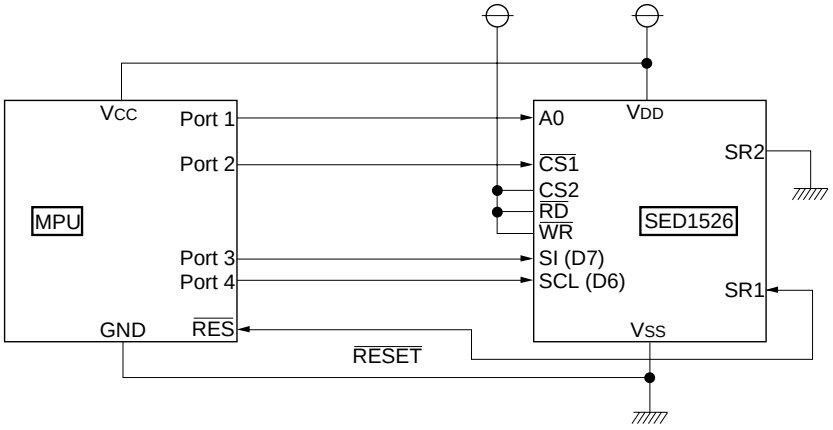


Serial interface

Wiring example 1:

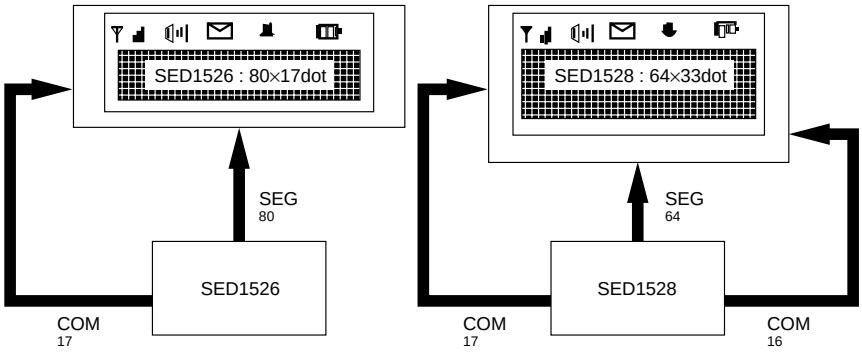


Wiring example 2:



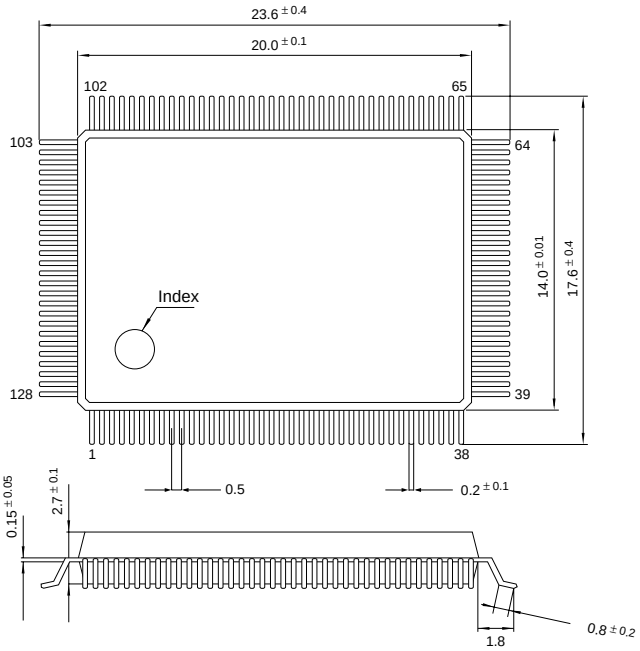
LCD Panel and Wiring Examples

Single-chip configuration



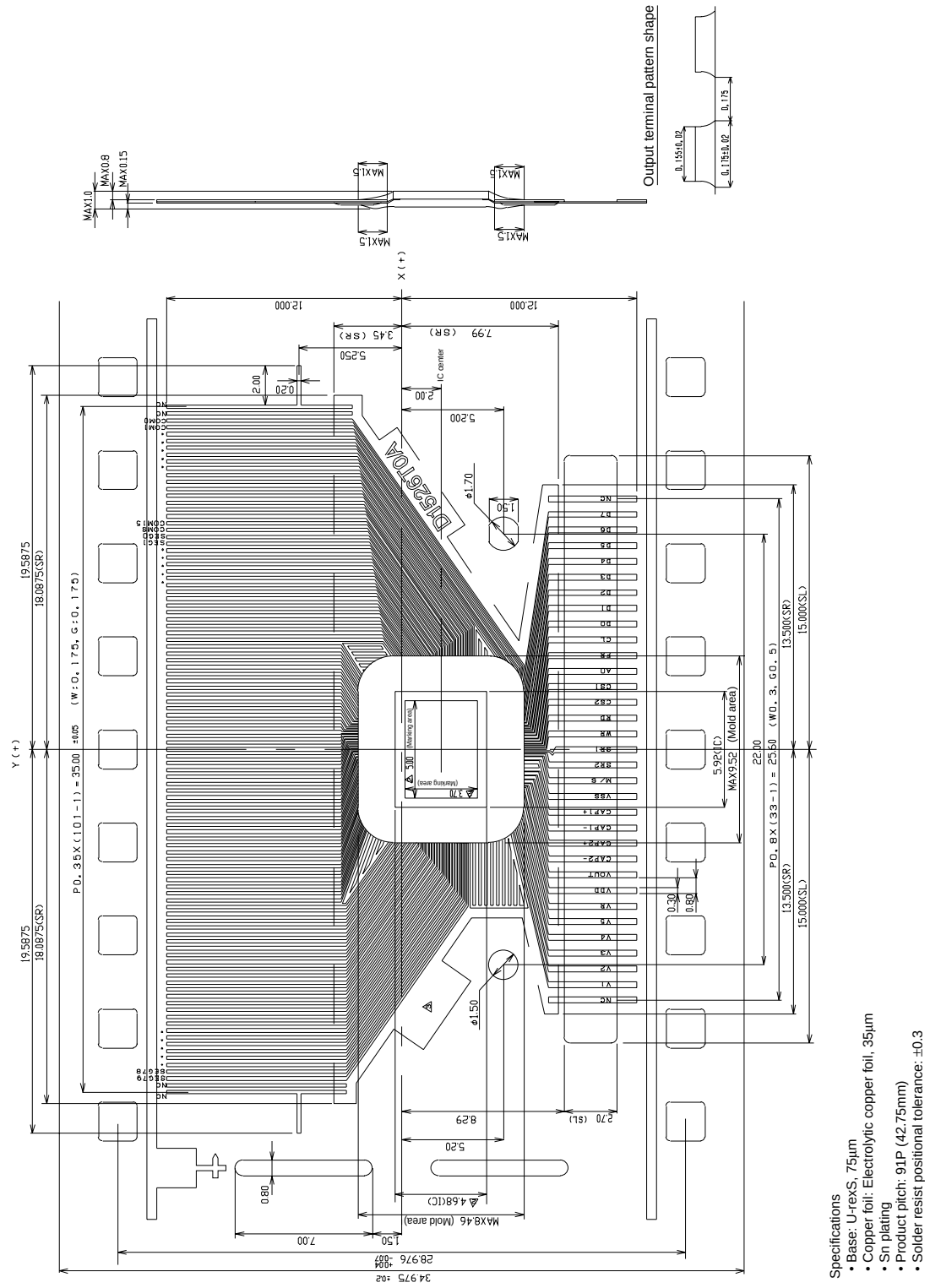
DIMENSIONS

Plastic 128-Pin QFP5 Package



The package dimensions are subject to change without notice.

TPC shape SED1526T0A (Reference drawing)



This dimensional outline drawing is subject to change for improvements without prior notice

5. SED1530 Series

Contents

OVERVIEW

The SED1530 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's) which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of microprocessor clock.

The use of the on-chip display RAM of 65 × 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

As a total of 133 circuits of common and segment outputs are incorporated, a single chip of SED1530 series can make 33 × 100-dot (16 × 16-dot kanji font: 6 columns × 2 lines) displays, and a single chip of SED1531 can make 65 × 132-dot (kanji font: 8 columns x 4 lines) displays when the SED1531 is combined with the common driver SED1635.

The SED1532 can display the 65 × 200-dot (or 12-column by 4-line Kanji font) area using two ICs in master and slave modes. As an independent static indicator display is provided for time-division driving, the low-power display is realized during system standby and others.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Two types of SED1530 series are available: one in which common outputs are arranged on a single side and the other in which common outputs are arranged on both sides.

FEATURES

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: 65 × 132 = 8580 bits
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800.
- Serial interface
- Many command functions: Read/Write Display Data, Display ON/OFF, Normal/Reverse Display, Page Address Set, Set Display Start Line, Set Column Address, Read Status, All Display ON/OFF, Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction, Power Save

• Series specifications (in cases of chip shipments)

Type 1 [V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: 0.2% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530D0∗	1/33	1/5, 1/6	100	33	33 × 100	COM single-side layout
SED1530DA∗	1/33	1/5, 1/6	100	33	33 × 100	COM dual-side layout
SED1531D0∗	1/65	1/6, 1/8	132	0	65 × 132	SED1635 is used as the COM.
SED1532D0∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
SED1532DB∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, left-hand layout
SED1535DA∗	1/35	1/5, 1/6	98	35	35 × 98	COM both-side layout

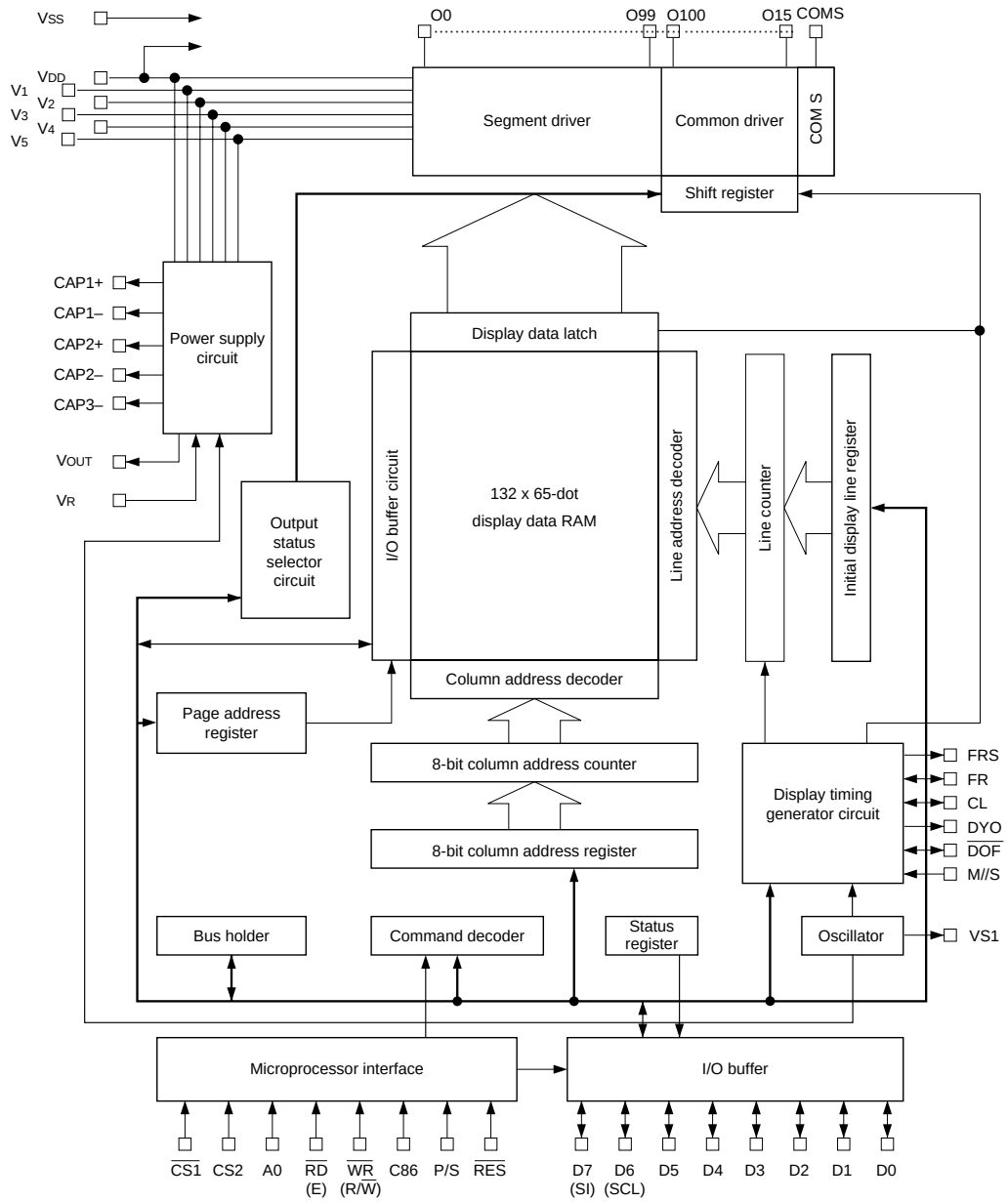
Type 2 [V_{REG} Temperature gradient: 0.00% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530DF∗	1/33	1/5, 1/6	100	33	33 × 100	COM both-side layout
SED1532DE∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
SED1533DF∗	1/17	1/5	116	17	17 × 116	COM both-side layout
SED1534DE∗	1/9	1/5	124	9	9 × 124	COM single-side layout

Note: The SED1530 series has the following subcodes depending on their shapes. (The SED1530 examples are given.)
SED1530T∗∗ : TCP (The TCP subcode differs from the inherent chip subcode.)
SED1530D∗∗ : Bear chips — SED1530D∗A : Aluminum pad
SED1530D∗B : Gold bump

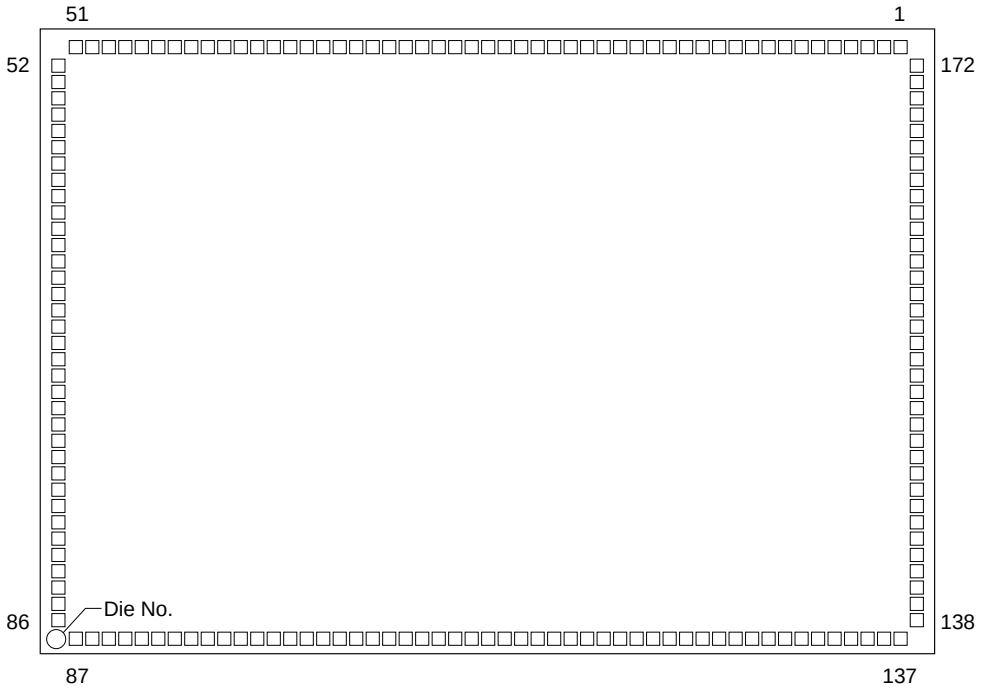
- On-chip LCD power circuit: Voltage booster, voltage regulator, voltage follower × 4.
- On-chip electronic contrast control functions
- Ultra low power consumption
- Power supply voltages: V_{DD} - V_{SS} -2.4 V to -6.0 V
  V_{DD} - V5 -4.5 V to -16.0 V
- Wide operating temperature range:
  Ta = -40 to 85°C
- CMOS process
- Package: TCP and bare chip
- Non-radiation-resistant design

BLOCK DIAGRAM (SED1530D0B)



PIN ASSIGNMENT

SED1530 series chips



Chip Size:	6.65x4.57 mm
Pad Pitch:	118 µm (Min)
SED153*D*A	(Aluminum pad model)
Pad Center Size:	90x90 µm
Chip Thickness:	300 µm
SED153*D*B	(Gold bump model)
Bump Size:	76x76 µm
Bump Height:	23µm (Typ.)
Chip Thickness:	625 µm

Pad Center Coordinates

Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	O127	2986	2142	51	O5	-2986	2142	101	O55	-1298	-2142	151	O105	3178	-472
2	O128	2862		52	O6	-3178	2006	102	O56	-1180		152	O106		-354
3	O129	2738		53	O7		1888	103	O57	-1062		153	O107		-236
4	O130	2614		54	O8		1770	104	O58	-944		154	O108		-118
5	O131	2490		55	O9		1652	105	O59	-826		155	O109		0
6	COMS	2366		56	O10		1534	106	O60	-708		156	O110		118
7	FRS	2242		57	O11		1416	107	O61	-590		157	O111		236
8	FR	2124		58	O12		1298	108	O62	-472		158	O112		354
9	DYO	2006		59	O13		1180	109	O63	-354		159	O113		472
10	CL	1888		60	O14		1062	110	O64	-236		160	O114		590
11	$\overline{DOF}$	1770		61	O15		944	111	O65	-118		161	O115		708
12	VS1	1652		62	O16		826	112	O66	0		162	O116		826
13	M/S	1534		63	O17		708	113	O67	118		163	O117		944
14	$\overline{RES}$	1416		64	O18		590	114	O68	236		164	O118		1062
15	P/S	1298		65	O19		472	115	O69	354		165	O119		1180
16	$\overline{CS1}$	1180		66	O20		354	116	O70	472		166	O120		1298
17	CS2	1062		67	O21		236	117	O71	590		167	O121		1416
18	C86	944		68	O22		118	118	O72	708		168	O122		1534
19	A0	826		69	O23		0	119	O73	826		169	O123		1652
20	$\overline{WR}$(W/$\overline{R}$)	708		70	O24		-118	120	O74	944		170	O124		1770
21	$\overline{RD}$(E)	590		71	O25		-236	121	O75	1062		171	O125		1888
22	V_{DD}	354		72	O26		-354	122	O76	1180		172	O126		2006
23	D0	236		73	O27		-472	123	O77	1298					
24	D1	236		74	O28		-590	124	O78	1416					
25	D2	118		75	O29		-708	125	O79	1534					
26	D3	0		76	O30		-826	126	O80	1652					
27	D4	-118		77	O31		-944	127	O81	1770					
28	D5	-236		78	O32		-1062	128	O82	1888					
29	D6(SCL)	-354		79	O33		-1180	129	O83	2006					
30	D7(SI)	-472		80	O34		-1298	130	O84	2124					
31	V_{SS}	-590		81	O35		-1416	131	O85	2242					
32	V_{OUT}	-708		82	O36		-1534	132	O86	2366					
33	CAP3-	-826		83	O37		-1652	133	O87	2490					
34	CAP1+	-944		84	O38		-1770	134	O88	2614					
35	CAP1-	-1062		85	O39		-1888	135	O89	2738					
36	CAP2+	-1180		86	O40		-2006	136	O90	2862					
37	CAP2-	-1298		87	O41	-2986	-2142	137	O91	2986					
38	V_5	-1416		88	O42	-2862		138	O92	3178	-2006				
39	V_R	-1534		89	O43	-2738		139	O93		-1888				
40	V_{DD}	-1652		90	O44	-2614		140	O94		-1770				
41	V_1	-1770		91	O45	-2490		141	O95		-1652				
42	V_2	-1888		92	O46	-2366		142	O96		-1534				
43	V_3	-2006		93	O47	-2242		143	O97		-1416				
44	V_4	-2124		94	O48	-2124		144	O98		-1298				
45	V_5	-2242		95	O49	-2006		145	O99		-1180				
46	O0	-2366		96	O50	-1888		146	O100		-1062				
47	O1	-2490		97	O51	-1770		147	O101		-944				
48	O2	-2614		98	O52	-1652		148	O102		-826				
49	O3	-2738		99	O53	-1534		149	O103		-708				
50	O4	-2862		100	O54	-1416		150	O104		-590				

PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5V power supply. Connect to microprocessor power supply pin V_{CC}.	2
V_{SS}	Supply	Ground	1
V_1, V_2 V_3, V_4 V_5	Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command. (The SED1533 and SED1534 are fixed to 1/5 bias.)	6

	SED1530/SED1535	SED1531	SED1532
V_1	1/5•V_5 1/6•V_5	1/6•V_5 1/8•V_5	1/6•V_5 1/8•V_5
V_2	2/5•V_5 2/6•V_5	2/6•V_5 2/8•V_5	2/6•V_5 2/8•V_5
V_3	3/5•V_5 4/6•V_5	4/6•V_5 6/8•V_5	4/6•V_5 6/8•V_5
V_4	4/5•V_5 5/6•V_5	5/6•V_5 7/8•V_5	5/6•V_5 7/8•V_5

	SED1533	SED1534
V_1	1/5•V_5	1/5•V_5
V_2	2/5•V_5	2/5•V_5
V_3	3/5•V_5	3/5•V_5
V_4	4/5•V_5	4/5•V_5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
CAP3–	O	DC/DC voltage converter capacitor 1 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit microprocessor data bus. When the serial interface selects; D7: Serial data input (SI) D6: Serial clock input (SCL)	8
A0	I	Control/display data flag input. It is connected to the LSB of micro-processor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
$\overline{RES}$		When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is low and CS2 is high. When chip select is non-active, D0 to D7 will be "HZ".	2
RD (E)	I	• When interfacing to an 8080 series microprocessor: Active low. This input connects the RD signal of the 8080 series microprocessor. While this signal is low, the SED1530 series data bus output is enabled. • When interfacing to a 6800 series microprocessor: Active high. This is used as an enable clock input pin of the 6800 series microprocessor.	1

Name	I/O	Description	Number of pins
$\overline{WR}$ (R/$\overline{W}$)	I	• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active low. • When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is high and it will be write mode when R/$\overline{W}$ is low. R/$\overline{W}$ = "1":Read R/$\overline{W}$ = "0":Write	1
C86	I	Microprocessor interface select terminal. C86 = high: 6800 series microprocessor interface C86 = low: 8080 series microprocessor interface	1
P/S	I	Serial data input/parallel data input select pin. P/S | Chip select | Data/command | Data | Read/write | Serial clock "H" | $\overline{CS1}$, CS2 | A0 | D0-D7 | $\overline{RD}$, $\overline{WR}$ | — "L" | $\overline{CS1}$, CS2 | A0 | SI(D7) | Write only | SCL(D6) * In serial mode, no data can be read from RAM. When P/S = low, D0 to D5 are HZ and $\overline{RD}$ and $\overline{WR}$ must be fixed high or low.	1

LCD Driver Outputs

Name	I/O	Description	Number of pins
M/S	I	SED1530 series master/slave mode select input. When a necessary signal is output to the LCD, the master operation is synchronized with the LCD system, while when a necessary signal is input to the LCD, the slave operation is synchronized with the LCD system. M/S = high: Master operation M/S = low : Slave operation The following is provided depending on the M/S status. Model | Status | OSC circuit | Power supply circuit | CL | FR | DYO | FRS | DOF SED153*D** | Master | Enabled | Enabled | Output | Output | Output | Output | Output Slave | Disabled | Disabled | Input | Input | HZ | HZ | Input	1
CL	I/O	Display clock input/output. When the SED1530 series selects master/slave mode, each CL pin is connected. When it is used in combination with the common driver, this input/output is connected to common driver YSCL pin. M/S = high: Output M/S = low: Input	1
FR	I/O	LCD AC signal input/output. When the SED1530 series selects master/slave mode, each FR pin is connected. When the SED1530 series selects master mode this input/output is connected to the common driver FR pin. M/S = high: Output M/S = low: Input	1
DYO	I/O	Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pin. It becomes HZ at slave operation.	1
VS1	O	Internal power supply voltage monitor output.	1
$\overline{DOF}$	I/O	LCD blanking control input/output. When the SED1530 series selects master/slave mode, the respective $\overline{DOF}$ pin is connected. When it is used in combination with the common driver (SED1635), this output/input is connected to the common driver $\overline{DOFF}$ pin. M/S = high: Output M/S = low: Input	1
FRS	O	Static drive output. This is enabled only at master operation and used together with the FR pin. This output becomes HZ at slave operation.	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>On
(SEG n)
(Com n)</td><td>O</td><td>
LCD drive output. The following assignment is made depending on the model.
<table>
<tr><th></th><th>SEG</th><th>COM</th></tr>
<tr><td>SED1530D0*</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>SED1530DA*
SED1530DF*</td><td>O16~O115</td><td>O0~O15, O116~O131</td></tr>
<tr><td>SED1531D0*</td><td>O0~O131</td><td></td></tr>
<tr><td>SED1532D0*
SED1532DE*</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>SED1532DB*</td><td>O32~O131</td><td>O0~O31</td></tr>
<tr><td>SED1533DF*</td><td>O8~O123</td><td>O0~O7, O124~O131</td></tr>
<tr><td>SED1534DE*</td><td>O0~O123</td><td>O124~O131</td></tr>
<tr><td>SED1535DA*</td><td>O18~O115</td><td>O6~O17, O116~O131</td></tr>
</table>
SEG output. LCD segment drive output. One of V_{DD}, V_2, V_3 and V_5 levels is selected by combination of the contents of display RAM and FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">On output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">0</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{DD}</td></tr>
</table>
COM output. LCD common drive output. One of V_{DD}, V_1, V_4 and V_5 levels is selected by combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>On output voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table>
</td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. When it is not used, it is made open.
Effective only with the SED1530, SED1532, SED1533 and SED1534, SED1535 and “HZ” with the SED1531.
When multiple numbers of the SED1530, SED1532, SED1533 and SED1534, SED1535 are used, the same COMS signal is output to both master and slave units.</td><td></td></tr>
<tr><td></td><td></td><td>Total</td><td>172</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED1530 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). When high or low is selected for the polarity of P/S pin, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, RAM data cannot be read out.

Table 1

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
H	Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
L	Serial input	$\overline{CS1}$	CS2	A0	–	–	–	SI	SCL	(HZ)

"–" must always be high or low.

Parallel input

When the SED1530 series selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pin to go high or low as shown in Table 2.

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
H	6800 micro-processor bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
L	8080 micro-processor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{RW}$	D0 to D7

Data Bus Signals

The SED1530 series identifies the data bus signal according to A0, E, R/$\overline{W}$, ($\overline{RD}$, $\overline{WR}$) signals.

Table 3

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.

Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock (SCL) goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.

The serial data input (S1) is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.

Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

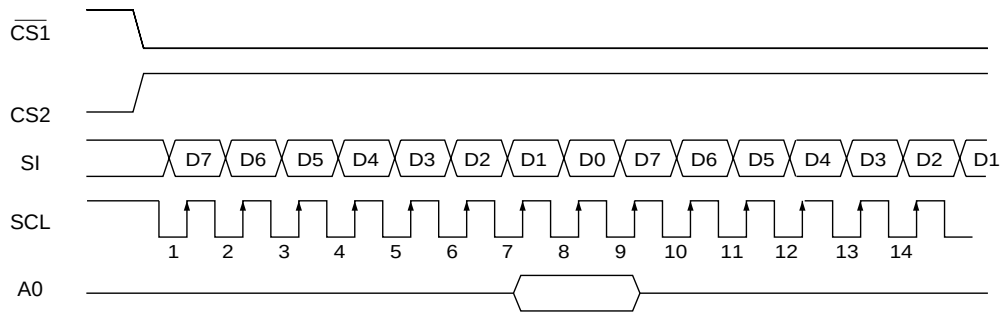


Figure 1

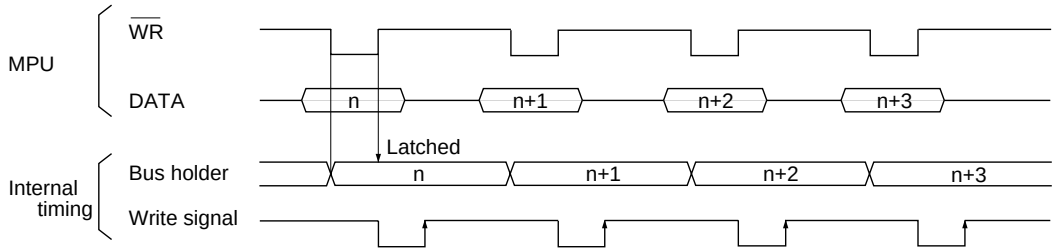
Chip Select Inputs

The SED1530 series has two chip select pins, $\overline{CS1}$ and CS2 and can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high. When these pins are set to any other combination, D0 to D7 are high impedance and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled.
When serial input interface is selected, the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The SED1530 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the SED1530 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

•Write



•Read

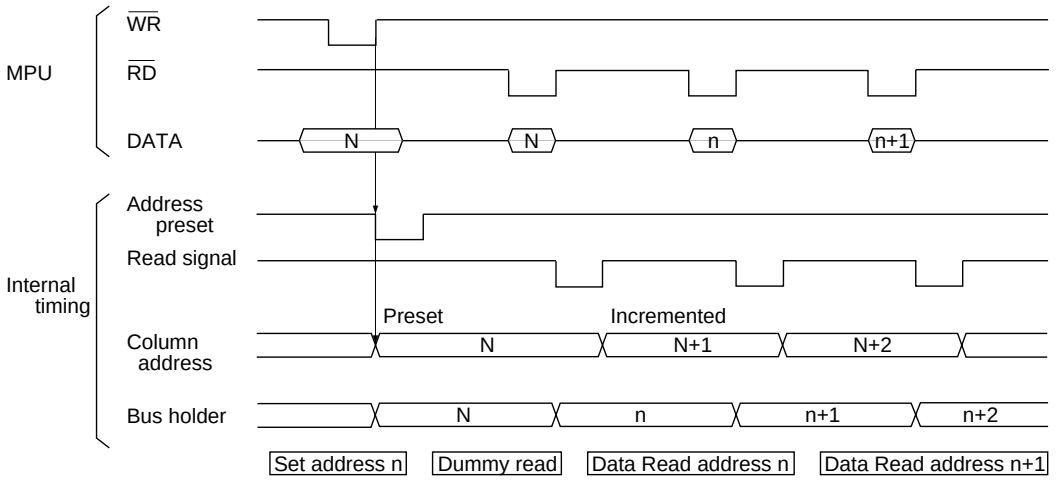


Figure 2

Busy Flag

The Busy flag is set when the SED1530 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 6-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by CL signal and it generates a line address to allow 132-bit

Column Address Counter

This is a 8 bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2, D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 65-column by 132-row (8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1530's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

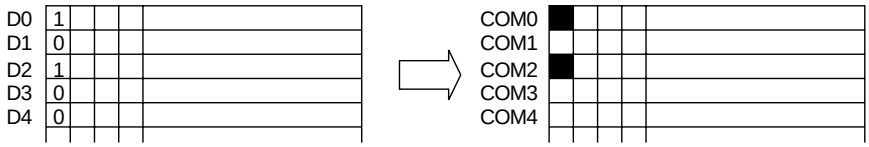


Figure 3

Relationship between display data RAM and addresses (if initial display line is 1CH):

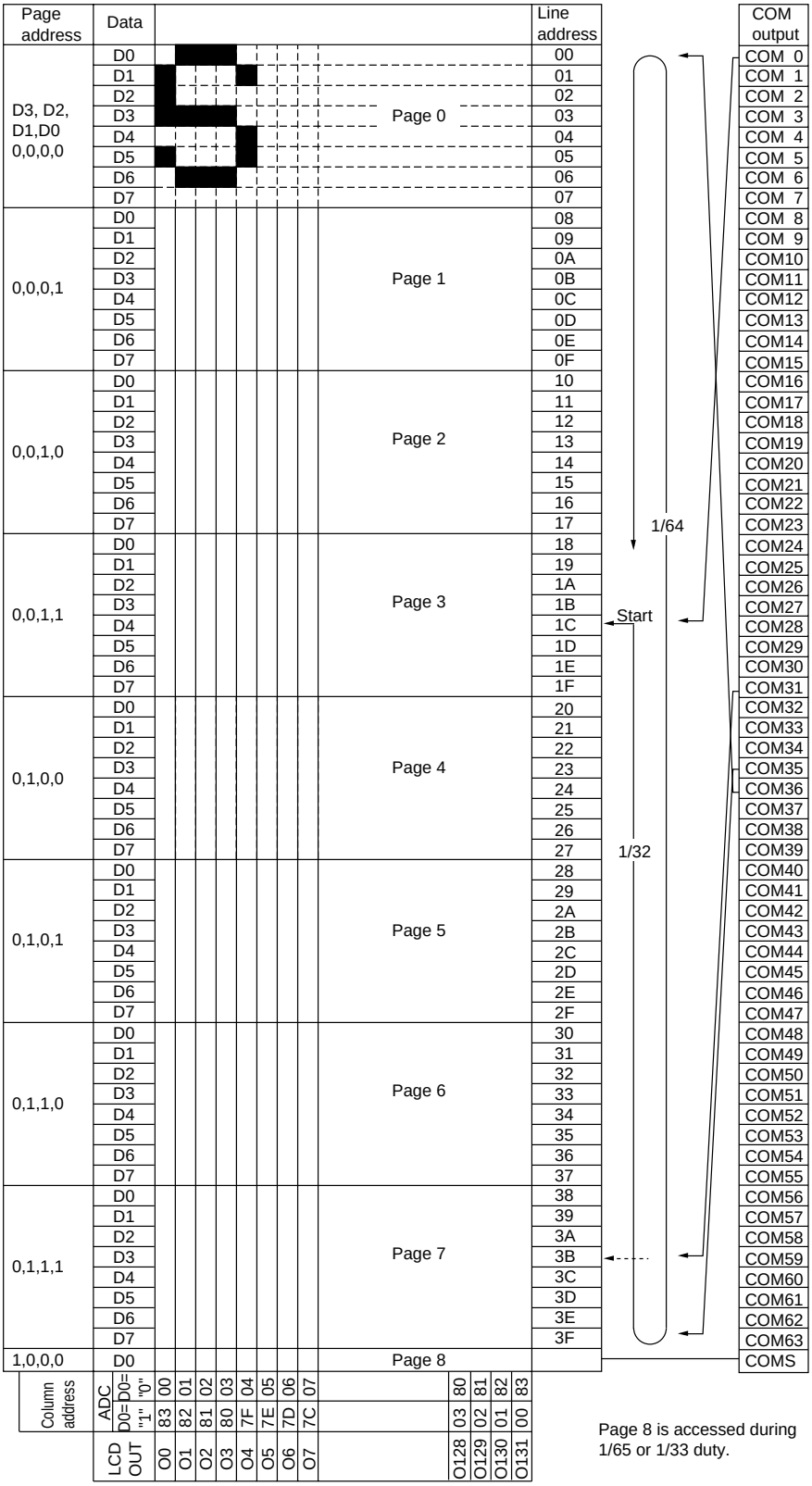


Figure 4

Output Status Selector

The SED1530 series except SED1531 can set a COM output scan direction to reduce restrictions at LCD module assembly. This scan direction is set by setting "1" or "0" in the output status register D3. Fig.5 shows the status.

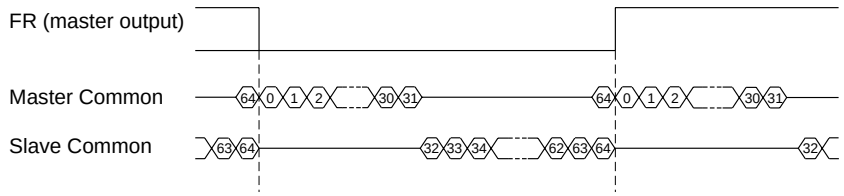
Fig. 5 shows the status.

LCD output		O0		O131
ADC (D0)	"0"	0 (H) →	Column address	→ 83 (H)
	"1"	83 (H) ←		← 0 (H)
		Display data RAM		

	D3			
SED1530D0*	0	SEG100		COM0 ---------- COM31
	1	SEG100		COM31---------- COM0
SED1530DA*	0	COM15--0	SEG100	COM16--31
SED1530DF*	1	COM16--31	SEG100	COM15--0
SED1531D0*	–	SEG132		
SED1532D0*	0	SEG100		COM0 ---------- COM31
SED1532DE*	1	SEG100		COM31---------- COM0
SED1532DB*	0	COM31---------- 0	SEG100	
	1	COM0 ---------- 31	SEG100	
SED1533DF*	0	COM7 --0	SEG116	COM8 --15
	1	COM8 --15	SEG116	COM7 --0
SED1534DE*	0	SEG124		COM0 --7
	1	SEG124		COM7 --0
SED1535DA*	0	COM17--0	SEG98	COM18--33
	1	COM18--33	SEG98	COM17--0

The COMS pin is assigned to COM32 on SED1530 and it is assigned to COM64 on SED1532 independent from their output status. The COMS pin of the SED1533 is assigned to COM16 and the COMS pin of the SED1534 is assigned to COM8.

Figure 5 shows the COM output pin numbers of SED1532D0* and SED1532DB* in the master mode. In the slave mode, COM0 to COM31 must be replaced by COM32 to COM63.



Display Timing Generator

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 132-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC signal (FR) generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform.
It generates a 2-frame AC drive waveform.

When the SED1530 is operated in slave mode on the assumption of multi-chip, the FR pin and CL pin become input pins.

Common timing signal generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pin.
When an AC signal (FR) is switched, a high pulse is output as a DYO output at the training edge of the previous display clock.
Refer to Fig. 6. The DYO output is output only in master mode.
When the SED1530 series is used for multi-chip, the slave requires to receive the FR, CL, $\overline{DOF}$ signals from the master.
Table 4 shows the FR, CL, DYO and $\overline{DOF}$ status.

Table 4

Model	Operation mode	FR	CL	DYO	$\overline{DOF}$
SED153*D**	Master	Output	Output	Output	Output
	Slave	Input	Input	Hz	Input

HZ denotes a high-impedance status.

Example of SED1530D0B 1/33 duty

- **Dual-frame AC driver waveforms**

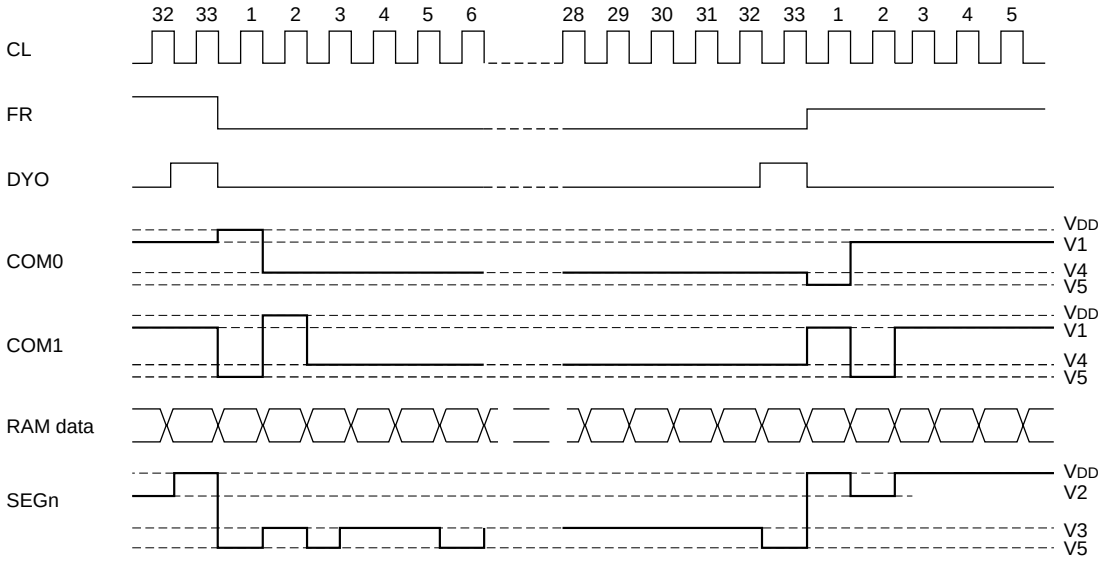


Fig. 6

Display Data Latch Circuit.

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/in reverse Display ON/OFF and Static All-display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 133 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 8 gives an example of SEG and COM output waveforms.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for voltage booster circuit of the LCD power supply.
The oscillator circuit is available in master mode only.
The oscillator signal is divided and output as display clock at CL pin.

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in SED1530 master mode only. The power supply circuit consists of a voltage booster voltage regulator, and LCD drive voltage follower.
The power supply circuit built in the SED1530 series is set for a small-scale LCD panel and is inappropriate to a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.

The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]
Status 1: To use only the internal power supply.
Status 2: To use only the voltage regulator and voltage follower.
Status 3: To use only the voltage follower. input the external voltage as V5=Vout.
Status 4: To use only an external power supply because the internal power supply does not operate.

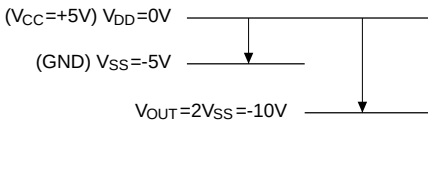
* The voltage booster terminals are CAP1+, CAP1-, CAP2+, CAP2- and CAP3-.
* Combinations other than those shown in the above table are possible but impractical.

	D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
①	1 1 1	ON	ON	ON	—	Used	Used
②	0 1 1	OFF	ON	ON	V_{OUT}	OPEN	Used
③	0 0 1	OFF	OFF	ON	V_5	OPEN	OPEN
④	0 0 0	OFF	OFF	OFF	V_1 to V_5	OPEN	OPEN

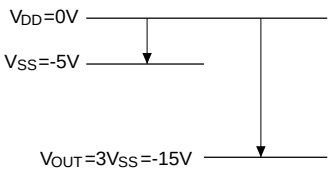
Booster circuit

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, CAP1+ and CAP3- and VSS and VOUT, the potential between VDD and VSS is boosted to quadruple toward the negative side and it is output at VOUT.
For triple boosting, remove only capacitor C1 between CAP+1 and CAP3- from the connection of quadruple boosting operation and jumper between CAP3- and VOUT. The triple boosted voltage appears at VOUT (CAP3-).

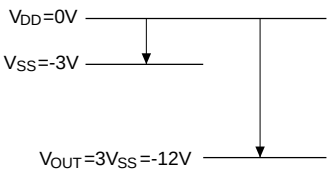
For double boosting, remove only capacitor C1 between CAP2+ and CAP2- from the connection of triple boosting operation, open CAP+2 and jumper between CAP2- and VOUT (CAP3-). The double boosted voltage appears at VOUT (CAP3-, CAP2-).
For quadruple boosting, set a VSS voltage range so that the voltage at VOUT may not exceed the absolute maximum rating.
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must operate.
Subsection 10.1.1 gives an external wiring example to use master and slave chips when on-board power supply is active.



Potential during double boosting



Potential during triple boosting



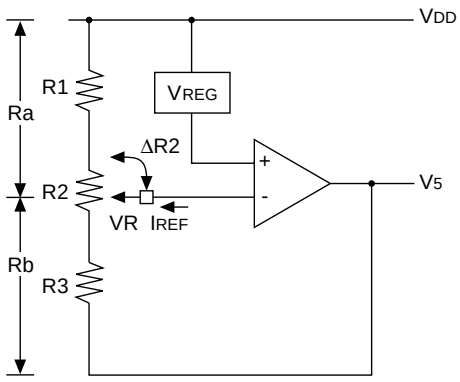
Potential during quadruple boosting

Voltage regulator circuit

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) V_{REG} + I_{REF} \cdot Rb$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) V_{REG} + I_{REF} \cdot (R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and in case of Type 1, it is constant and $V_{REG} \fallingdotseq -2.55$ V (if V_{DD} is 0 V), In case of Type 2, $V_{REG}=V_{SS}$ (V_{DD} basis). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots \textcircled{1}$$

(As I_{REF} = 0 A)

- R1 + R2 + R3 = 5MΩ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 V_5 = –6 to –10 V
  (Determined by the LCD characteristics)
  ΔR2 = OΩ, V_{REG} = –2.55V
  To obtain V_5 = -10 V, from equation ①:
  R2 + R3 = 2.92 × R1 ..... ③
  ΔR2 = R2, V_{REG} = –2.55V
  To obtain V_5 = -6 V, from equation ①:
  1.35 × (R1 + R2) = R3 ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator circuit has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the V_R pin has a high input impedance, the shielded and short lines must be protected from a noise interference.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) V_{REG} + Rb \times \Delta I_{REF} \quad \cdots\cdots \textcircled{5}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.55V±0.20V (Type1)	V_{REG} = –0.2%/°C
V_{REG} = V_{SS} (V_{DD} basis) (Type2)	V_{REG} = –0.00%/°C
I_{REF} = –3.2µA±40% (For 16 levels)	I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)	0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

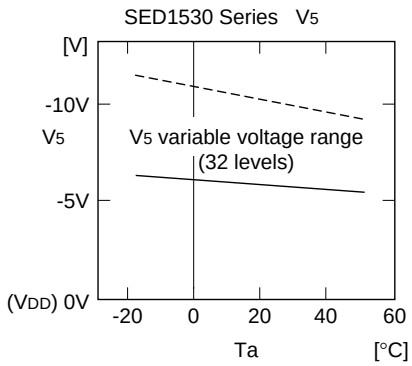
$$R3 = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{4V}{6.5\mu A} \quad \underline{Rb = 625K\Omega}$$

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5max}{V_{REG}} - 1} = \frac{625k\Omega}{\frac{-6V}{-2.55V} - 1} \qquad \underline{Ra = 462K\Omega}$$

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (-2.55V)$
$= -6.0V$
$V_5min = V_5 max + Rb \times I_{REF}$
$= -6V + 625k \times (-6.5\mu A)$
$= -10.0V$



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=–10°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (-10°C-25°C)\}$
$= -6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= -6.42V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times (-10°C-25°C)\}$
$= -11.63V$

Ta=–50°C

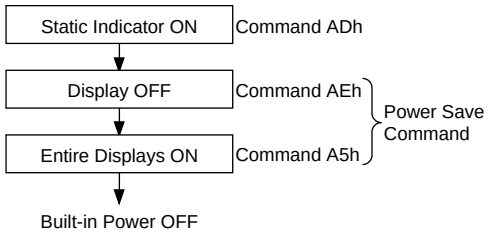
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (50°C-25°C)\}$
$= -5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= -5.7V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times (50°C-25°C)\}$
$= -8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.

In case of Type 2, it so becomes that V_{REG} = V_{SS} (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

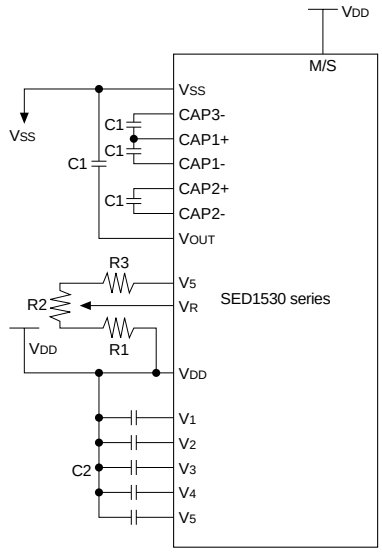
Command Sequence when Built-in Power Supply is Turned OFF

To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system into the standby mode.

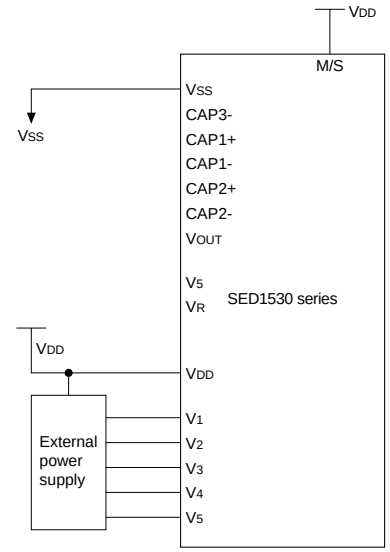


Voltage generator circuit

when the on-chip power circuit is used



when the on-chip power circuit is used



Reference setup value: SED1530 $V_5 \fallingdotseq$ -7 to -9 V
SED1531 $V_5 \fallingdotseq$ -11 to -13 V (variable)
SED1532 $V_5 \fallingdotseq$ -11 to -13 V (variable)

	SED1530	SED1531	SED1532
C1	1.0~4.7 uF	1.0~4.7 uF	1.0~4.7 uF
C2	0.22~0.47 uF	0.47~1.0 uF	0.47~1.0 uF
R1	700 KΩ	1 MΩ	1 MΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	1.6 MΩ	4 MΩ	4 MΩ
LCD SIZE	16 × 50 mm	32 × 64 mm	32 × 100 mm
DOT CONFIGURATION	32 × 100	64 × 128	64 × 200

1: As the input impedance of V_R is high, a noise protection using short wire and cable shield is required.

*2: C1 and C2 depend on the capacity of the LCD panel to be driven. Set a value so that the LCD drive voltage may be stable.

[Setup example]
Turn on the voltage regulator and voltage follower and give an external voltage to V_{OUT}. Display a horizontal-stripe LCD heavy load pattern and determine C2 so that the LCD drive voltage (V_1 to V_5) may be stable. However, the capacity value of C2 must be all equal. Next, turn on all the on-board power supplies and determine C1.

*3: LCD SIZE means the length and breadth of the display portion of the LCD panel.

Model	LCD drive voltage
SED1530	1/5 or 1/6 bias
SED1531 SED1532	1/6 or 1/8 bias

Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized status

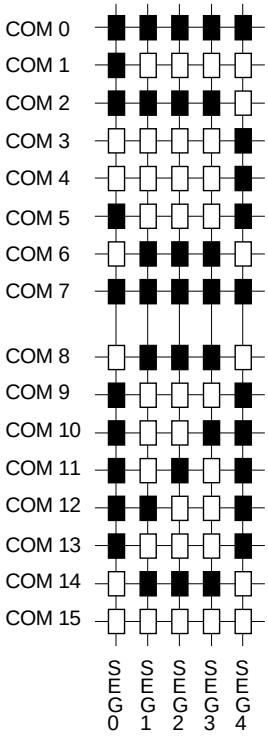
1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = low)
4. Read modify write OFF
5. Power control register (D2, D1, D0) = (0, 0, 0)
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/6 (SED1530), 1/8 (SED1531, SED1532)
8. Static indicator: OFF
9. Display start line register set at line 1
10. Column address counter set at address 0
11. Page address register set at page 0
12. Output status register (D3) = (0)
13. Electronic control register set at 0
14. Test command OFF

As seen in 11. Microprocessor Interface (Reference Example), connect the $\overline{RES}$ pin to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the SED1530 series does not use the internal LCD power supply circuit, the $\overline{RES}$ must be low when the external LCD power supply is turned on.

When $\overline{RES}$ goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pins (FR, CL, DYO, D0 to D7).
The initialization by $\overline{RES}$ pin signal is always required during power-on. If the control signal from the MPU is HZ, an overcurrent may flow through the IC. A protection is required to prevent the HZ signal at the input pin during power-on.

Be sure to initialize it by $\overline{RES}$ pin when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the above initialization are executed.


COM 0
COM 1
COM 2
COM 3
COM 4
COM 5
COM 6
COM 7
COM 8
COM 9
COM 10
COM 11
COM 12
COM 13
COM 14
COM 15
SEG 0
SEG 1
SEG 2
SEG 3
SEG 4

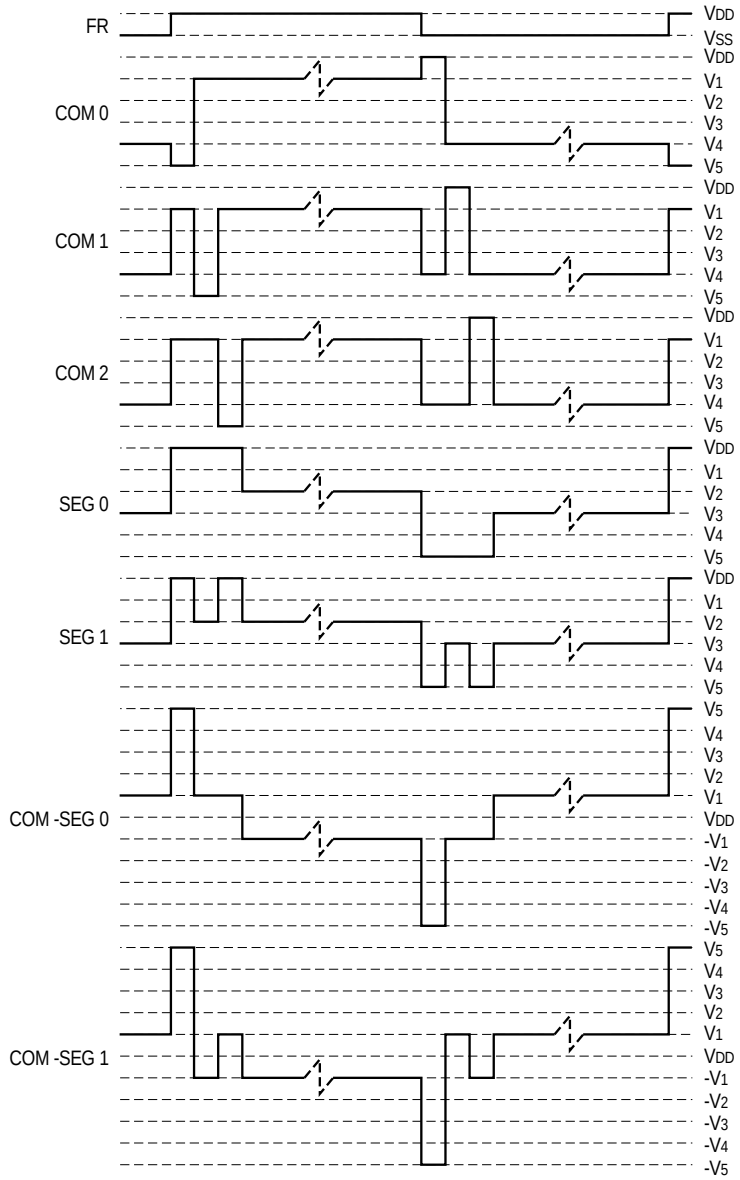

FR
VDD
VSS
COM 0
V1
V2
V3
V4
V5
COM 1
COM 2
SEG 0
SEG 1
COM -SEG 0
-V1
-V2
-V3
-V4
-V5
COM -SEG 1

Figure 8

COMMANDS

The SED1530 series uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pin and a write status when a low pulse is input to the $\overline{WR}$ pin. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pin and a write status when a low pulse is input to this pin. When a high pulse is input to the E pin, the command is activated. (For timing, see Timing Characteristics.) Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (high) when the 6800 series microprocessor interface reads status or display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands will be explained below.
When the serial interface is selected, input data starting from D7 in sequence.

• Command set

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Start Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	6 2
1	1	1	1	1	1	6 3

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(4) Set Column Address
Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	1 3 1

(5) Read Status

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: When high, the SED1526 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "131-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by Reset command. When low, the display is on. When high, the chip is being reset.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data
Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select
Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Normal/Reverse Display
Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).
When D is high, the RAM data is low, being LCD ON potential (reverse display).

(10) Entire Display ON
Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided.
If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias
Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.
(The LCD bias setting command is invalid for the SED1533 and SED1534. They are being fixed to the 1/5 bias.)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

The potential V_5 is resistively divided inside the IC to produce potentials V_1, V_2, V_3 and V_4 which are necessary to drive the LCD. The bias ratio can be selected using the LCD bias setting command. (The SED1533 and SED1534 are fixed to 1/5 bias.)
Moreover, the potentials V_1, V_2, V_3 and V_4 are converted in the impedance and supplied to the LCD drive circuit.

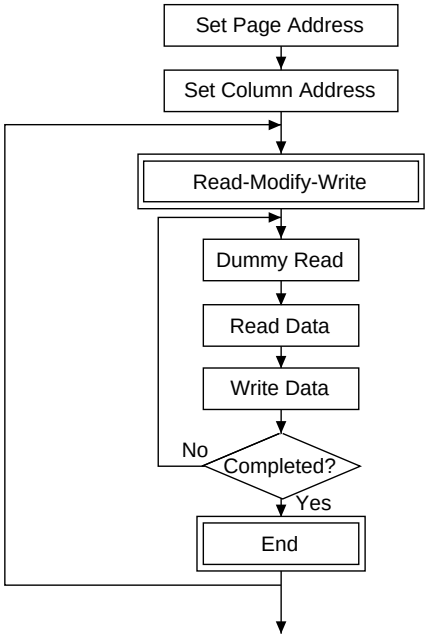
Model	Bias ratio of LCD power supply
SED1530	1/5 bias or 1/6 bias
SED1531 SED1532	1/6 bias or 1/8 bias
SED1533 SED1534	1/5 bias

(12) Read-Modify-Write
A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

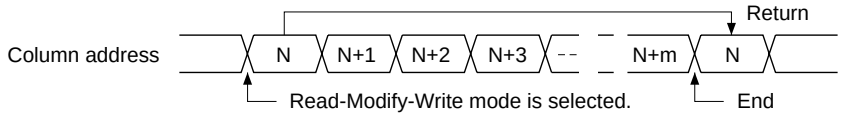
• Cursor display sequence



(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset siganl to the $\overline{RES}$ pin can initialize the supplies.

(15) Output Status Select Register

Applicable to the SED1530 and SED1532. When D is high or low, the scan direction of the COM output pin is selectable. Refer to Output Status Selector Circuit in Functional Description for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pin
* : Invalid bit

(16) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

(17) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V5 LCD drive voltage that is output by voltage regulator of on-board power supply.
This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator section of FUNCTIONAL DESCRIPTION for details.

A0	RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

D4	D3	D2	D1	D0	| V5 |
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(18) Static Indicator

This command turns on or off static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes are dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

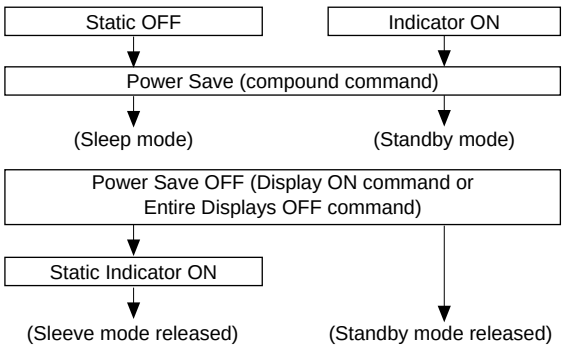
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D 0: Static indicator OFF
1: Static indicator ON

(19) Power Save (Compound Command)

When all displays are turned on during indicator off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.

Release the Sleep mode using the both Power Save OFF command (Indicator ON command or All Indicator Displays OFF command) and Static Indictor ON command.
Release the Standby mode using the Power Save OFF command (Indicator ON command or All Indicator Displays OFF command).



Sleep mode
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the SED1530 series is in the standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VDD level, prior to or concurrently with causing the 1530 series to go to the sleep mode or standby mode.

When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VDD level, prior to or concurrently with causing the SED1530 series to go to the sleep mode or standby mode.

When the common driver SED1635 or SED1651 is combined with the SED1531 in the configuration, the $\overline{DOF}$ pin of the SED1531 must be connected to the $\overline{DOFF}$ pin of the SED1635 or SED1651.

(20) Test Command
This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued erroneously, set the -$\overline{RES}$ input to low or issue the Reset command to release the test mode.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* : Invalid bit

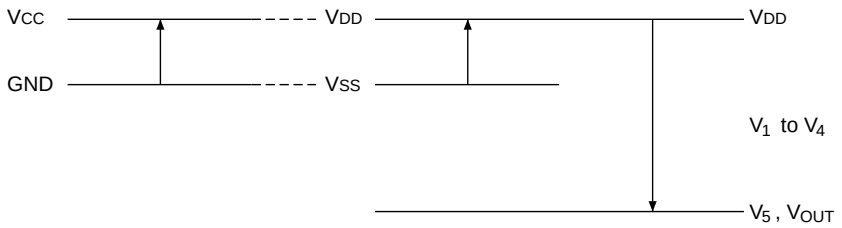
Cautions: The SED1530 Series holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.
The test command can be inserted in an unexpected place. Therefore, it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	0	1	Start display address						Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register.
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1).
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Output Status Register	0	1	0	1	1	0	0	0 1	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode.
(17) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V5 output voltage to Electronic Control register.
(18) Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0: OFF 1: ON
(19) Power Save	–	–	–	–	–	–	–	–	–	–	–	Compound command of display OFF and entire display ON
(20) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(21) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple boosting		–0.3 to +6.0	
	Quadruple boosting		–0.3 to +4.5	
Supply voltage range (1) (V_{DD} Level)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage range (2) (V_{DD} Level)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	TCP	T_{STR}	–55 to +100	°C
	Bear chip		–55 to +125	



Notes: 1. V_1 to V_5, V_{OUT}, voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0 V, V_{DD} = 5 V ±10%, Ta = –40 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommended Operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
	Operational				2.4	–	6.0		
Operating voltage (2)	Operational	V_5	V_{DD} level (V_{DD} = 0 V)		–16.0	–	–4.5	V	V_5 *2
	Operational	V_1, V_2	V_{DD} level (V_{DD} = 0 V)		$0.4 \times V_5$	–	V_{DD}	V	V_1, V_2
	Operational	V_3, V_4	V_{DD} level (V_{DD} = 0 V)		V_5	–	$0.6 \times V_5$	V	V_3, V_4
CMOS High-level input voltage		V_{IHC}			$0.7 \times V_{DD}$	–	V_{DD}	V	*3
			V_{DD} = 2.7 V		$0.8 \times V_{DD}$	–	V_{DD}		*3
CMOS Low-level input voltage		V_{ILC}			V_{SS}	–	$0.3 \times V_{DD}$	V	*3
			V_{DD} = 2.7 V		V_{SS}	–	$0.2 \times V_{DD}$		*3
CMOS High-level output voltage		V_{OHC}	I_{OH} = –1 mA		$0.8 \times V_{DD}$	–	V_{DD}	V	*5
			V_{DD} = 2.7 V, I_{OH} = –0.5 mA		$0.8 \times V_{DD}$	–	V_{DD}		*5
CMOS Low-level output voltage		V_{OLC}	I_{OL} = 1 mA		V_{SS}	–	$0.2 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V, I_{OL} = 0.5 mA		V_{SS}	–	$0.2 \times V_{DD}$		*5
Schmitt High-level input voltage		V_{IHS}			$0.85 \times V_{DD}$	–	V_{DD}		*4
			V_{DD} = 2.7 V		$0.8 \times V_{DD}$	–	V_{DD}		*4
Schmitt Low-level input voltage		V_{ILS}			V_{SS}	–	$0.15 \times V_{DD}$		*4
			V_{DD} = 2.7 V		V_{SS}	–	$0.2 \times V_{DD}$		*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	–	1.0	µA	*6
Output leakage current		I_{LO}			–3.0	–	3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V_5 = –14.0 V	–	2.0	3.0	KΩ	SEG n COM n *8
			V_{DD} level	V_5 = –8.0 V	–	3.0	4.5		
Static current consumption		I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		–	0.01	5.0	µA	V_{SS}
		I_{5Q}	V_5 = –18.0 V (V_{DD} level)		–	0.01	15.0	µA	V_5
Input pin capacity		C_{IN}	Ta = 25°C, f = 1 MHz		–	5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	Ta = 25°C	V_{DD} = 5 V	18	22	26	kHz	*9
				V_{DD} = 2.7 V	18	22	26		

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Built-in power circuit	Input voltage	V_{DD}	Triple boosting	2.4	–	6.0	V	*10
			Quadruple boosting	2.4	–	4.5		
	Booster output voltage	V_{OUT}	Triple voltage conversion (V_{DD} level)	–18.0	–	–	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}	(V_{DD} level)	–18.0	–	–6.0	V	V_{OUT}
	Voltage follower operation voltage	V5	(V_{DD} level)	–18.0	–	–6.0	V	*11
				–16.0	–	–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C (V_{DD} level)	–2.75	–2.55	–2.35	V	

For the mark *, refer to P. 1–25

Dynamic current consumption (1) when the built-in power supply is OFF

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530/ SED1535	I_{DD} (1)	V_{DD} = 5.0V, V_5 – V_{DD} = –8.0 V	—	24	40	µA	*12
		V_{DD} = 3.0V, V_5 – V_{DD} = –8.0 V	—	22	35		
SED1531		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V	—	40	65		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V	—	36	60		
SED1532		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V	—	39	65		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V	—	32	55		
SED1533		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V	—	20	35		
SED1534		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V	—	20	35		

Dynamic current consumption (2) when the built-in power supply is ON

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530/ SED1535	I_{DD} (1)	V_{DD} = 5.0V, V_5 – V_{DD} = –8.0 V, dual boosting	—	41	70	µA	*13
		V_{DD} = 3.0V, V_5 – V_{DD} = –8.0 V, triple boosting	—	48	80		
SED1531		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V, triple boosting	—	96	160		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V, quadruple boosting	—	118	190		
SED1532		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V, triple boosting	—	95	160		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V, quadruple boosting	—	114	190		
SED1533		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V, dual boosting	—	30	50		
SED1534		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V, dual boosting	—	32	55		

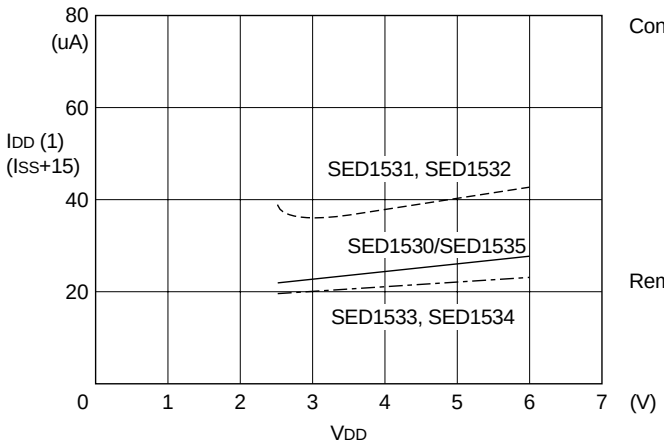
Current consumption during Power Save mode

V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
During sleep	I_{DDS1}	SED1530, SED1531, SED1532	—	0.01	1	µA	
During standby	I_{DDS2}	SED1530, SED1531, SED1532	—	10	20		

Typical current consumption characteristics (reference data)

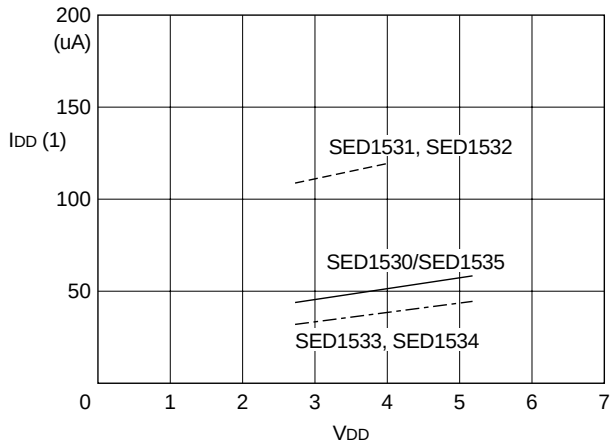
- Dynamic current consumption (1) when LCD external power mode lamp is ON



Condition: The built-in power supply is OFF and an external power supply is used.
SED1530/SED1535 V_5-V_{DD}=–8.0V
SED1531 V_5-V_{DD}=–11.0V
SED1532 V_5-V_{DD}=–11.0V
SED1533 V_5-V_{DD}=–6.0V
SED1534 V_5-V_{DD}=–6.0V
Ta=25°C

Remarks: ✻12

- Dynamic current consumption (2) when the LCD built-in power circuit lamp is ON



Condition: The built-in power circuit is ON.
SED1530/SED1535: V_5-V_{DD}=–8.0 V, triple boosting
SED1531: V_5-V_{DD}=–11.0 V, quadruple boosting
SED1532: V_5-V_{DD}=–11.0 V, quadruple boosting
SED1533: V_5-V_{DD}=–5.0 V, dual boosting
SED1534: V_5-V_{DD}=–5.0 V, dual boosting
Ta=25°C

Remarks: ✻13

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the microprocessor.
*2 V_{DD} and V_5 operating voltage range. (Refer to Fig. 10.)
The operating voltage range applies if an external power supply is used.
*3 A0, D0 - D5, D6, D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$ pins
*4 CL, SCL (D6) and $\overline{RES}$ pins
*5 D0 - D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins
*6 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, $\overline{RES}$, C86 and P/S pins
*7 Applies when the D0 - D7, FR, CL, DYO and $\overline{DOF}$ pins are in high impedance,
*8 Resistance value when 0.1 V is applied between the output pin SEGn or COMn and each power supply pin (V1, V2, V3, V4). This is specified in the operating voltage (2) range.
R ON = 0.1 V/ΔI (ΔI: Current flowing when 0.1 V is applied in the ON status.)
*9 For the relationship between oscillation frequency and frame frequency, refer to Fig. 9.
*10 For triple or quadruple boosting using the on-chip power useing the primary-side power supply V_{DD} must be used within the input voltage range.
*11 The voltage regulator adjusts V_5 within the voltage follower operating voltage range.
*12, *13 Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc. This is current consumption under the conditions of display data = checker, display ON, SED1530 = 1/33 duty (1/6 Bias), and SED1531 and SED1532 = 1/65 duty. (1/8 Bias)
*12 Applies to the case where the on-chip oscillator circuit is used and no access is made from the microprocessor.
*13 Applies to the case where the on-chip oscillator circuit and the on-chip power circuit are used and no access is made from the microprocessor.
The current flowing through voltage regulation resistors (R1, R2 and R3) is not included.
The current consumption, when the on-chip voltage booster is used, is for the power supply V_{DD}.

- Relationship between oscillation frequency and frame frequency

The relationship between oscillation frequency f_{OSC} and LCD frame frequency, f_F can be obtained by the following expression.

	Duty	f_{CL}	f_F
SED1530	1/33	$f_{OSC}/8$	$f_{OSC}/(8*33)$
SED1531 SED1532	1/65	$f_{OSC}/4$	$f_{OSC}/(4*65)$
SED1533	1/17	$f_{OSC}/8$	$f_{OSC}/(8*17)$
SED1534	1/9	$f_{OSC}/8$	$f_{OSC}/(8*9)$
SED1535	1/35	$f_{OSC}/8$	$f_{OSC}/(8*35)$

(f_F does not indicate the FR signal cycle but the AC cycle.)

Fig. 9

Relationship between clock (f_{CL}) and frame frequency f_F

- V_{SS} and V_5 operating voltage range

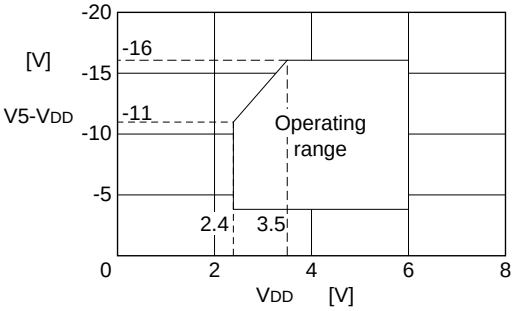
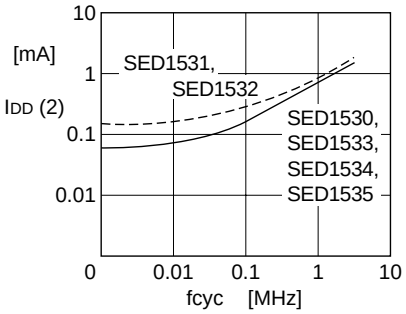


Fig 10

- Current consumption at access IDD (2) - Microprocessor access cycle



This indicates current consumption when data is always written on the checker pattern at fcyc. When no access is made, only IDD (1) occurs.

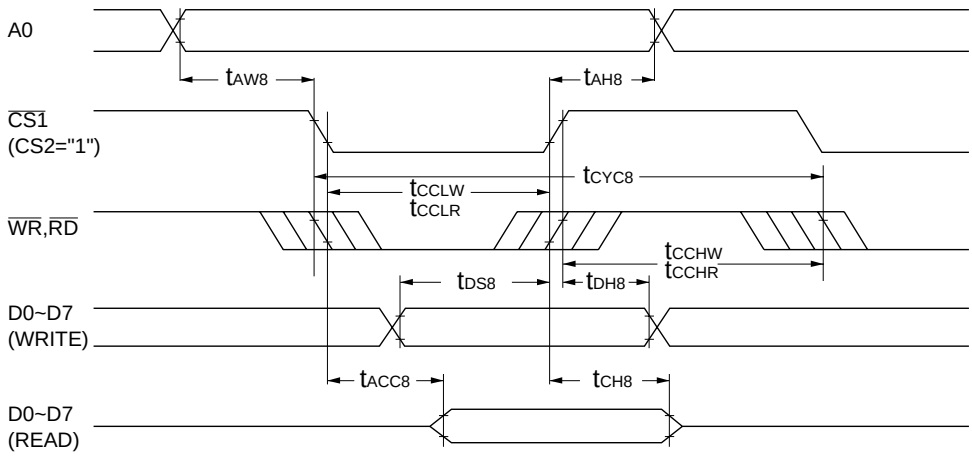
Condition: SED1530/SED1535 V_5-V_{DD}=-8.0V, triple boosting
SED1531 V_5-V_{DD}=-11.0V, quadruple boosting
SED1532 V_5-V_{DD}=-11.0V, quadruple boosting
SED1533 V_5-V_{DD}=-6.0V, dual boosting
SED1534 V_5-V_{DD}=-6.0V, dual boosting
Ta = 25°C

Fig. 11

AC Characteristics

(1) System buses

Read/write characteristics I (8080-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		10	–	ns
Address setup time		t_{AW8}		10	–	ns
System cycle time		t_{CYC8}		166	–	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		30	–	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		70	–	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		100	–	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		70	–	ns
Data setup time		t_{DS8}		20	–	ns
Data hold time		t_{DH8}		10	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L=100pF	–	70	ns
Output disable time		t_{CH8}		10	50	ns

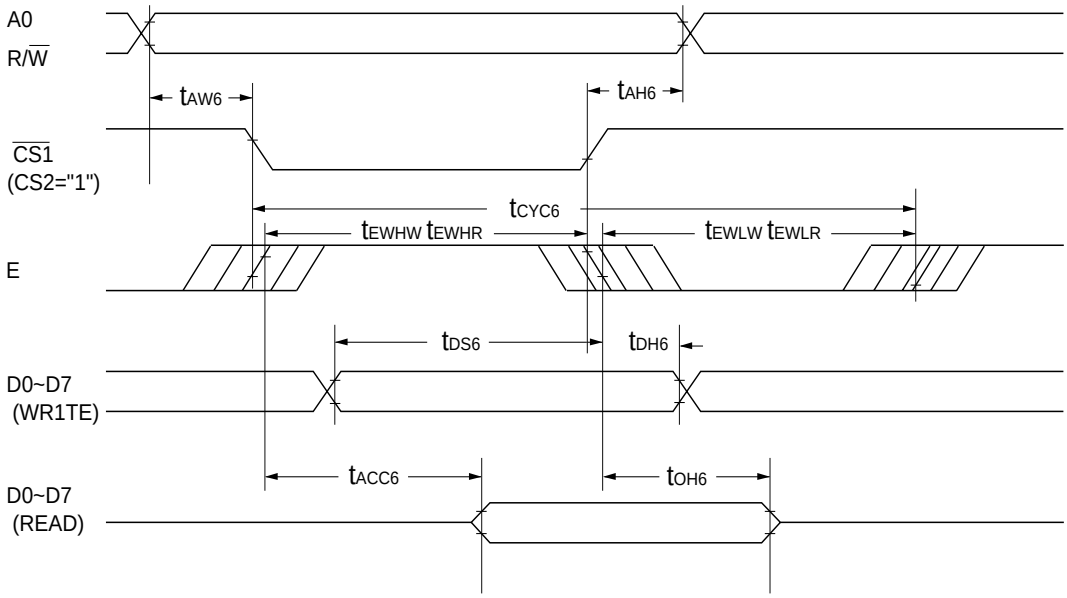
V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		19	–	ns
Address setup time		t_{AW8}		15	–	ns
System cycle time		t_{CYC8}		450	–	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		60	–	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		140	–	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		200	–	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		140	–	ns
Data setup time		t_{DS8}		40	–	ns
Data hold time		t_{DH8}		15	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L=100pF	–	140	ns
Output disable time		t_{CH8}		10	100	ns

Notes: 1. The input signal rise/fall time (t_r, t_f) is specified at 15 ns or less.
When system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC8} - t_{CCLW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which $\overline{CS1}$ is "0" (CS2 = "1") and $\overline{WR}$ and $\overline{RD}$ are "0".

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

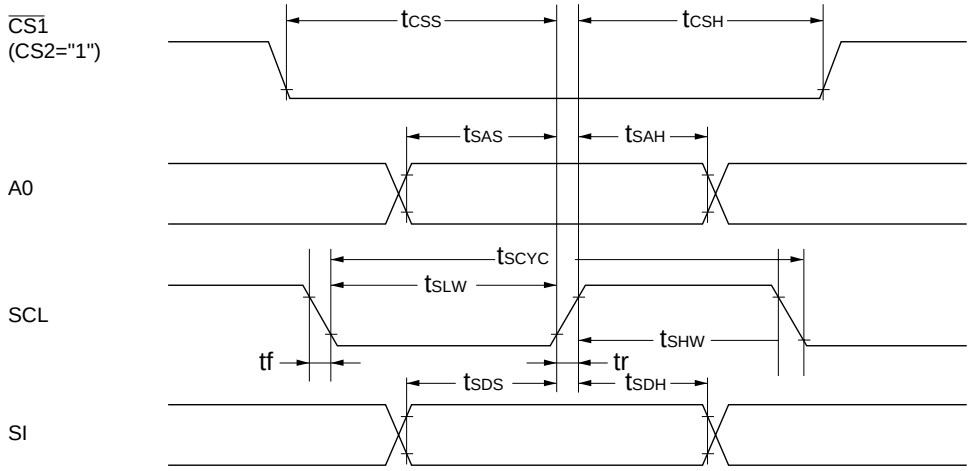
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		166	–	ns
Address setup time Address hold time		A0 W/$\overline{R}$	t_{AW6} t_{AH6}		10 10	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		20 10	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L=100pF	10 –	50 70	ns ns
Enable low pulse width	READ WRITE	E	t_{EWHR} t_{EWHW}		70 30	– –	ns ns
Enable high pulse width	READ WRITE	E	t_{EWLR} t_{EWLW}		70 100	– –	ns ns

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		450	–	ns
Address setup time Address hold time		A0 R/$\overline{W}$	t_{AW6} t_{AH6}		15 19	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L=100pF	10 –	100 140	ns ns
Enable low pulse width	READ WRITE	E	t_{EWHR} t_{EWHW}		140 60	– –	ns ns
Enable high pulse width	READ WRITE	E	t_{EWLR} t_{EWLW}		140 200	– –	ns ns

Notes: 1. The input rise/fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $tr + tf \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which CS1 is "0" (CS2 = "1") and E is "1".

(3) Serial interface



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

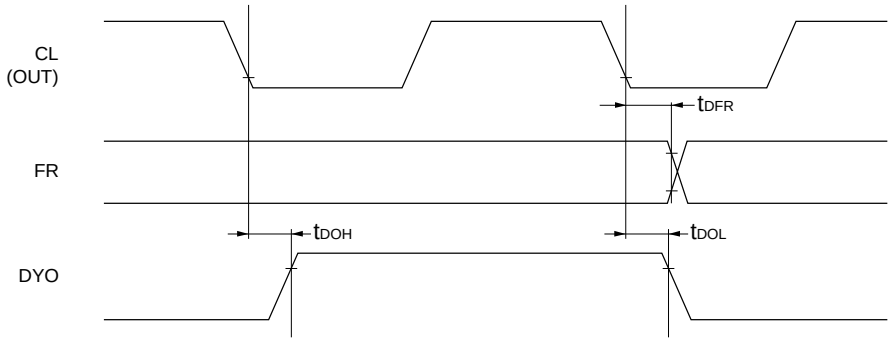
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250	–	ns
Serial clock H pulse width		t_{SHW}		100	–	ns
Serial clock L pulse width		t_{SLW}		75	–	ns
Address setup time	A0	t_{SAS}		50	–	ns
Address hold time		t_{SAH}		200	–	ns
Data setup time	SI	t_{SDS}		50	–	ns
Data hold time		t_{SDH}		50	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		30	–	ns
		t_{CSH}		100	–	

V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500	–	ns
Serial clock H pulse width		t_{SHW}		200	–	ns
Serial clock L pulse width		t_{SLW}		150	–	ns
Address setup time	A0	t_{SAS}		100	–	ns
Address hold time		t_{SAH}		400	–	ns
Data setup time	SI	t_{SDS}		100	–	ns
Data hold time		t_{SDH}		100	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		60	–	ns
		t_{CSH}		200	–	

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) Display control timing



Output timing V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

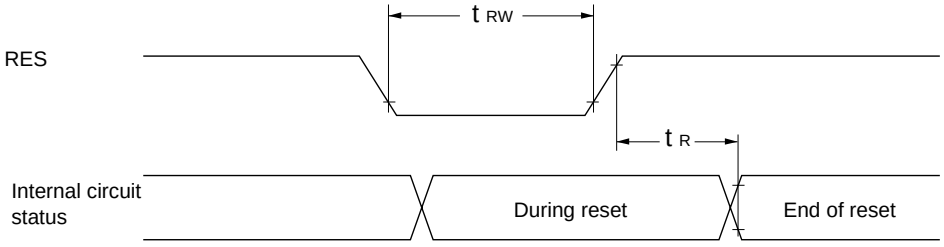
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	C_L = 50 pF	–	10	40	ns
DYO "H" delay time	DYO	t_{DOH}		–	40	100	ns
DYO "L" delay time		t_{DOL}		–	40	100	ns

Output timing V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	C_L = 50 pF	–	15	80	ns
DYO "H" delay time	DYO	t_{DOH}		–	70	200	ns
DYO "L" delay time		t_{DOL}		–	70	200	ns

Notes: 1. The otput timing is valid in master mode.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

(5) Reset timing



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		0.5	–	–	µs
Reset low pulse width	$\overline{RES}$	t_{RW}		0.5	–	–	µs

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

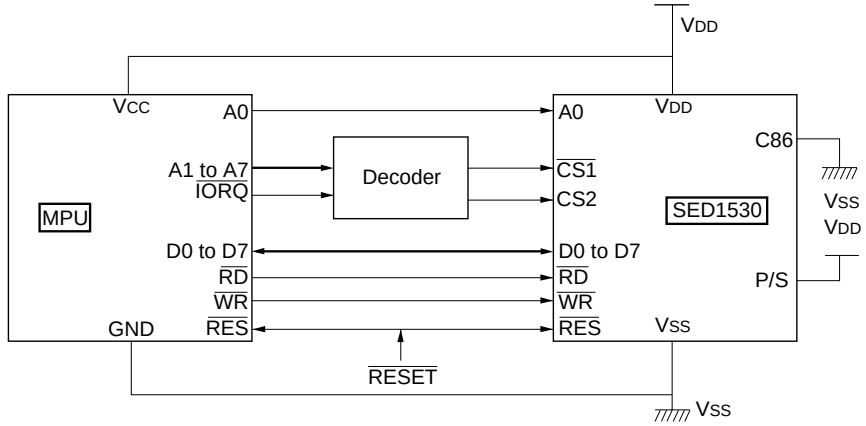
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0	–	–	µs
Reset low pulse width	$\overline{RES}$	t_{RW}		1.0	–	–	µs

Note: The reset timing is specified on the basis of 20% and 80% of V_{DD}.

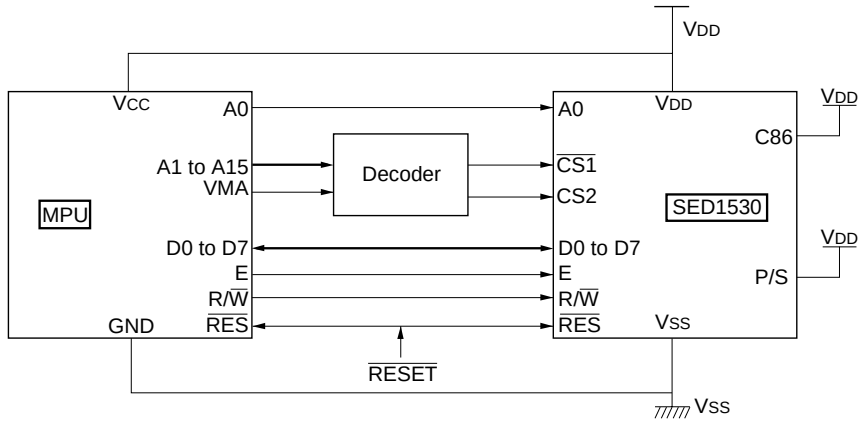
MICROPROCESSOR INTERFACE (Reference example)

The SED1530 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them. When multiple chips are used in the SED1530 series they can be connected to the microprocessor and one of them can be selected by Chip Select.

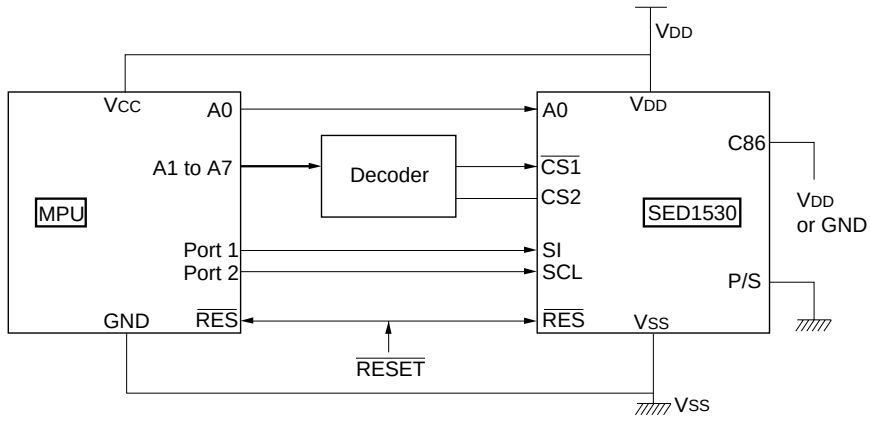
8080-series microprocessors



6800-series microprocessors



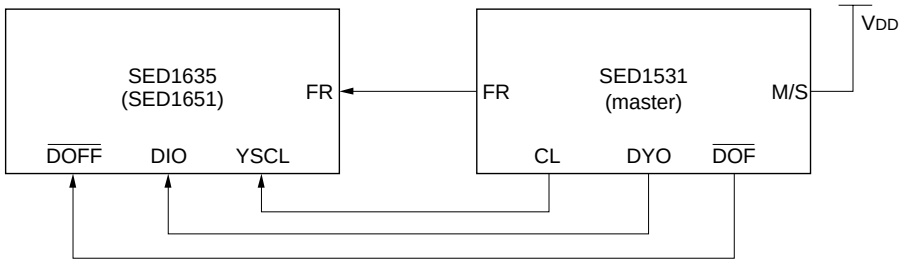
Serial interface



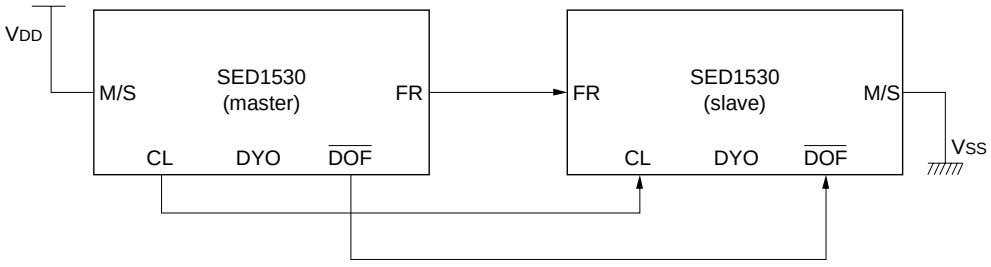
CONNECTION BETWEEN LCD Drivers

The LCD panel display area can easily be expanded by use of multiple SED1530 series chips. The SED1530 series can also be connected to the common driver (SED1635).

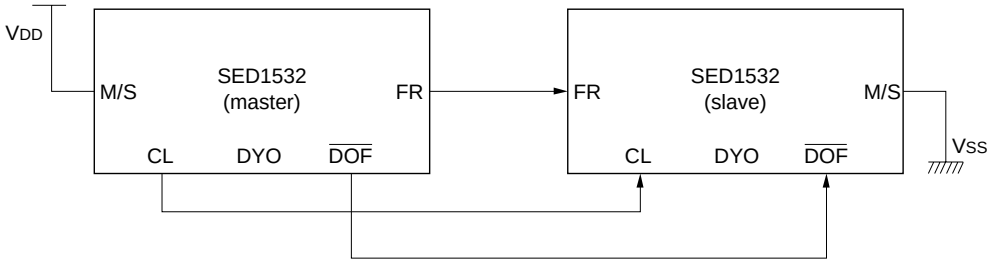
SED1531 to SED1635 (SED1651)

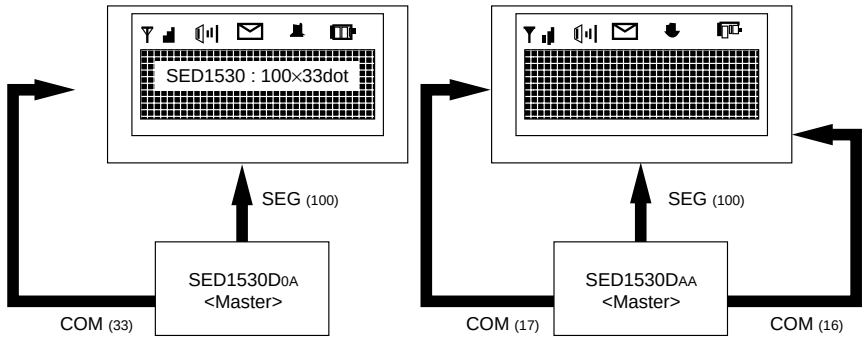


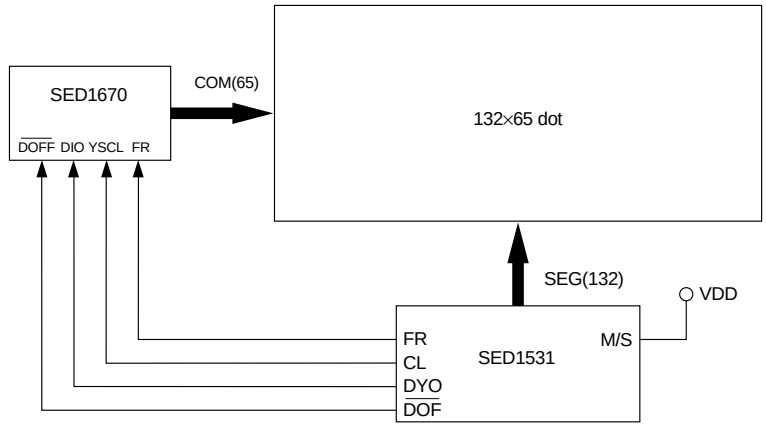
SED1530 to SED1531

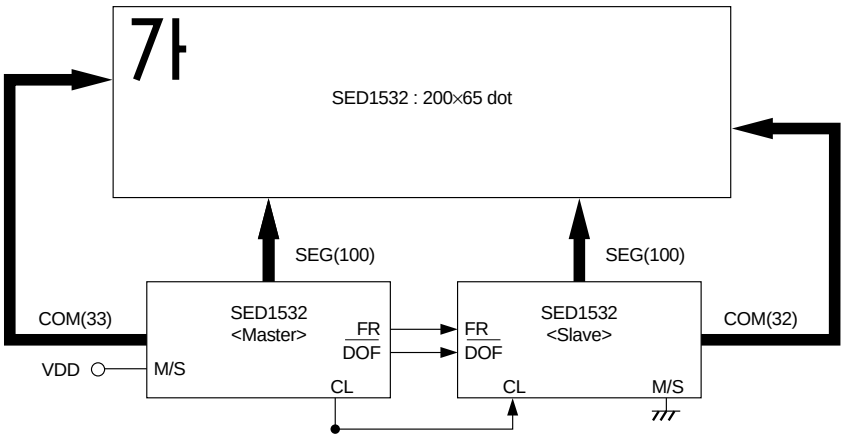


SED1532 to SED1532



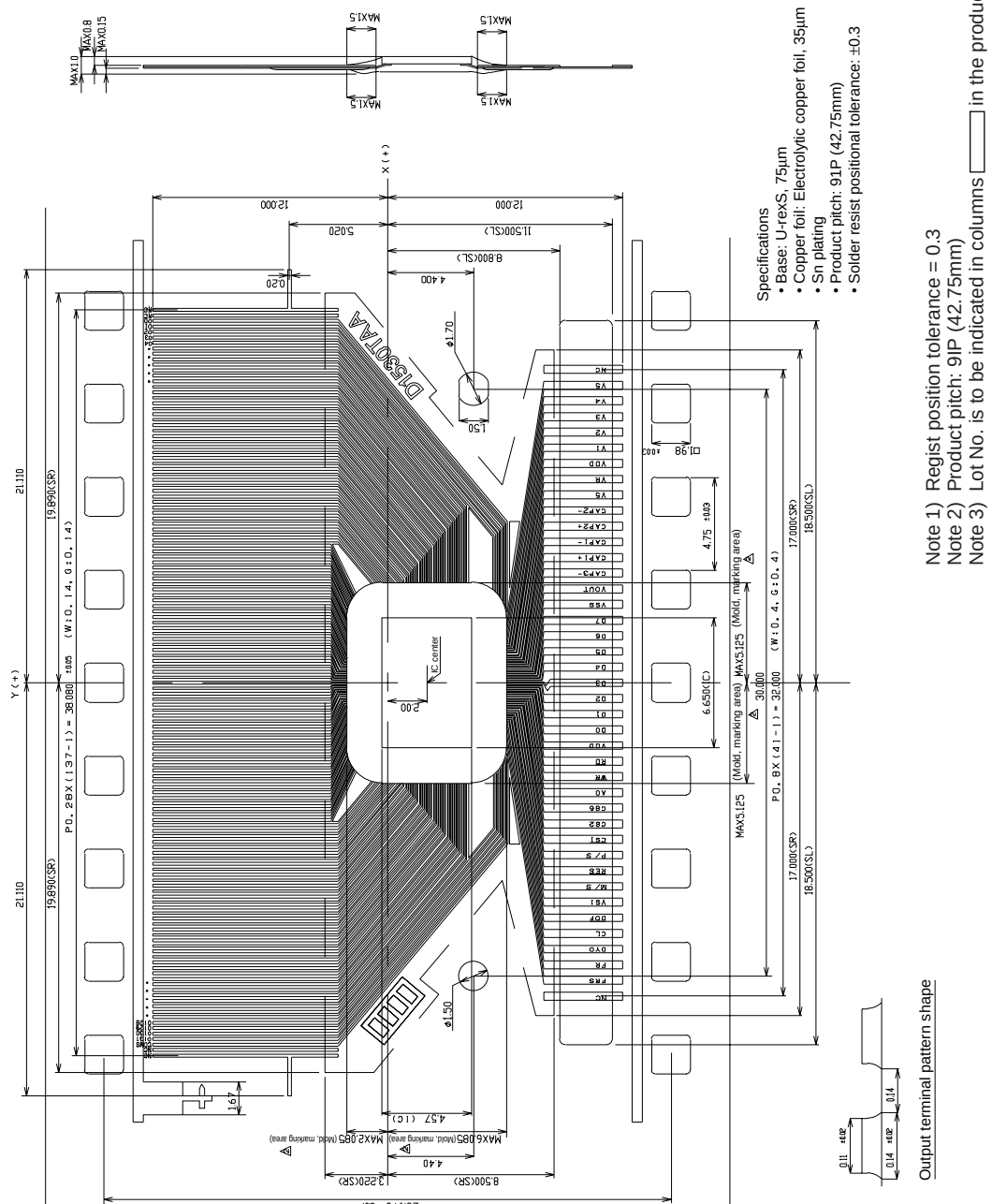

SED1530 : 100×33dot
SEG (100)
SED1530D0A
<Master>
COM (33)
SEG (100)
SED1530DAA
<Master>
COM (17)
COM (16)


SED1670
DOFF DIO YSCL FR
COM(65)
132×65 dot
SEG(132)
VDD
FR
CL
DYO
DOF
SED1531
M/S


SED1532 : 200×65 dot
SEG(100)
SEG(100)
COM(33)
VDD
M/S
SED1532
<Master>
FR
DOF
CL
FR
DOF
SED1532
<Slave>
CL
M/S
COM(32)

Dimensional outline drawing of the flexible substrate

(an example) The dimensions are subject to change without prior notice.



6. SED1540 Series

Contents

OVERVIEW

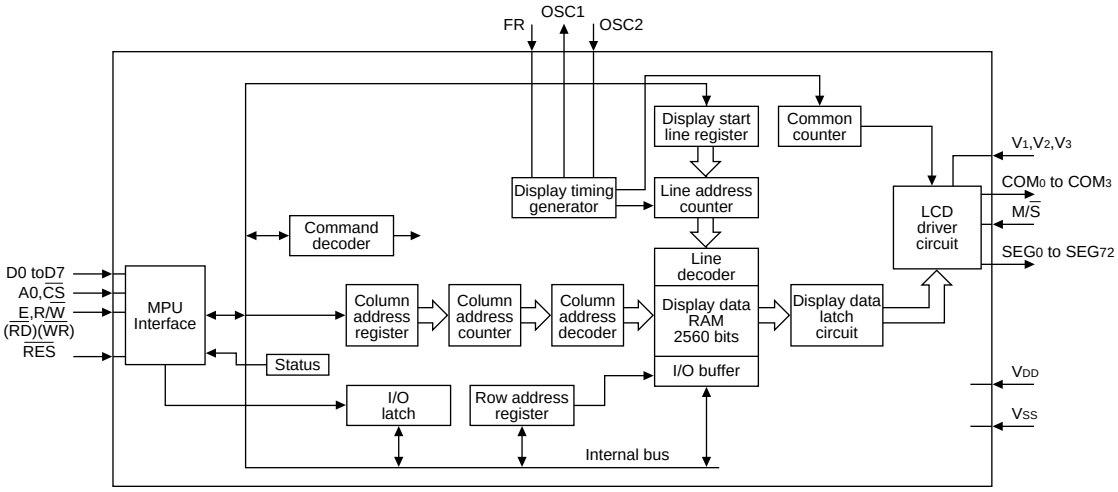
The SED1540 is a segment LCD driver intended for use with medium size LCD panels.
The driver generates LCD drive signals from data supplied by an MPU over a high speed, 8-bit bus, 4-bit bus and stored in its internal display RAM.
The SED1540 incorporates innovative circuit design strategies, to achieve very low power consumption at a wide range of operating voltages, and a rich command set. These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

FEATURES

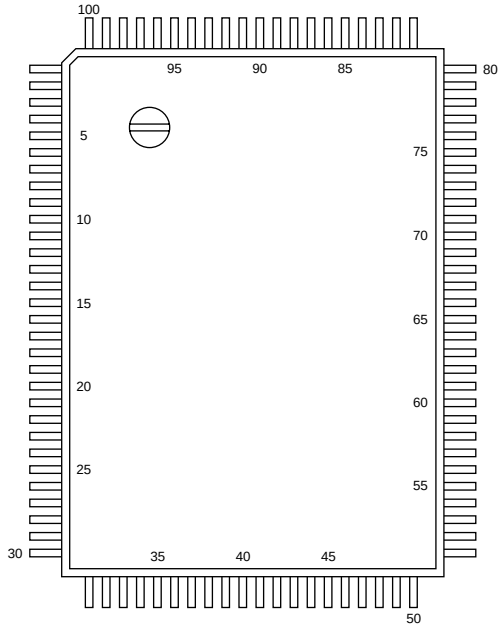
- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Rich command set
- 73 segment drive outputs
- 4 common drive outputs
- Selectable 1/3 or 1/4 duty cycle
- Low power consumption -70 μW maximum
- Wide range of supply voltages, V_{SS} –2.4 V to –7.0 V
- Implemented in CMOS
- Choice of packages
  —SED1540F0A : 100-pin QFP
  —SED1540D0A : Aluminum pad chip
  —SED1540D0B : Gold bump chip

Clock Source	f_{CL}	Frame Frequency
External clock	4 kHz	85/64 Hz
Internal osc.	18 kHz	375/281 Hz

BLOCK DIAGRAM



PACKAGE OUTLINE



PIN OUT

For chip pad locations see section 4.3, Mechanical Specifications.

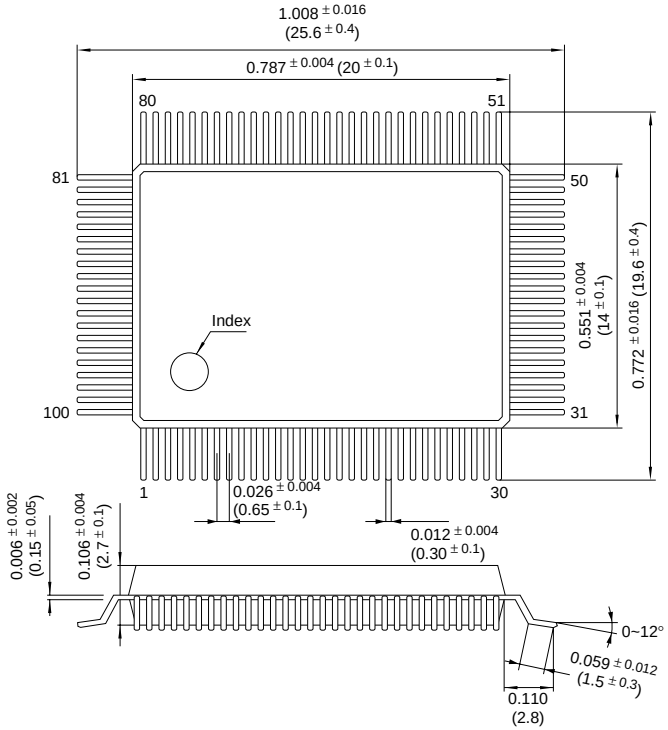
Number	Name	Number	Name	Number	Name	Number	Name
1	SEG71	26	SEG46	51	SEG21	76	E ($\overline{RD}$)
2	SEG70	27	SEG45	52	SEG20	77	R/$\overline{W}$ ($\overline{WR}$)
3	SEG69	28	SEG44	53	SEG19	78	V_{SS}
4	SEG68	29	SEG43	54	SEG18	79	DB0
5	SEG67	30	SEG42	55	SEG17	80	DB1
6	SEG66	31	SEG41	56	SEG16	81	DB2
7	SEG65	32	SEG40	57	SEG15	82	DB3
8	SEG64	33	SEG39	58	SEG14	83	DB4
9	SEG63	34	SEG38	59	SEG13	84	DB5
10	SEG62	35	SEG37	60	SEG12	85	DB6
11	SEG61	36	SEG36	61	SEG11	86	DB7
12	SEG60	37	SEG35	62	SEG10	87	V_{DD}
13	SEG59	38	SEG34	63	SEG9	88	$\overline{RES}$
14	SEG58	39	SEG33	64	SEG8	89	FR
15	SEG57	40	SEG32	65	SEG7	90	V3
16	SEG56	41	SEG31	66	SEG6	91	$\overline{CS}$
17	SEG55	42	SEG30	67	SEG5	92	NC
18	SEG54	43	SEG29	68	SEG4	93	M/$\overline{S}$
19	SEG53	44	SEG28	69	SEG3	94	V2
20	SEG52	45	SEG27	70	SEG2	95	V1
21	SEG51	46	SEG26	71	SEG1	96	COM0
22	SEG50	47	SEG25	72	SEG0	97	COM1
23	SEG49	48	SEG24	73	A0	98	COM2
24	SEG48	49	SEG23	74	OSC1	99	COM3
25	SEG47	50	SEG22	75	OSC2	100	SEG72

Duty	Pin	
	98	99
1/4	COM2	COM3
1/3	NC	COM2

Mechanical Specifications

SED1540F0A Flat Pack

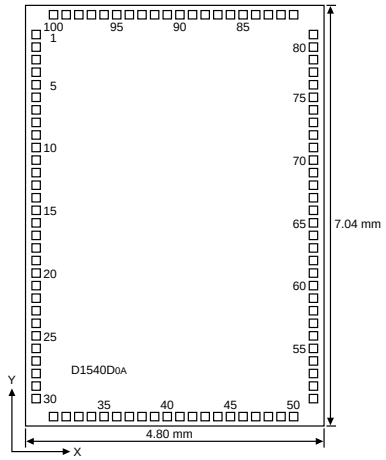
Dimensions: inches (mm)



SED1540D Chip Dimensions

Aluminum pad
- Die size: 4.80 mm × 7.04 mm × 0.525 mm
- Pad size: 100 × 100 μm

Gold bump
- Minimum bump pitch: 199 μm
- Bump height: 20 μm +10/–5 μm
- Bump size: 132 × 111 μm ±20 μm



Pad		X	Y
Number	Name		
1	SEG71	159	6507
2	SEG70	159	6308
3	SEG69	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
Number	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
Number	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	OSC1	4641	5247
75	OSC2	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/$\overline{W}$ ($\overline{WR}$)	4641	5846
78	VSS	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V3	2499	6884
91	$\overline{CS}$	2300	6884
92	NC	2100	6884
93	M/$\overline{S}$	1901	6884
94	V2	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	SEG72	504	6884
—	—	—	—
—	—	—	—

PIN DESCRIPTION

System Bus Interface

D0 – D7:
8-bit, tri-state, bi-directional I/O bus
A0:
Data/command select input
- A0=0: Display control data on D0–D7
- A0=1: Display data D0–D7

$\overline{RES}$:
Reset and interface configuration input. The driver is reset on any edge of $\overline{RES}$.
After reset the SED1540F is in the following state
- Display off
- Display startline register: Line 1
- Static drive off
- Column address counter: 0
- Page address register: 0
- Duty cycle: 1/4
- ADC: Forward (ADC command D0 = "0". ADC status flag "1")
- Read-modify-write OFF

In addition the MPU interface is configured by the level of $\overline{RES}$ as given in the table below

$\overline{RES}$	Interface	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
High	68 MPU	↑	↑	↑	↑	↑
Low	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

$\overline{CS}$: Active low chip select input
E or $\overline{RD}$:
- $\overline{RES}$ = 1: Enable clock input
- $\overline{RES}$ = 0: Active low read input. Taking both **$\overline{CS}$** and $\overline{RD}$ inputs low causes the driver to drive the MPU bus.

R/$\overline{W}$ or $\overline{WR}$:
- $\overline{RES}$ = 1: Read/write input
- $\overline{RES}$ = 0: Active low write strobe input. Data is latched into the driver on the falling edge of **$\overline{WR}$**.

LCD Interface

M/$\overline{S}$:
Master/slave driver select input.
- M/$\overline{S}$=1: Master
- M/$\overline{S}$=0: Slave
  The operation is different in master and slave mode as given in the table below.

M/S	COM output	OSC1	OSC2	FR
1	Valid	Input	Output	Output
0	Valid*	NC	Input	Input

Note: Using FR to synchronise master and slave drivers will produce in phase COM outputs.

FR:
LCD AC drive signal input/output.
- M/$\overline{S}$ = 1: Output
- M/$\overline{S}$ = 0: Input

SEG0 to SEG72:
LCD segment (column) driver outputs. The output levels of these pins are given in the table below.

FR	Data	
	1	0
1	V_{DD}	V_2
0	V_3	V_1

COM0 to COM13:
LCD common (row) driver outputs. The output levels of these pins depend on FR and the output of the common counter and are given in the table below.

FR	Counter	
	1	0
1	V_3	V_1
0	V_{DD}	V_2

Oscillator

OSC1:
- M/$\overline{S}$ = 1: Connect the internal oscillator feedback register, R_f, to this pin.
- M/$\overline{S}$ = 0: Leave open.

OSC2:
- M/$\overline{S}$ = 1: Connect the internal oscillator feedback resistor, R_f, to this pin.
- M/$\overline{S}$ = 0: Clock input.

Power Supply

V_{DD}:
+5 V input (0 V ground)
V_{SS}:
0 V ground (-5 V input)
V_1, V_2, V_3:
LCD driver power supply. These voltages must conform to the following relation
$V_{DD} \geq V1 \geq V2 \geq V3$

BLOCK DESCRIPTION

System Bus

Data transfer

The SED1540F driver uses the A0, E (or $\overline{RD}$) and R/W (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table below.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers, all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example, when the MPU executes a read cycle to access display RAM, the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

By using an MPU data bus I/O latch the display data RAM access timing is determined by the driver cycle time, t_{cyc}, not by the RAM access time. In general this strategy leads to faster data transfers between the driver and the MPU.

If the MPU access frequency is likely to exceed $1/t_{cyc}$, then the designer has the choice of inserting NOPs into the access loop or polling the driver, by reading the busy flag, to see if it will accept new data or instructions.

This means that a dummy read cycle has to be executed at the start of every series of reads.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

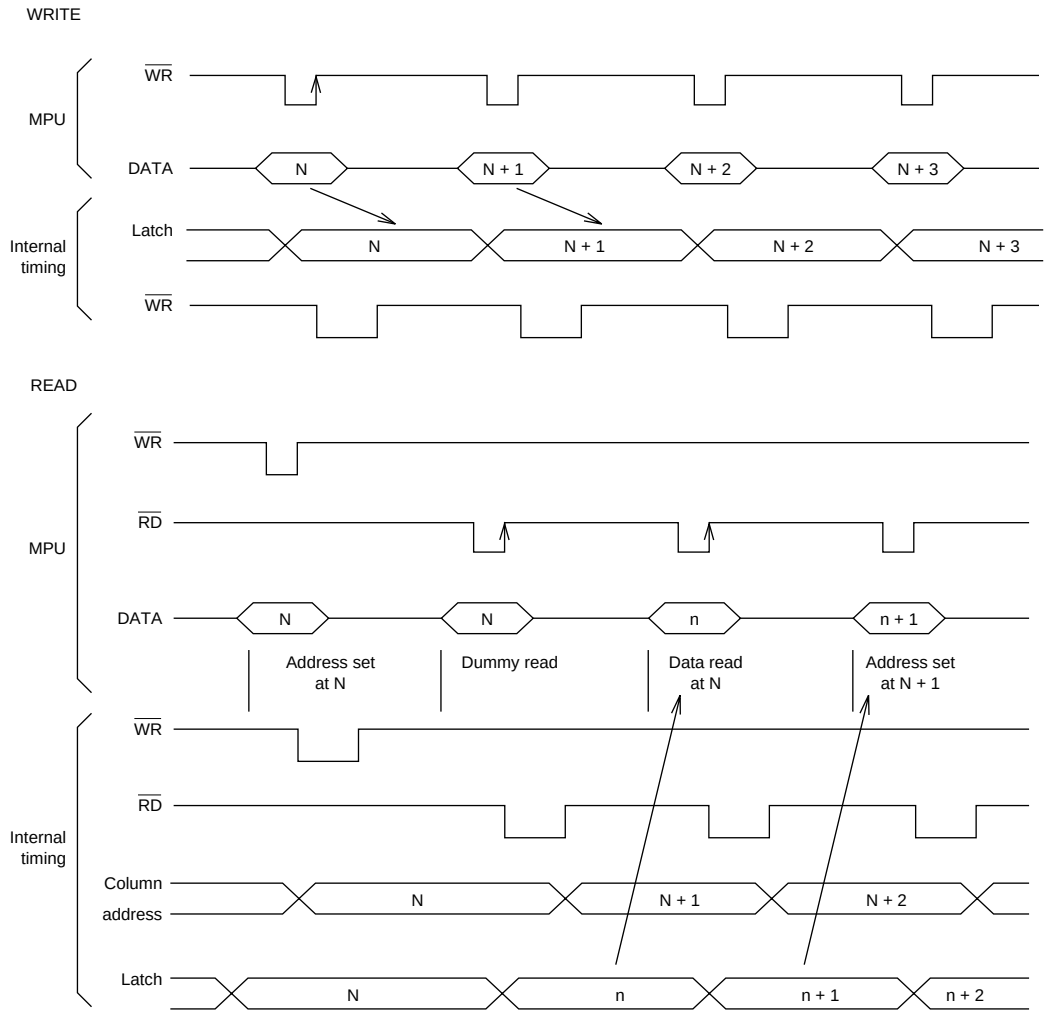


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the SED1540 is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the "Set Display Start Line" command (see section 3).
The contents of the display start-line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data in display data RAM being transferred to the segment driver ciruits.

Column Address Counter

The column address counter is a 7-bit presettable counter which supplies the column address (see figure 2) for MPU accesses to the display data RAM. The counter is incremented by one every time the driver receives a Read or Write Display Data Command.
Addresses above 50 H are invalid, and the counter will not increment past this valu. The contents of the column address conter are set with the Set Column Address command.

Page Register

The page register is a 2-bit register which supplies the page address (see figure 2) for MPU accesses to the display data RAM. The contents of the Page Register are set by the Set Page Register Command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in figure 2.

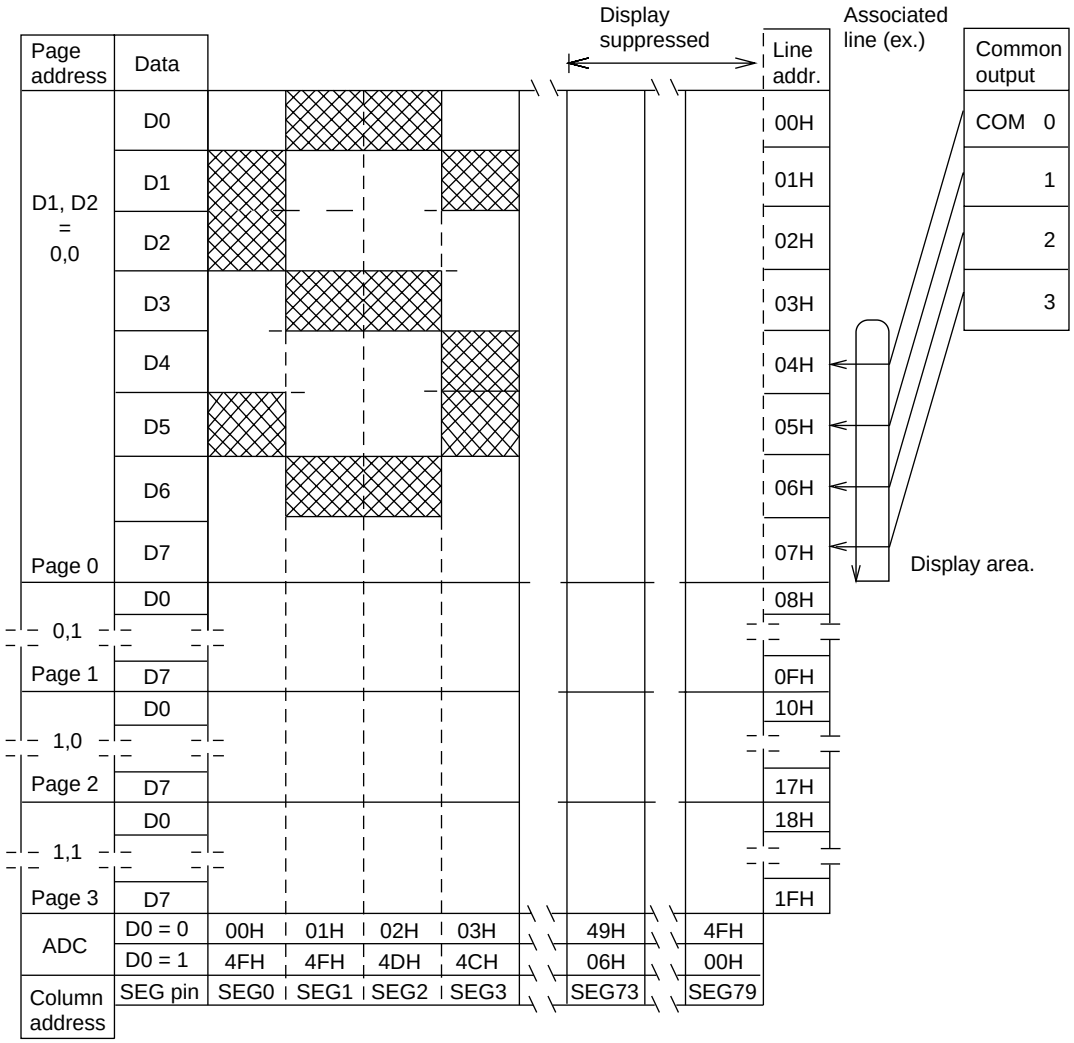


Figure 2 Display Data RAM Addressing

Common Timing Generator

This circuit generates common timing and frame (FR) signals from the basic clock CL. The "Select Duty Cycle" command selects a duty cycle of 1/3 or 1/4.

Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the "Display ON/OFF" and "Static Driver ON/OFF" commands.

LCD Drive Circuit

The LCD driver circuitry generates the 77 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

Display Timing Generator

This circuit generates the internal display timing signal using the basic clock OSC1, and the frame signal, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. OSC1 is used to lock the line counter to the system line scan rate.

Oscillation Circuit

The oscillator is a low power RC oscillator whose frequency of oscillation is determined by the value of the feedback resistor R_f or an externally generated 50% duty cycle clock input via OSC1. If a slave SED1540F is used, its OSC2 input is connected to the OSC2 output of the master driver.

Reset Circuit

This circuit senses both the edge and the level of the signal at the $\overline{RES}$ pin and uses this information to

- Initialization status

1. Display is off.
2. Display start line register is set to line 1.
3. Static drive is turned off.
4. Column address counter is set to address 0.
5. Page address register is set to page 0.
6. 1/4 duty is selected.
7. Forward ADC is selected (ADC command D0 is 0 and ADC status flag is 1).
8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.

When the Reset command is issued, initialization items 2, 4 and 5 above are executed.

As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.

If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.

COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF *
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (0 to 72)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: busy 0: Ready ADC 1: Forward 0: Reverse ON/OFF 1: Display off 0: Display on RESET 1: being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: Forward, 1: Reverse
Statis drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/4, 0: 1/3
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address register by 1 druing write only.
End	0	1	0	1	1	1	0	1	1	1	0	Read modify write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Sets the display start line register to line 1, and sets the column address counter and page address register to 0.

* The Power Save mode is selected if the static drive is turned ON when the display is OFF.

Command Description

Display ON/OFF

Table 3 is the command table. The SED1540 identifies a data bus using a combination of A0 and R/$\overline{W}$ ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.
D=1: Display ON
D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	0	A_4	A_3	A_2	A_1	A_0	C0H to DFH

A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	1	1	0	A_1	A_0	B8H to BBH

A_1	A_0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0	00H to 4FH

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

Read Status

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The BUSY bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-n → segment driver n.
- The ON/OFF bit indicates the current status of the display.
  ON/OFF=1: Display OFF
  RESET=0: Display ON
- The RESET bit indicates whether the driver is executing a reset or is in normal operating mode.
  RESET=1: Currently executing reset command
  RESET=0: Normal operation

Write Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM at a location specified by the contents of the column address and page address registers, and increments the column address register by one.

Read Display Data

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O buffer with display data from the display data RAM location specified by the contents of the column address and page address registers and increments the column address register.
After loading a new address into the column address register, one dummy read is required before valid data is obtained.

Select ADC

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

Selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICS and routing of traces during printed circuit board design. See figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A_0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

Sets the duty cycle of the LCD drive.
D=1: 1/4 duty cycle
D=0: 1/3 duty cycle

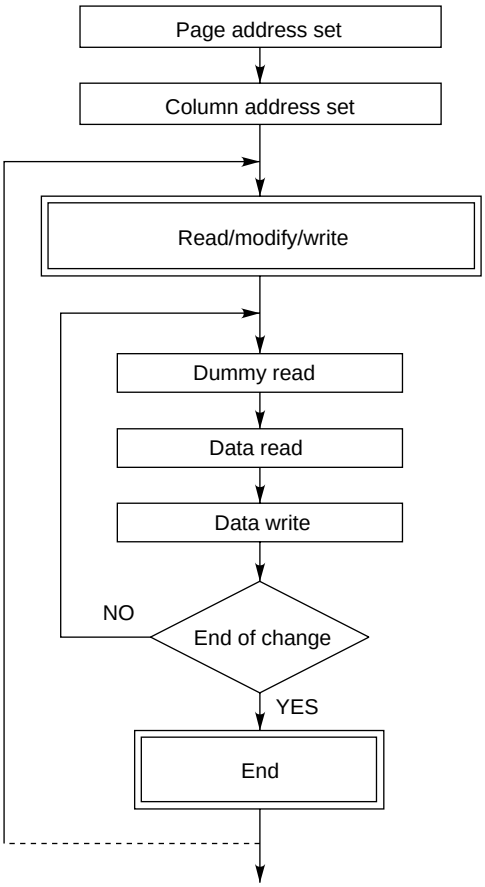
Read-Modify-Write

This command is used in combination with the End command. Once the Read-Modify-Write command is entered, the column address is incremented by 1 only by the display data write command but not incremented by the display data read command. This status is kept until the End command is entered.
When the End command is entered, the column address is returned to the column address when the Read-Modify-Write command is entered. This function can reduce the load of MPU when it repeatedly changes data of the specific display area such as a blinking cursor.

A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	0	0	E0H

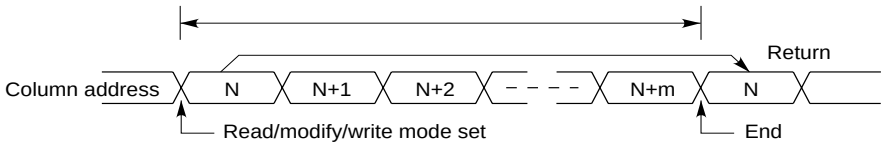
* Any command other than data read and write can be used during the Read-Modify-Write mode. However, the Column Address Set command cannot be used.

Sequence when the cursor is displayed



End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH



Cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the read-modify-write command.

Reset

This command resets the display start line register, column address counter, and page address register to their initial status. This command does not affect on the display data RAM. For details, see the Reset circuit of the functional block explanation.

The counter and registers are reset after the Reset command has been entered.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

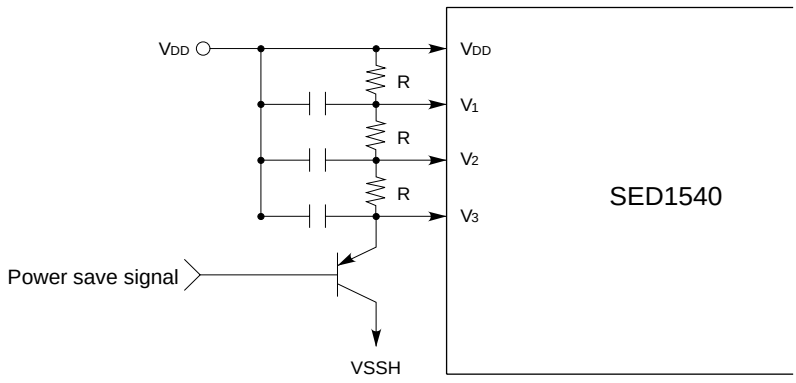
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (compound command)

The system enters the power save state by switching the static drive on in the display off state, reducing the consumed current almost to static current. The internal state in the power save state is as follows:

- The LCD drive is stopped, and the segment and common drivers output the VDD level.
- Oscillating external clock entry is inhibited, and OSC2 becomes floating.
- The display data and the operation mode are held.

The power save state can be canceled by switching the display on or static drive off.
When the LCD drive voltage level is supplied by an externally-equipped resistance dividing circuit, the current flowing through the resistor must be cut by means of the power save signal.



SPECIFICATIONS

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply voltage (1)		V_{SS}	–8.0 to +0.3	V
Supply voltage (2)		V_3	–15.0 to +0.3	V
Supply voltage (3)		V_1, V_2, V_3	V3 to +0.3	V
Input voltage		V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage		V_O	V_{SS}–0.3 to +0.3	V
Power dissipation		P_D	250	mW
Operating temperature		T_{opr}	–30 to +85	deg. C
Storage temperature	QFP	Tstg	–65 to +150	deg. C
	chip		–55 to +125	
Soldering temperature × time (at lead)		T_{sol}	260, 10	deg. C, s

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must always hold $V_{DD} \geq V_1 \geq V_2 \geq V_3$.
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced during the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

(Ta = –20 to 75 deg. C, V_{DD} = 0 V)

Parameter		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_3			–11.0	—	–3.5	V	V_3, See note 10.
	Allowable				–11.0	—	–2.7		
	Allowable	V_1			0.6×V_3	—	V_{DD}	V	V_1
	Allowable	V_2			V_3	—	0.4×V_3	V	V_2
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		See note 3
Low-level input voltage		V_{ILT}			V_{SS}	—	V_{SS}+0.8	V	See note 2
		V_{ILC}			V_{SS}	—	0.8×V_{SS}		See note 3
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	See note 4
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		See note 5
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		OSC2
Low-level output voltage		V_{OLT}	I_{OL} = 3.0 mA		—	—	V_{SS}+0.4	V	See note 4
		V_{OLC1}	I_{OL} = 2.0 mA		—	—	V_{SS}+0.4		See note 5
		V_{OLC2}	I_{OL} = 120 µA		—	—	0.8×V_{SS}		OSC2
Input leakage current		I_{LI}			–1.0	—	1.0	µA	See note 6.
Output leakage current		I_{LO}			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistor		R_{ON}	Ta = 25 deg. C	V_3 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 72, COM0 to 3. See note 11.
				V_3 = –3.5 V	—	10.0	50.0		
Static current dissipation		I_{DD0}	$\overline{CS}$ = CL = V_{DD}		—	0.05	1.0	µA	V_{DD}

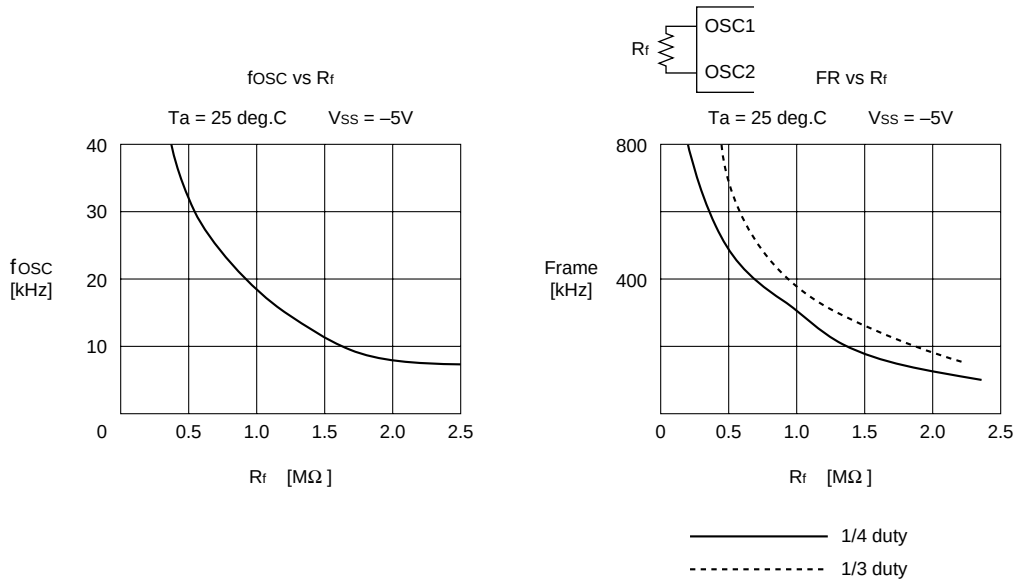
DC Characteristics (Cont'd)

(Ta = –20 to 75 deg. C, V_{DD} = 0 V)

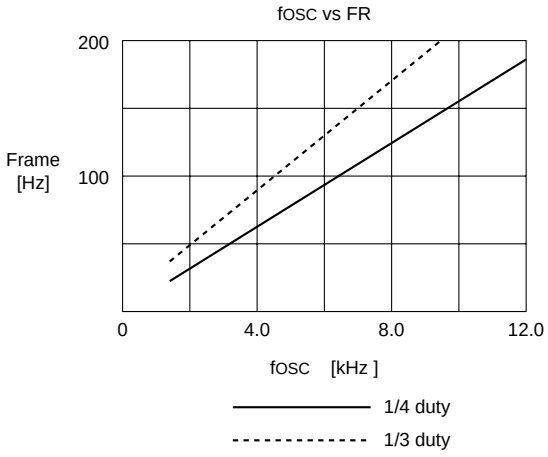
Parameters	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Dynamic current dissipation	I_{DD} (1)	During display	f_{OSC} = 4 kHz	—	1.5	4.0	µA	V_{DD}
		V_3 = –5.0 V	R_f = 1 MΩ	—	9.5	15.0		
	I_{DD} (2)	During assess fcyc = 200 kHz		—	300	500		See note 8.
Input pin capacitance	C_{IN}	Ta = 25 deg. C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	f_{OSC}	R_f = 1.0 MΩ ±2%, Vss=-5.0V		15	18	21	kHz	See note 9.
		R_f = 1.0 MΩ ±2%, Vss=–5.0V		11	16	21		
Reset time	t_R			1.0	—	1000	µS	$\overline{RES}$

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL and M/$\overline{S}$, $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write access at a frequency of t_{cyc}. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V_1, …, V_2) and output (COM, SEG) pins. All voltages within specified operating voltage range.

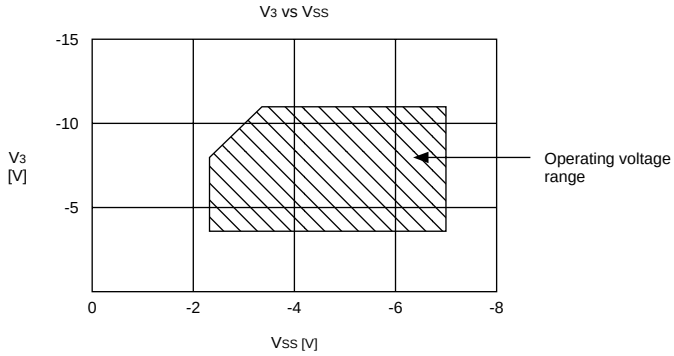
Relationship between f_{OSC}, f_{FR} and R_f



Relationship between f_{CL} and FR

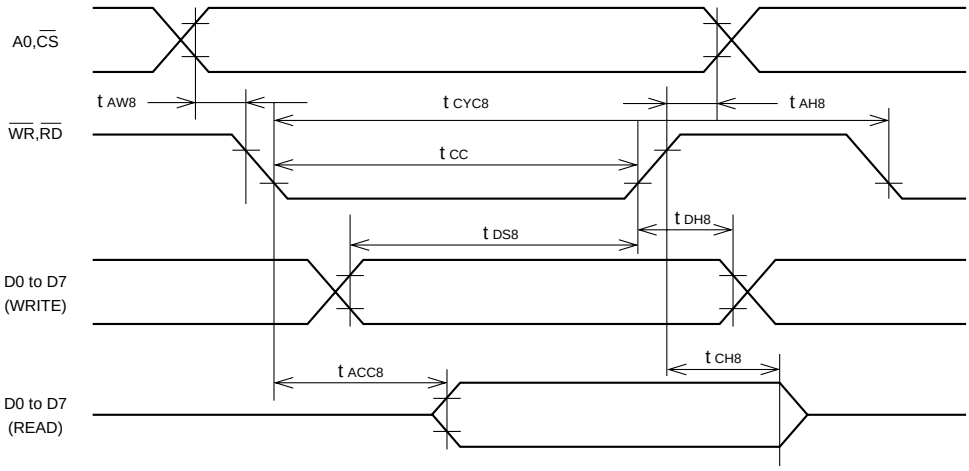


Operating bounds on Vss and V3



AC Characteristics

- MPU Bus Read/Write I (80-family MPU)

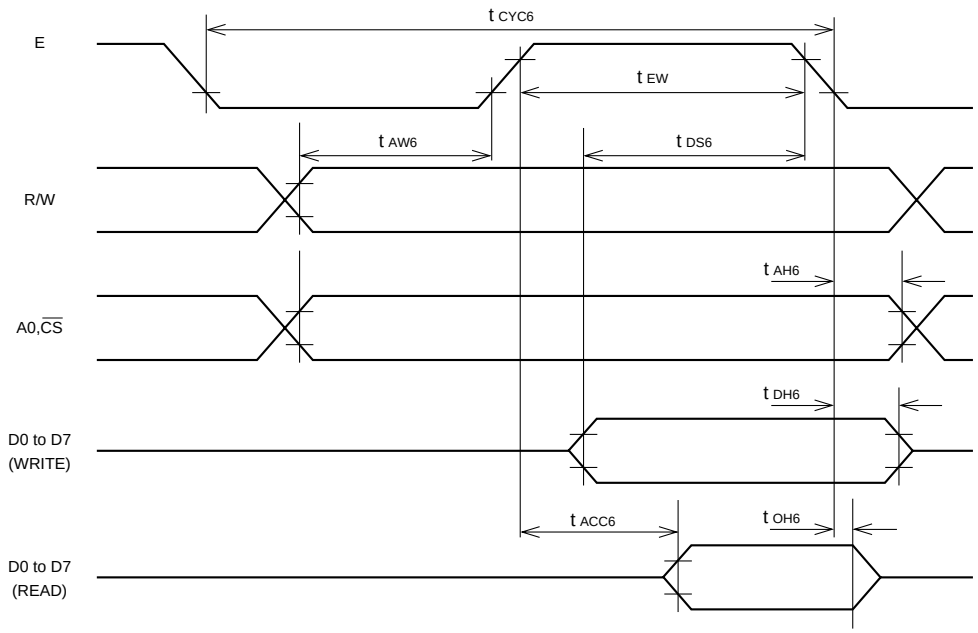


(Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	t_{AH8}		10	—	ns	A0, $\overline{CS}$
Address setup time	t_{AW8}		20	—	ns	
System cycle time	t_{CYC8}		1000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	t_{CC}		200	—	ns	
Data setup time	t_{DS8}		80	—	ns	D0 to D7
Data setup time	t_{DH8}		10	—	ns	
$\overline{RD}$ access time	t_{ACC8}	C_L = 100 pF	—	90	ns	
Output disable time	t_{CH8}		10	60	ns	

Notes: 1. All parameter values for a V_{SS} of –3.0 V are about 100% of their value for a V_{SS} of –5.0 V.
2. All inputs must have a rise and fall time of less than 15 ns.

• MPU Bus Read/Write II (68-family MPU)

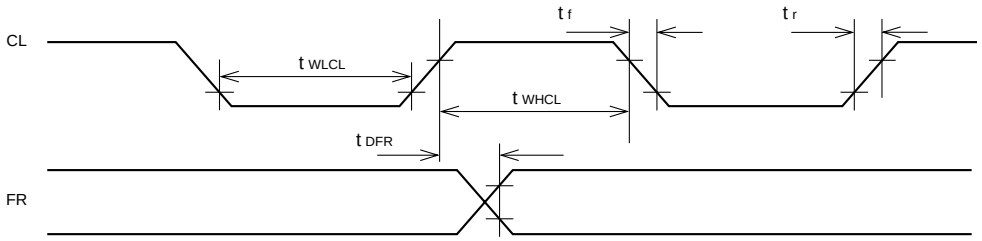


(Ta = –20 to 75 deg. C, V_{SS} = –5 V ±10%)

Parameters		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		t_{CYC6}		1000	—	ns	A0, $\overline{CS}$, R/W
Address setup time		t_{AW6}		20	—	ns	
Address hold time		t_{AH6}		10	—	ns	
Data setup time		t_{DS6}		80	—	ns	D0 to D7
Data hold time		t_{DH6}		10	—	ns	
Output disable time		t_{OH6}	C_L = 100 pF	10	60	ns	
Access time		t_{ACC6}		—	90	ns	
Enable pulse width	Read	t_{EW}		100	—	ns	E
	Write			8	—	ns	

Notes: 1. t_{cyc6} is the cycle time of $\overline{CS}$.E, not the cycle time of E.
2. All parameter values for a V_{SS} of –3.0 V are about 100% of their value for a V_{SS} of –5.0 V.
3. All inputs must have a rise and fall time of less than 15 ns.

• Display Control Signal Timing



Input

(Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	t_{WLCL}		35	—	—	µs	CL
High-level pulse width	t_{WHCL}		35	—	—	µs	
Rise time	t_r		—	30	150	ns	
Fall time	t_f		—	30	150	ns	
FR delay time	t_{DFR}		–2.0	0.2	2.0	µs	FR

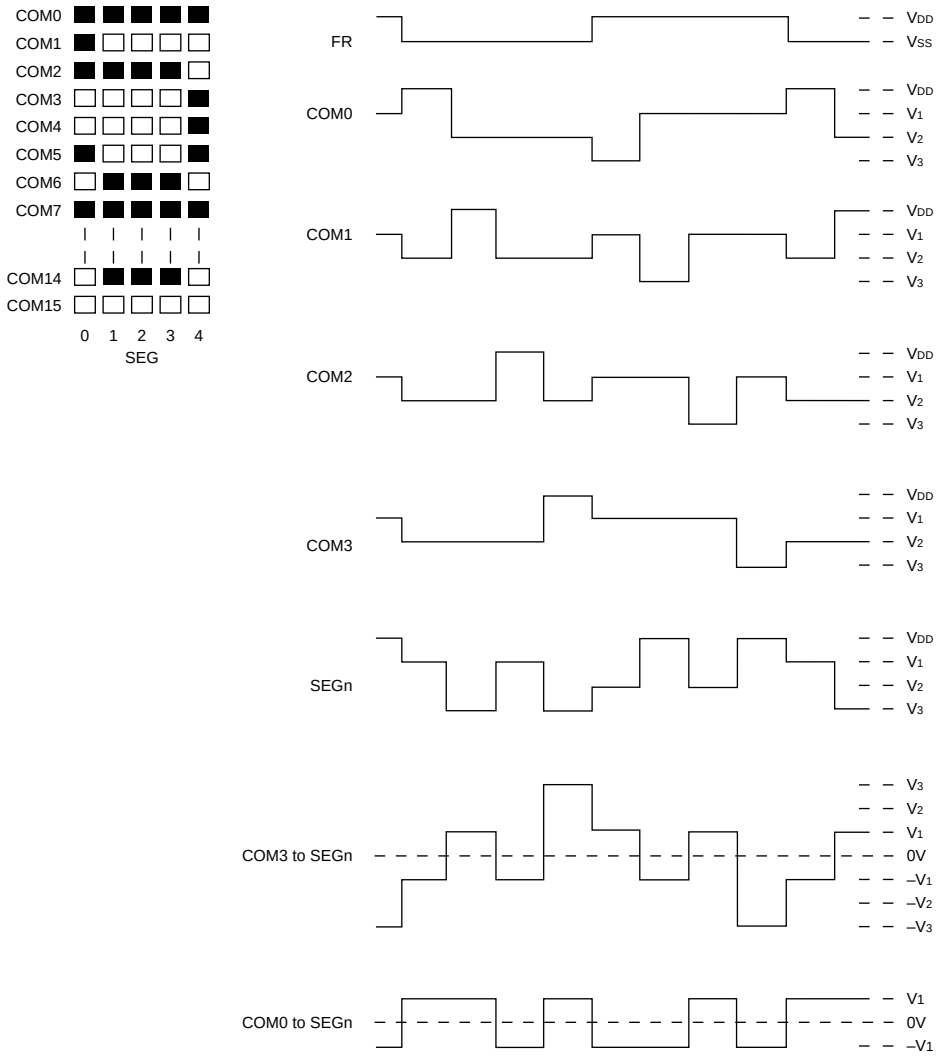
Output

(Ta = –20 to 75 deg. C, V_{SS} = –5.0 V ±10%)

Parameters	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	t_{DFR}	C_L = 100 pF	—	0.2	0.4	µs	FR

Notes: 1. The listed input t_{DFR} applies to the SED1540 in slave mode. The listed output t_{DFR} applies to the SED1540 in master mode.
2. All parameter values for a V_{SS} of –3.0 V are about 100% of their value for a V_{SS} of –5.0 V.

Example Drive Waveforms (1/3 Bias, 1/4 duty)



APPLICATION NOTES

The Oscillator

The external feedback resistor, Rf, is connected as shown in figure 3.

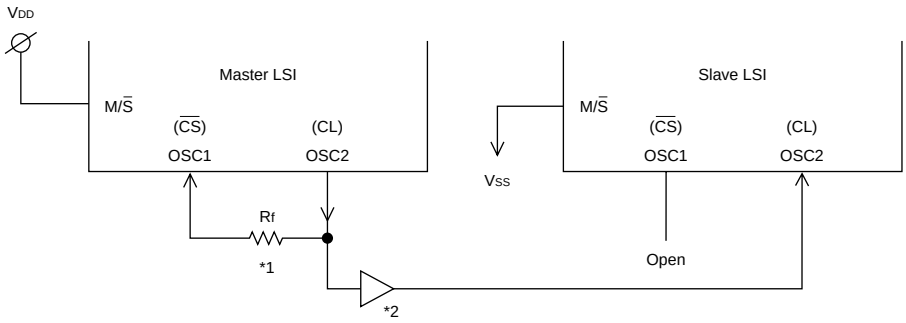
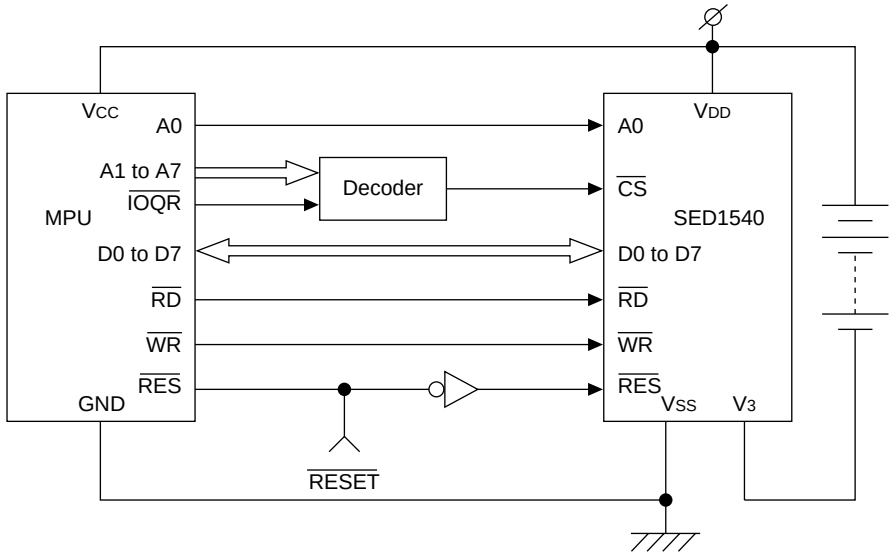


Figure 3 External Rf Connection

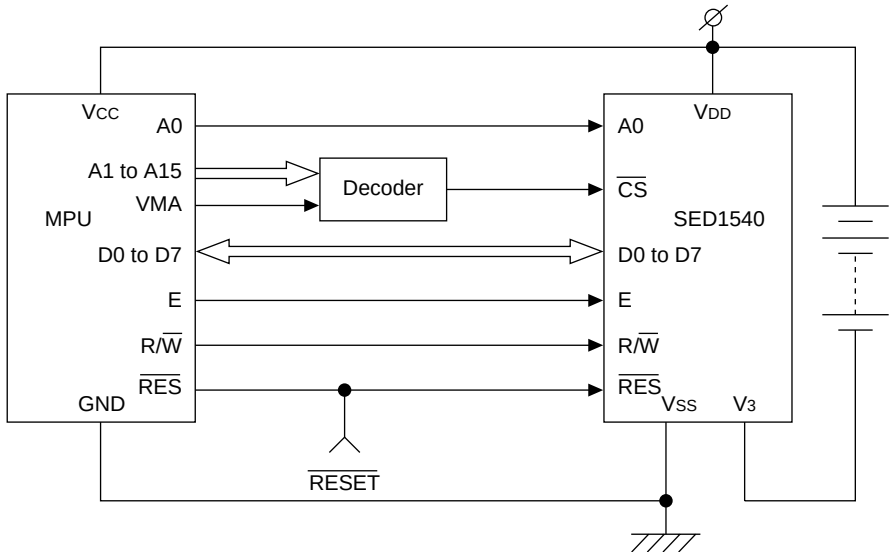
Notes: 1. Parasitic capacitance in the feedback loop will decrease fOSC. The leads of the feedback resistor, Rf, must be kept as short as possible. It may be necessary to reduce Rf to keep fOSC within its specified limits.
2. If a system has two or more slave drivers, a CMOS buffer will be required.

MPU Interface Configuration

80 Family MPU

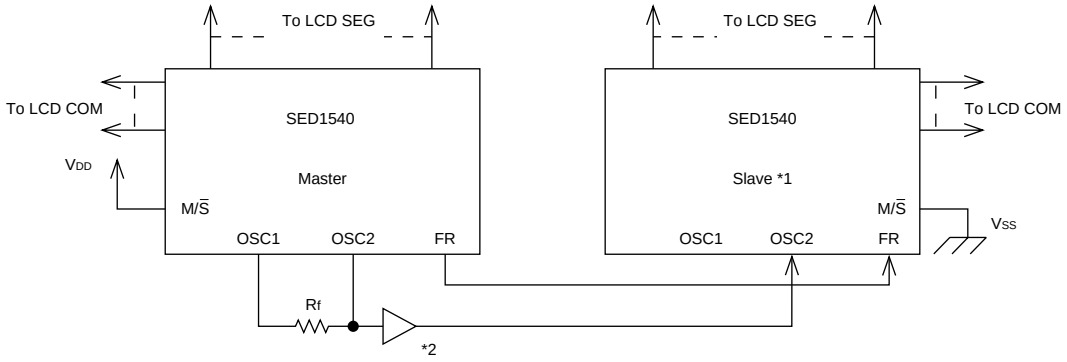


68 Family MPU

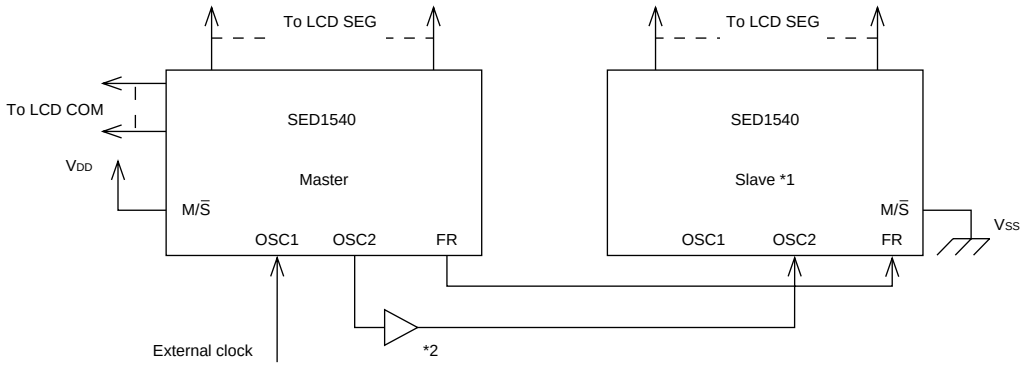


LCD Drive Interface Configuration

SED1540 - SDE1540 (Internal Oscillator)

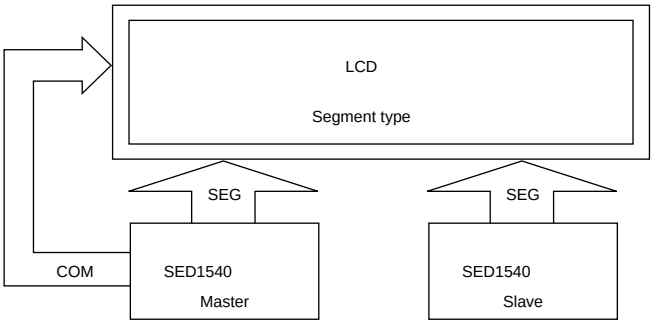


SED1540 - SED1540 (External clock)



Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

Panel Interface Configuration



7. SED1560 Series

Contents

OVERVIEW

The SED1560 series is a single-chip LCD driver for dot-matrix liquid crystal displays. It accepts serial or 8-bit parallel display data directly from a microprocessor and stores data in an on-chip 166 × 65-bit RAM.

The SED1560 features 167 common and segment outputs to drive either a 65 × 102-pixel (SED1560) display (4 rows × 6 columns with 16 × 16-pixel characters) or a 33 × 134-pixel (SED1561) display (2 rows × 8 columns with 16 × 16-pixel characters) or a 17 × 150-pixel (SED1562) display (1 row × 9 columns with 16 × 16 characters). In addition, two SED1560s can be connected together to drive a 65 × 268-pixel graphics display panel.

The SED 1560 series can read and write RAM data with the minimum current consumption as it does not require any external operation clock. Also, it has a built-in LCD power supply featuring the very low current consumption and, therefore, the display system of a high-performance but handy instrument can be realized by use of the minimum current consumption and LSI chip configuration.

The SED 1560 Series has the SED1560, SED1561 and SED1562 available according to the duty.

FEATURES

- Wide variety of duty and display areas

Model	Duty	LCD bias	Single-chip display area
SED1560	1/65 1/64 1/49 1/48	1/9 1/7	65 × 102 64 × 102 49 × 102 48 × 102
SED1561	1/33 1/32 1/25 1/24	1/7 1/5	33 × 134 32 × 134 25 × 134 24 × 134
SED1562	1/17 1/16	1/5	17 × 150 16 × 150

Note: The LCD bias is obtained if the built-in power supply is used.

- On-chip 166 × 65-bit display RAM
- Direct relationship between RAM bits and display pixels.
- High speed Interfaces to 6800- and 8080-series microprocessors
- Selectable 8-bit parallel/serial interface
- Many command functions
- On-chip LCD power circuit including DC/DC voltage converter, voltage regulator and voltage followers.
- On-Chip Contrast control.
- Two types of V_{REG} (Built-in power supply regulator temperature gradient).
- Type1 (SED156*D0*, SED156*DA*)...0.2%/˚C
- Type2 (SED1560DE*)...0.00%/˚C
- On-chip oscillator
- Ultra low power consumption
- Power Supply
  $V_{DD} - V_{SS}$ –2.4 V to –6.0 V
  $V_{DD} - V_5$ –3.5 V to –16.0 V
- Ta = –30 to 85°C
- CMOS process
- TCP, QTCP
- The system is not designed against the radio activity.

PAD LAYOUT

Chip size	:	8.08 × 5.28 mm
Pad pitch	:	100 µm (Min.)
Chip thickness	:	625 µm
	:	300 µm (Al-pad)

• Au-Bump

Bump size A	:	103 µm × 95 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
Bump size B	:	69 µm × 95 µm (Typ.) (other then the above)
Bump hight	:	23 µm (Typ.)

• Al-pad

Pad size A	:	111 µm × 102 µm (Typ.) (Pad No. 1 ~ 6, 18, 36 ~ 42, 44 ~ 49)
Bump size B	:	77 µm × 99 µm (Typ.) (Other then the above)

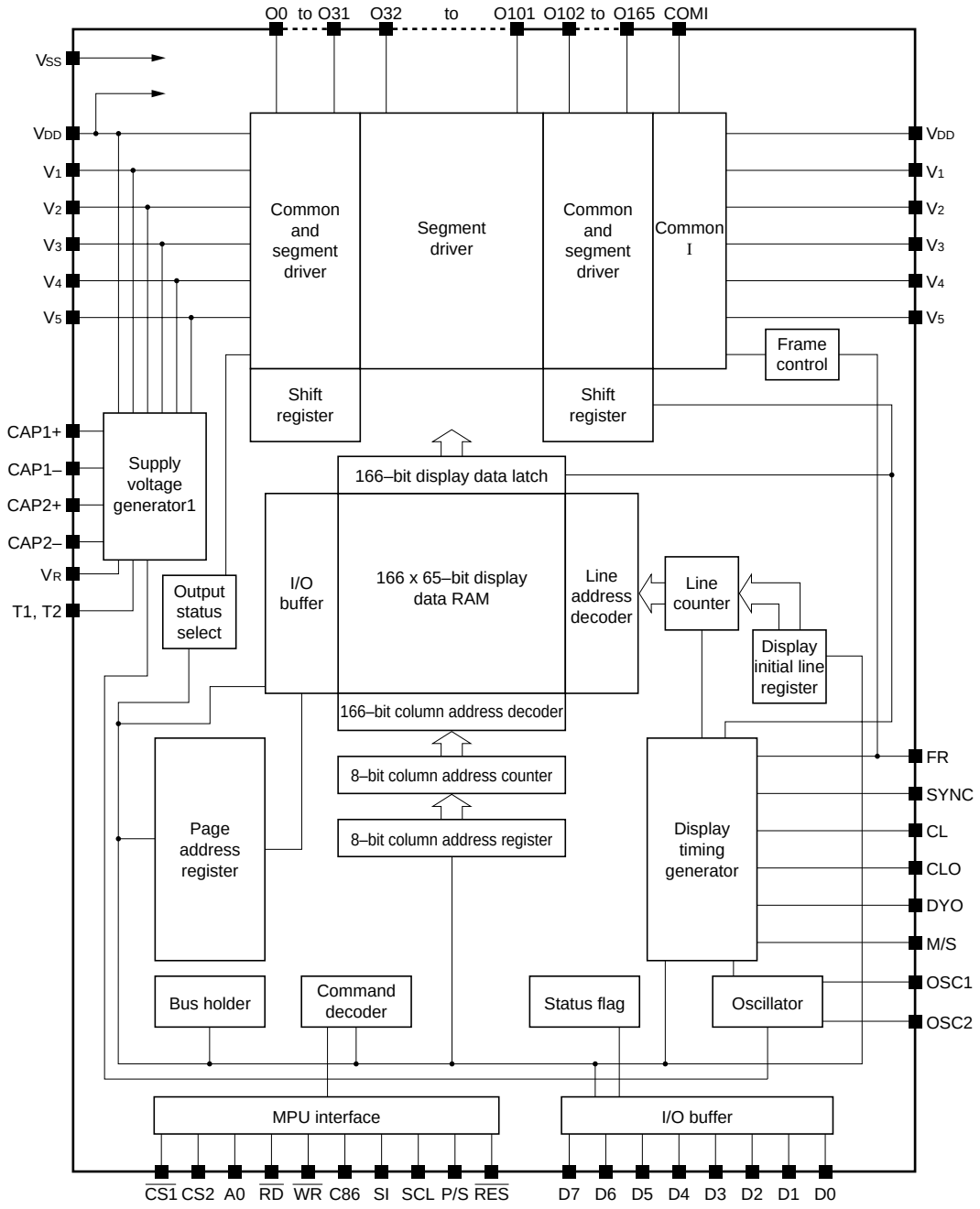
SED1560SERIES

PAD Center Coordinates

Unit : μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	V_5	3640	2487	55	05	-3887	1794	109	059	-2411	-2487	163	0113	2989	-2487
2	V_4	3489	2487	56	06	-3887	1694	110	060	-2311	-2487	164	0114	3089	-2487
3	V_3	3339	2487	57	07	-3887	1594	111	061	-2211	-2487	165	0115	3189	-2487
4	V_2	3188	2487	58	08	-3887	1494	112	062	-2111	-2487	166	0116	3289	-2487
5	V_1	3037	2487	59	09	-3887	1394	113	063	-2011	-2487	167	0117	3389	-2487
6	V_{DD}	2889	2487	60	010	-3887	1294	114	064	-1911	-2487	168	0118	3489	-2487
7	$\overline{M/S}$	2755	2487	61	011	-3887	1194	115	065	-1811	-2487	169	0119	3589	-2487
8	$\overline{RES}$	2604	2487	62	012	-3887	1094	116	066	-1711	-2487	170	0120	3689	-2487
9	SCL	2453	2487	63	013	-3887	994	117	067	-1611	-2487	171	0121	3887	-2206
10	SI	2302	2487	64	014	-3887	894	118	068	-1511	-2487	172	0122	3887	-2106
11	$\overline{P/S}$	2151	2487	65	015	-3887	794	119	069	-1411	-2487	173	0123	3887	-2006
12	$\overline{CS1}$	2001	2487	66	016	-3887	694	120	070	-1311	-2487	174	0124	3887	-1906
13	CS2	1850	2487	67	017	-3887	594	121	071	-1211	-2487	175	0125	3887	-1806
14	C86	1699	2487	68	018	-3887	494	122	072	-1111	-2487	176	0126	3887	-1706
15	$\overline{A0}$	1548	2487	69	019	-3887	394	123	073	-1011	-2487	177	0127	3887	-1606
16	$\overline{WR}$	1397	2487	70	020	-3887	294	124	074	-911	-2487	178	0128	3887	-1506
17	$\overline{RD}$	1247	2487	71	021	-3887	194	125	075	-811	-2487	179	0129	3887	-1406
18	V_{SS}	1077	2487	72	022	-3887	94	126	076	-711	-2487	180	0130	3887	-1306
19	D0	945	2487	73	023	-3887	-6	127	077	-611	-2487	181	0131	3887	-1206
20	D1	794	2487	74	024	-3887	-106	128	078	-511	-2487	182	0132	3887	-1106
21	D2	643	2487	75	025	-3887	-206	129	079	-411	-2487	183	0133	3887	-1006
22	D3	493	2487	76	026	-3887	-306	130	080	-311	-2487	184	0134	3887	-906
23	D4	342	2487	77	027	-3887	-406	131	081	-211	-2487	185	0135	3887	-806
24	D5	191	2487	78	028	-3887	-506	132	082	-111	-2487	186	0136	3887	-706
25	D6	40	2487	79	029	-3887	-606	133	083	-11	-2487	187	0137	3887	-606
26	D7	-111	2487	80	030	-3887	-706	134	084	89	-2487	188	0138	3887	-506
27	DYO	-261	2487	81	031	-3887	-806	135	085	189	-2487	189	0139	3887	-406
28	CLO	-412	2487	82	032	-3887	-906	136	086	289	-2487	190	0140	3887	-306
29	SYNC	-563	2487	83	033	-3887	-1006	137	087	389	-2487	191	0141	3887	-206
30	FR	-714	2487	84	034	-3887	-1106	138	088	489	-2487	192	0142	3887	-106
31	CL	-865	2487	85	035	-3887	-1206	139	089	589	-2487	193	0143	3887	-6
32	OSC2	-1015	2487	86	036	-3887	-1306	140	090	689	-2487	194	0144	3887	94
33	OSC1	-1166	2487	87	037	-3887	-1406	141	091	789	-2487	195	0145	3887	194
34	T2	-1317	2487	88	038	-3887	-1506	142	092	889	-2487	196	0146	3887	294
35	T1	-1468	2487	89	039	-3887	-1606	143	093	989	-2487	197	0147	3887	394
36	V_{SS}	-1638	2487	90	040	-3887	-1706	144	094	1089	-2487	198	0148	3887	494
37	CAP1+	-1789	2487	91	041	-3887	-1806	145	095	1189	-2487	199	0149	3887	594
38	CAP1-	-1939	2487	92	042	-3887	-1906	146	096	1289	-2487	200	0150	3887	694
39	CAP2+	-2090	2487	93	043	-3887	-2006	147	097	1389	-2487	201	0151	3887	794
40	CAP2-	-2241	2487	94	044	-3887	-2106	148	098	1489	-2487	202	0152	3887	894
41	V_{OUT}	-2392	2487	95	045	-3887	-2206	149	099	1589	-2487	203	0153	3887	994
42	V_5	-2543	2487	96	046	-3711	-2487	150	0100	1689	-2487	204	0154	3887	1094
43	V_R	-2674	2487	97	047	-3611	-2487	151	0101	1789	-2487	205	0155	3887	1194
44	V_{DD}	-2844	2487	98	048	-3511	-2487	152	0102	1889	-2487	206	0156	3887	1294
45	V_1	-2995	2487	99	049	-3411	-2487	153	0103	1989	-2487	207	0157	3887	1394
46	V_2	-3146	2487	100	050	-3311	-2487	154	0104	2089	-2487	208	0158	3887	1494
47	V_3	-3297	2487	101	051	-3211	-2487	155	0105	2189	-2487	209	0159	3887	1594
48	V_4	-3447	2487	102	052	-3111	-2487	156	0106	2289	-2487	210	0160	3887	1694
49	V_5	-3598	2487	103	053	-3011	-2487	157	0107	2389	-2487	211	0161	3887	1794
50	00	-3887	2294	104	054	-2911	-2487	158	0108	2489	-2487	212	0162	3887	1894
51	01	-3887	2194	105	055	-2811	-2487	159	0109	2589	-2487	213	0163	3887	1994
52	02	-3887	2094	106	056	-2711	-2487	160	0110	2689	-2487	214	0164	3887	2094
53	03	-3887	1994	107	057	-2611	-2487	161	0111	2789	-2487	215	0165	3887	2194
54	04	-3887	1894	108	058	-2511	-2487	162	0112	2889	-2487	216	COMI	3887	2294

BLOCK DIAGRAM



PIN DESCRIPTION

Power Supply

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>Supply</td><td>V_{DD}</td><td>5V supply. Common to MPU power supply pin V_{CC}.</td></tr>
<tr><td>2</td><td>Supply</td><td>V_{SS}</td><td>Ground</td></tr>
<tr><td>11</td><td>Supply</td><td>V_1 to V_5</td><td>LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltages should be determined on a V_{DD}-basis so as to satisfy the following relationship.
The voltages must satisfy the following relationship.
$V_{DD} \geq V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
When master mode selects, these voltages are generated on-chip.
<table>
<tr><th></th><th>SED1560D0B</th><th>SED1560DAB
SED1561D0B</th><th>SED1561DAB
SED1562D0B</th></tr>
<tr><td>V_1</td><td>1/9 V_5</td><td>1/7 V_5</td><td>1/5 V_5</td></tr>
<tr><td>V_2</td><td>2/9 V_5</td><td>2/7 V_5</td><td>2/5 V_5</td></tr>
<tr><td>V_3</td><td>7/9 V_5</td><td>5/7 V_5</td><td>3/5 V_5</td></tr>
<tr><td>V_4</td><td>8/9 V_5</td><td>6/7 V_5</td><td>4/5 V_5</td></tr>
</table>
</td></tr>
</table>

LCD Driver Supplies

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>O</td><td>CAP1+</td><td>DC/DC voltage converter capacitor 1 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP1–</td><td>DC/DC voltage converter capacitor 1 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2+</td><td>DC/DC voltage converter capacitor 2 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2–</td><td>DC/DC voltage converter capacitor 2 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>V_{OUT}</td><td>DC/DC voltage converter output</td></tr>
<tr><td>1</td><td>I</td><td>V_R</td><td>Voltage adjustment pin. Applies voltage between V_{DD} and V_5 using a resistive divider.</td></tr>
<tr><td>2</td><td>I</td><td>T1, T2</td><td>Liquid crystal power control terminals
<table>
<tr><th>T1</th><th>T2</th><th>Boosting circuit</th><th>Voltage regulation circuit</th><th>V/F circuit</th></tr>
<tr><td>L</td><td>L</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>L</td><td>H</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>L</td><td>Invalid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>H</td><td>Invalid</td><td>Invalid</td><td>Valid</td></tr>
</table>
</td></tr>
</table>

Microprocessor Interface

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>8</td><td>I/O</td><td>D0 to D7</td><td>Data inputs/outputs</td></tr>
<tr><td>1</td><td>I</td><td>A0</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
When LOW, the data on D0 to D7 is control data.
When HIGH, the data on D0 to D7 is display data.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RES}$</td><td>Reset input. System is reset and initialized when LOW.</td></tr>
<tr><td>2</td><td>I</td><td>$\overline{CS1}$, CS2</td><td>Chip select inputs. Data input/output is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RD}$ (E)</td><td>Read enable input. See note. 1</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>Write enable input. See note. 2</td></tr>
<tr><td>1</td><td>I</td><td>C86</td><td>Microprocessor interface select input. LOW when interfacing to 8080-series. HIGH when interfacing to 6800-series.</td></tr>
<tr><td>1</td><td>I</td><td>SI</td><td>Serial data input</td></tr>
<tr><td>1</td><td>I</td><td>SCL</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td></tr>
<tr><td>1</td><td>I</td><td>P/S</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating mode</th><th>Chip select</th><th>Data/command</th><th>Data input/ output</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td></tr>
</table>

Note 1
When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.

Note 2
When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, It will be read mode when $\overline{WR}$ is high and It will be write mode when $\overline{WR}$ is LOW.

Oscillator and Timing Control

<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>I</td><td>OSCI</td><td>Connecting pins for feedback resistors of the built-in oscillator
When M/S = “H”: Connect oscillator resistor Rf to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td></tr>
<tr><td>2</td><td>I/O</td><td>OSC2</td><td>When M/S = “L”: The OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the CL pin to the VSS level when using the internal oscillator circuit as the display clock.</td></tr>
<tr><td>1</td><td>I</td><td>CL</td><td>Display clock input. The line counter increments on the rising edge of CL and the display pattern is output on the falling edge. When use external display clock, OSC1 = “H”, OSC2 = “L” and reset this LSI by $\overline{RES}$ pin.</td></tr>
<tr><td>1</td><td>O</td><td>CLO</td><td>Display clock output. When using the master operation, the clock signal is output on this pin. Connect CLO to YSCL on the common driver.</td></tr>
<tr><td>1</td><td>I</td><td>M/S</td><td>Master/slave select input. Master makes some signals for display, and slave gets them. This is for display syncronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating mode</th><th>Internal oscillator</th><th>Power supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156XDOB</td><td>Low</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note
I = input mode
O = output mode</td></tr>
<tr><td>1</td><td>I/O</td><td>FR</td><td>LCD AC drive signal input/output. If the SED1560 series MPU’s are used in master and slave configuration, this pin must be connected to each FR pin. Also when the SED1560 series is used as the master MPU, this pin must be connected to the FR pin of the common driver. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>I/O</td><td>SYNC</td><td>Display sync input/output. If the SED1560 series MPU’s are used in master and slave configuration, this pin must be connected to each SYNC pin. Output is selected when M/S is HIGH, and Input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>O</td><td>DYO</td><td>Start-up output for common driver. Connect to DIO of the common driver.</td></tr>
</table>

LCD Driver Outputs

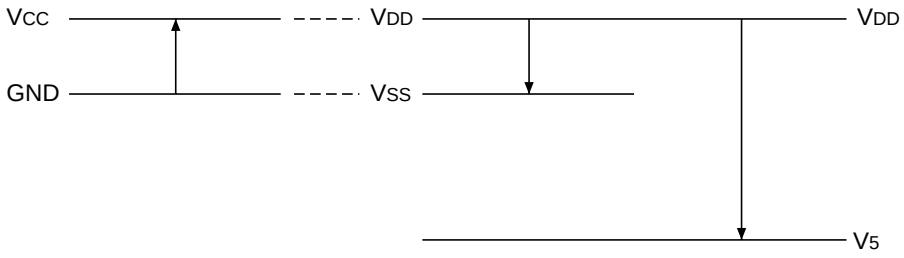
<table>
<tr><th>Number of pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>166</td><td>O</td><td>O0 to O165</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.

For segment outputs, the ON voltage level is given as shown in the following table.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">LCD ON voltage</th></tr>
<tr><th>Normal display</th><th>Inverse display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table.
<table>
<tr><th>Scan data</th><th>FR</th><th>LCD ON voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>HIGH</td><td>V_1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>HIGH</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>1</td><td>O</td><td>COMI</td><td>LCD driver common output. Common outputs when the “DUTY + 1” command is executed are as follows:
<table>
<tr><th></th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>SED1560</td><td>COM64, COM48</td><td>V_1 or V_4</td></tr>
<tr><td>SED1561</td><td>COM32, COM24</td><td>V_1 or V_4</td></tr>
<tr><td>SED1562</td><td>COM16</td><td>V_1 or V_4</td></tr>
</table>
Common output special for the indicator.</td></tr>
</table>

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 +0.03	V
Supply voltage range (2) (DC/DC When in use)		–6.0 to 0.3 (when triple boosting)	
Driver supply voltage range (1)	V_5	–18.0 to 0.3	V
Driver supply voltage range (2)	V_1, V_2, V_3, V_4	V_5 to 0.3	V
Input voltage range	V_{IN}	V_{SS} –0.3 to 0.3	V
Output voltage range	Vo	V_{SS} –0.3 to 0.3	V
Operating temperature range	Topr	–30 to 85	deg. C
Storage temperature range (TCP)	Tstr	–55 to 100	deg. C



Notes: 1. The voltages shown are based on V_{DD} = 0 V.
2. Always keep the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ for voltages V_1, V_2, V_3 and V_4.
3. If LSIs are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. A guarantee on operating temperature below –30°C may be studied individually.

DC Characteristics

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommended operation	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Operational				–6.0		–2.4		*1
Operating voltage (2)	Operational	V_5			–16.0		–4.0	V	V_5 *2
	Operational	V_1, V_2			0.4 × V_5		V_{DD}	V	V_1, V_2
	Operational	V_3, V_4			V_5		0.6 × V_5	V	V_3, V_4
High-level input voltage		V_{IHC1}			0.3 × V_{SS}		V_{DD}	V	*3
		V_{IHC2}			0.15 × V_{SS}		V_{DD}		*4
		V_{IHC1}	V_{SS} = –2.7 V		0.3 × V_{SS}		V_{DD}		*3
		V_{IHC2}	V_{SS} = –2.7 V		0.2 × V_{SS}		V_{DD}		*4
Low-level input voltage		V_{ILC1}			V_{SS}		0.7 × V_{SS}	V	*3
		V_{ILC2}			V_{SS}		0.85 × V_{SS}		*4
		V_{ILC1}	V_{SS} = –2.7 V		V_{SS}		0.7 × V_{SS}		*3
		V_{ILC2}	V_{SS} = –2.7 V		V_{SS}		0.8 × V_{SS}		*4
High-level output voltage		V_{OHC1}		I_{OH} = –1 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}		I_{OH} = –120 µA	0.2 × V_{SS}		V_{DD}		OSC2
		V_{OHC1}	V_{SS} = –2.7 V	I_{OH} = –0.5 mA	0.2 × V_{SS}		V_{DD}	V	*5
		V_{OHC2}	V_{SS} = –2.7 V	I_{OH} = –50 µA	0.2 × V_{SS}		V_{DD}		OSC2
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}		I_{OL} = 120 µA	V_{SS}		0.8 × V_{SS}		OSC2
		V_{OLC1}	V_{SS} = –2.7 V	I_{OL} = 0.5 mA	V_{SS}		0.8 × V_{SS}	V	*5
		V_{OLC2}	V_{SS} = –2.7 V	I_{OL} = 50 µA	V_{SS}		0.8 × V_{SS}		OSC2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0		1.0	µA	*6
Output leakage current		I_{LO}			–3.0		3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V_5 = –14.0 V		2.0	3.0	KΩ	O0 to O166
				V_5 = –8.0 V		3.0	4.5		*8
Static power consumption		I_{SSQ}				0.00	5.0	µA	V_{SS}
		I_{5Q}	V_5 = –18.0V			0.01	15.0	µA	V_5
Input terminal capacity		C_{IN}	Ta = 25°C	f=1MHz		5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	R_f=1 MΩ	V_{SS} = –5V	15	18	22	kHz	*9
			±2%	V_{SS} = –2.7V	11	16	21		

Reset time	t_R		1.0			µs	*10
Reset “L” pulse width	t_{RW}		1.0			µs	*11

Built-in power circuit	Input voltage	V_{SS}		–6.0		–2.4	V	*12
	Amplified output voltage	V_{OUT}	when triple boosting	–18.0			V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}		–16.0		–6.0	V	V_{OUT}
	Voltage regulutor operation voltage	V_5 ①	Supplied to SED1560D$_{OB}$	–16.0		–6.0	V	*13
		V_5 ②	Supplied to SED1561D$_{OB}$	–16.0		–5.0	V	
		V_5 ③	Supplied to SED1561D$_{AB}$	–16.0		–4.0	V	
		V_5 ④	Supplied to SED1562D$_{OB}$	–16.0		–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C	–2.35	–2.5	–2.65	V	

*V_{SS} = –2.4V is on the same basis as V_{SS} = –2.7V.

* See the 4-12 page for details.

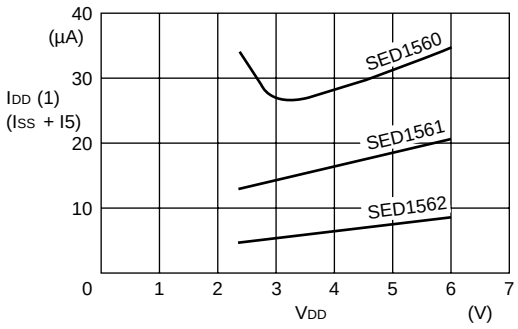
When dynamic current consumption (I) is displaye; the built-in power circuit is on and T1 = T2 = Low.

V_{DD} = 0 V, V_{SS} = –5 V ± 10%, Ta = –30 to +85°C unless otherwise noted.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
SED1560	I_{DD} (1)	V_5 = –12.5 V; 3 times amplified		169	340	µA	*16
SED1561		V_5 = –8.0 V ; 3 times amplified		124	250	µA	
SED1562		V_5 = –6.0 V ; 2 times amplified		53	110	µA	
		V_{SS} = –2.7 V; 3 times amplified V_5 = –6.0 V		66	130	µA	

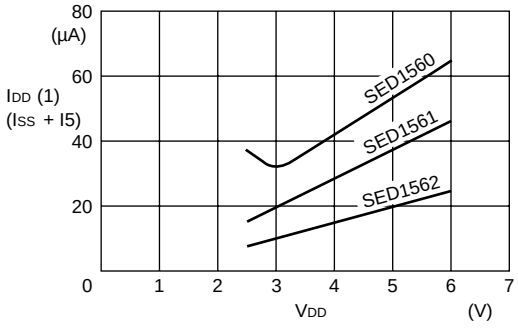
Typical current consumption characteristics

- Dynamic current consumption (I), if an external clock and an external power supply are used.



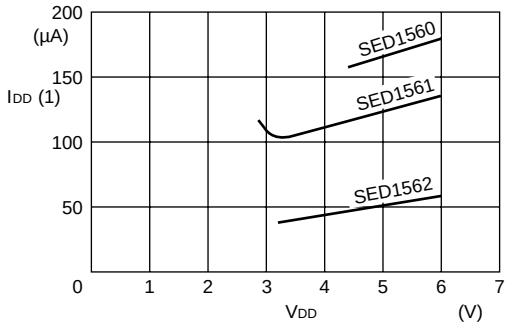
Conditions: The built-in power supply is off but the external one is used.
SED1560 $V_5 – V_{DD}$ = –12.5 V
SED1561 $V_5 – V_{DD}$ = –8.0 V
SED1562 $V_5 – V_{DD}$ = –6.0 V
External clock:
SED1560 f_{CL} = 4 kHz
SED1561 f_{CL} = 2 kHz
SED1562 f_{CL} = 1 kHz
Remarks: *14

- Dynamic current consumption (I), if the built-in oscillator and the external power supply are used.



Conditions: The built-in power supply is off but the external one is used.
SED1560 $V_5 – V_{DD}$ = –12.5 V
SED1561 $V_5 – V_{DD}$ = –8.0 V
SED1562 $V_5 – V_{DD}$ = –6.0 V
Internal oscillation:
SED1560 R_f = 1 MΩ
SED1561 R_f = 1 MΩ
SED1562 R_f = 1 MΩ
Remarks: *15

- Dynamic current consumption (I), if the built-in power supply is used.



Conditions: The built-in power supply is on and T1 = T2 = Low.

SED1560 $V_5 - V_{DD}$ = –12.5 V; 3 times amplified

SED1561 $V_5 - V_{DD}$ = –8.0 V; 3 times amplified

SED1562 $V_5 - V_{DD}$ = –6.0 V; 2 times amplified

Internal oscillation:

SED1560 R_f = 1 MΩ

SED1561 R_f = 1 MΩ

SED1562 R_f = 1 MΩ

Remarks: *16

Notes: *1. Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.

*2. The operating voltage range of the V_{SS} and V_5 systems (see Figure 11).
The operating voltage range is applied if an external power supply is used.

*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 and T2.

*4. Pins CL, SCL, and $\overline{RES}$

*5. Pins D0 to D7, FR, SYNC, CL0, and DY0

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.

*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.

*8. The resistance when the 0.1-volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).
R ON = 0.1 V/ΔI
(ΔI is the current that flows when 0.1 VDC is applied during power-on.)

*9. The relationship between the oscillation frequency, frame and Rf value (see Figure 10).

*10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the SED156∗ is usually operable after "tr" time.

*11. Specifies the minimum pulse width of $\overline{RES}$" signal. The Low pulse greater than "t_{RW}" must be entered for reset.

*12. If the voltage is amplified three times by the built-in power circuit, the primary power V_{SS} must be used within the input voltage range.

*13. The V_5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.

*14, 15, 16 Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.
The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the SED1560D_{0B} is set to 1/64 duty, the SED1561D_{0B} is set to 1/32 duty, and the SED1562D_{0B} is set to 1/16 duty.

*14. Applied if an external clock is used and if not accessed by the MPU.

*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.

*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU. Measuring conditions: C1 = 4.7 μF, C2 = 0.47 μF, Ra + Rb = 2 MΩ
This includes the current that flows through the voltage regulator resistor (Ra + Rb = 2 MΩ). If the built-in power circuit is used, the current consumption is equal to the current of V_{SS} power.

Oscillator frequency vs. frame vs. Rf [SED156*D0B]

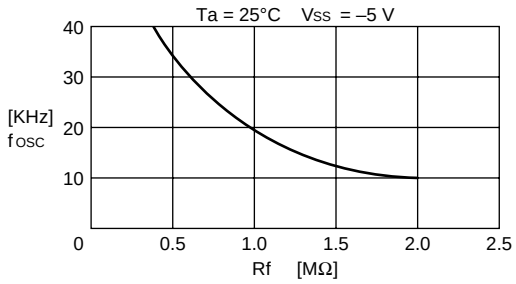


Figure 10 (a)

The relationship between oscillator frequency f_{OSC} and LCD frame frequency f_F is obtained from the following expression.

	Duty	f_F
SED1560	1/64	$f_{OSC/256}$
	1/48	$f_{OSC/192}$
SED1561	1/32	$f_{OSC/256}$
	1/24	$f_{OSC/192}$
SED1562	1/16	$f_{OSC/256}$

(f_F indicates not f_F signal cycle but cycle of LCD AC.)

External clock (f_{CL}) vs. frame [SED156*D*B]

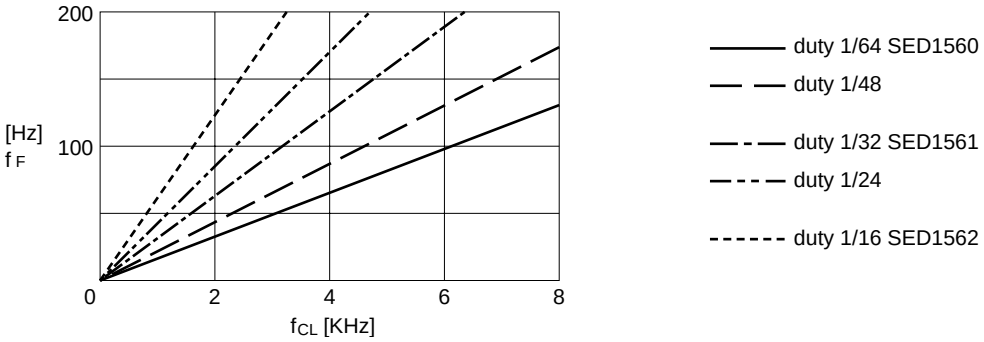


Figure 10 (b)

Operating voltage range for V_{SS} and V_5

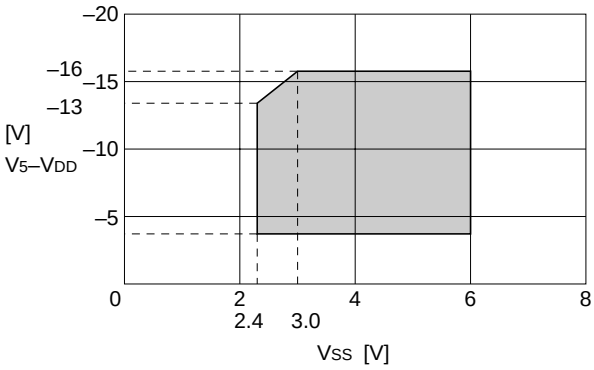


Figure 11

Power consumption during access (I_{DD} (2)) - MPU access cycle

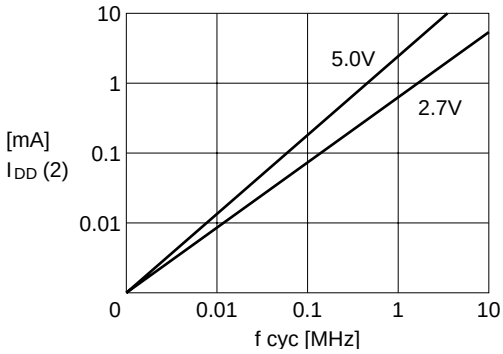


Figure 12

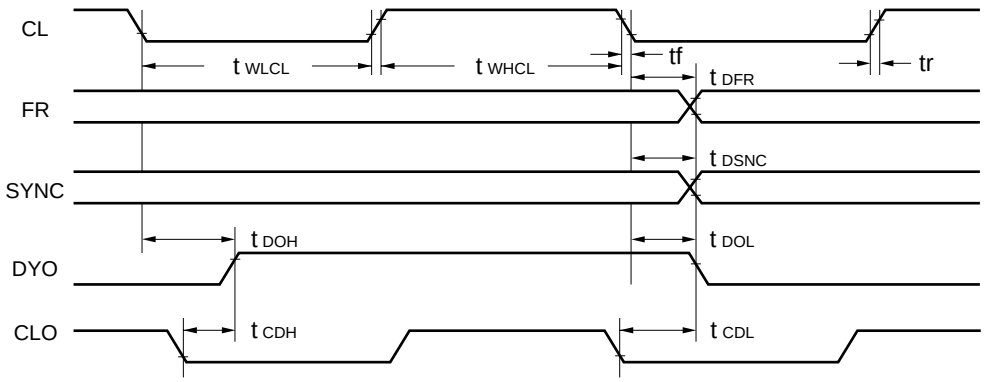
This graphic shows the current consumption when the vertical patterns are written during "fcyc". If not accessed, I_{DD}(1) is only shown.

Reset

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Reset time	t_R	See note.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

Note
t_R is measured from the rising edge of $\overline{RES}$. The SED1560 enters normal operating mode after a reset.

Display control timing



Input timing

Vss = –5.5 to –4.5 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	30	—	ns
CL fall time	tf		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Vss = –4.5 to –2.7 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	tr		—	40	—	ns
CL fall time	tf		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Notes: 1. Effective only when the SED156*DOB is in the master mode.
2. The FR/SYNC delay time input timing is provided in the slave operation.
The FR/SYNC delay time output timing is provided in the master operation.
3. Each timing is based on 20% and 80% of VSS.
4. When usingin the range of VSS = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

Output timing

V_{SS} = –5.5 to –4.5 V, Ta = –30 to 85 deg. C

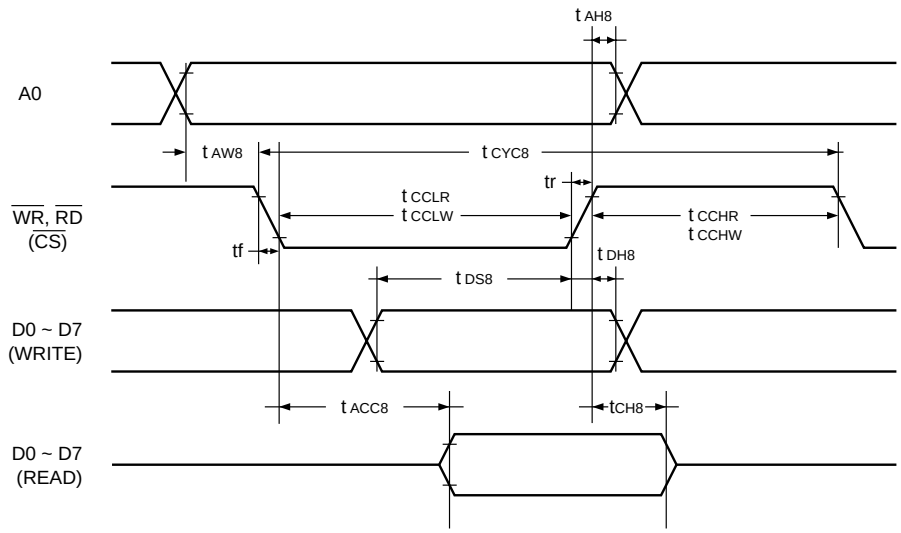
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	C_L = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}		—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO Low-level delay time	t_{CDL}	SED156✻D0B operating in master mode only	10	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156✻D0B operating in master mode only	10	40	100	ns

V_{SS} = –4.5 to –2.7 V, Ta = –30 to 85 deg. C

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
FR delay time	t_{DFR}	C_L = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}		—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156✻D0B operating in master mode only	10	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156✻D0B operating in master mode only	10	100	200	ns

(1) System buses

Read/write characteristics I (80-series MPU)



V_{SS} = –5.0 ±10%, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		10		ns
Address setup time		t_{AW8}		10		ns
System cycle time		t_{CYC8}		200		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22		ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77		ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172		ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f			15	ns

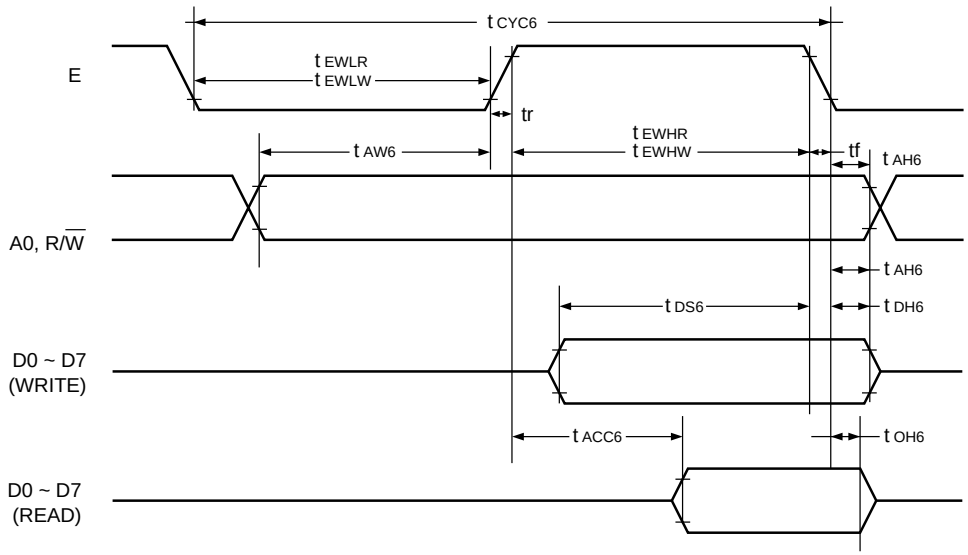
V_{SS} = –2.7 ~ –4.5 V, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Address hold time	A0, CS	t_{AH8}		0		ns
Address setup time		t_{AW8}		0		ns
System cycle time		t_{CYC8}		450		ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44		ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194		ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394		ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244		ns
Data setup time		t_{DS8}		20		ns
Data hold time		t_{DH8}		10		ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100pF		140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f			15	ns

Notes:
1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \le (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \le (t_{CYC8} - t_{CCLR} - t_{CCHR})$
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the RD or WR signal is in the low level.
   If read/write operation is performed by the RD or WR signal while CS is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.
   If read/write operation is performed by CS while the RD or WR signal is in the low level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(2) System buses

Read/write characteristics II (68-series MPU)



V_{SS} = –5.0 V ± 10%, Ta = –30 ~ 85 °C

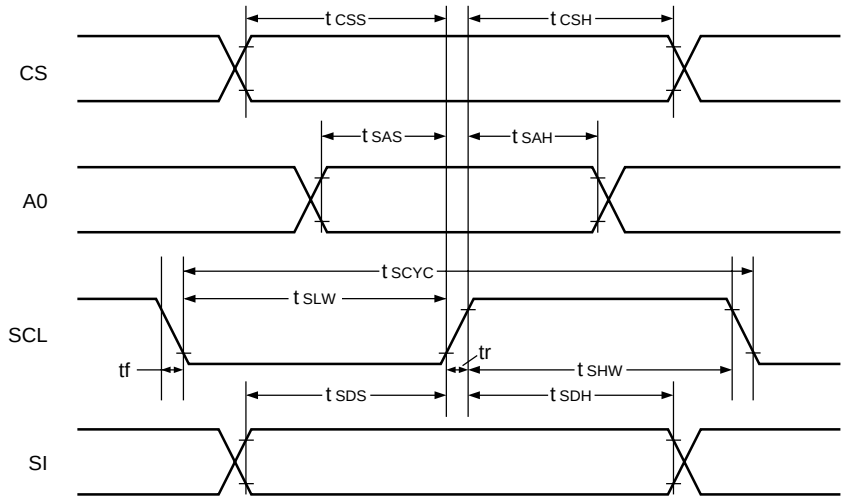
Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		200		ns
Address setup time		(A0)	t_{AW6}		10		ns
Address hold time		R/$\overline{W}$	t_{AH6}		10		ns
Data setup time		D0~D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		n
Output disable time			t_{OH6}	C_L = 100pF	10	50	ns
Access time			t_{ACC5}			70	ns
Enable H pulse width	READ	E	t_{EWHR}		77		ns
	WRITE		t_{EWHW}		22		ns
Enable L pulse width	READ	E	t_{EWLR}		117		ns
	WRITE		t_{EWLW}		172		ns
Input signal change time			t_r, t_f			15	ns

V_{SS} = –2.7 V ~ 4.5 V, Ta = –30 ~ 85 °C

Item		Signal	Symbol	Conditions	Min.	Max.	Unit
System cycle time			t_{CYC6}		450		ns
Address setup time		A0	t_{AW6}		0		ns
Address hold time		R/$\overline{W}$	t_{AH6}		0		ns
Data setup time		D0 to D7	t_{DS6}		20		ns
Data hold time			t_{DH6}		10		ns
Output disable time			t_{OH6}	C_L = 100pF	20	100	ns
Access time			t_{ACC5}			140	ns
Enable H pulse width	READ	E	t_{EWHR}		194		ns
	WRITE		t_{EWHW}		44		ns
Enable L pulse width	READ	E	t_{EWLR}		244		ns
	WRITE		t_{EWLW}		394		ns
Input signal change time			t_r, t_f			15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \le (t_{CYC6}-t_{EWLW}-t_{EWHW})$ or $t_r + t_f \le (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
2. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
3. Read/write operation is performed while CS ($\overline{CS1}$ and CS2) is active and the E signal is in the high level. If read/write operation is performed by the E signal while CS is active, it is determined by the E signal timing.
If read/write operation is performed by CS while the E signal is in the high level, it is determined by the CS active timing.
4. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

(3) Serial interface



V_{SS} = –5.0 V ±10%, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250		ns
SCL High pulse width		t_{SHW}		75		ns
SCL Low pulse width		t_{SLW}		75		ns
Address setup time	A0	t_{SAS}		50		ns
Address hold time		t_{SAH}		200		ns
Data setup time	SI	t_{SDS}		50		ns
Data hold time		t_{SDH}		30		ns
CS-SCL time	CS	t_{CSS}		30		ns
		t_{CSH}		400		
Input signal change time		t_r, t_f			50	ns

V_{SS} = –2.7 V ~ –4.5 V, Ta = –30 ~ 85 °C

Item	Signal	Symbol	Conditions	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500		ns
SCL High pulse width		t_{SHW}		150		ns
SCL Low pulse width		t_{SLW}		150		ns
Address setup time	A0	t_{SAS}		100		ns
Address hold time		t_{SAH}		400		ns
Data setup time	SI	t_{SDS}		100		ns
Data hold time		t_{SDH}		100		ns
CS-SCL time	CS	t_{CSS}		60		ns
		t_{CSH}		800		
Input signal change time		t_r, t_f			50	ns

*1. All signal timings are limited based on the 20% and 80% of V_{SS} voltage.
*2. When usingin the range of V_{SS} = –2.4 ~ –4.5V, raise the above ratings for –2.7 ~ –4.5V equally by 30%.

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Parallel/serial interface

Parallel data can be transferred in either direction between the controlling microprocessor and the SED1560 series through the 8-bit I/O buffer (D0 to D7). Serial data can be sent from the microprocessor to the SED1560 series through the serial data input (SI), but not from the SED1560 series to the microprocessor. The parallel or serial interface is selected by P/S as shown in table 1.

Table 1. Parallel/serial interface selection

P/S	Input type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	D0 to D7
HIGH	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	×	×	D0 to D7
LOW	Serial	$\overline{CS1}$	CS2	A0	×	×	×	SI	SCL	(Hz)

Note
× = don't care

For the parallel interface, the type of microprocessor is selected by C86 as shown in table 2.

Table 2. Microprocessor selection for parallel interface

C86	MPU bus type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
HIGH	6800-series	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
LOW	8080-series	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Parallel interface

A0, $\overline{WR}$ (or R/W) and $\overline{RD}$ (or E) identify the type of parallel data transfer to be made as shown in table 3.

Serial interface

The serial interface comprises an 8-bit shift register and a 3-bit counter. These are reset when $\overline{CS1}$ is HIGH and CS2 is LOW. When these states are reversed, serial data and clock pulses can be received from the microprocessor on SI and SCL, respectively.

Table 3. Parallel data transfer

Common	6800 series		8080 series		Description
A0	R/W	E	$\overline{RD}$	$\overline{WR}$	
1	1	1	0	1	Display data read out
1	0	1	1	0	Display data write
0	1	1	0	1	Status read
0	0	1	1	0	Write to internal reigister (command)

Serial data is read on the rising edge of SCL and must be input at SI in the sequence D7 to D0. On every eighth clock pulse, the data is transferred from the shift register and processed as 8-bit parallel data.
Input data is display data when A0 is HIGH and control data when A0 is LOW. A0 is read on the rising edge of every eighth clock signal.
The SLC signal is affected by the termination reflection and external noise caused by the line length. The operation check on the actual machine is recommended.

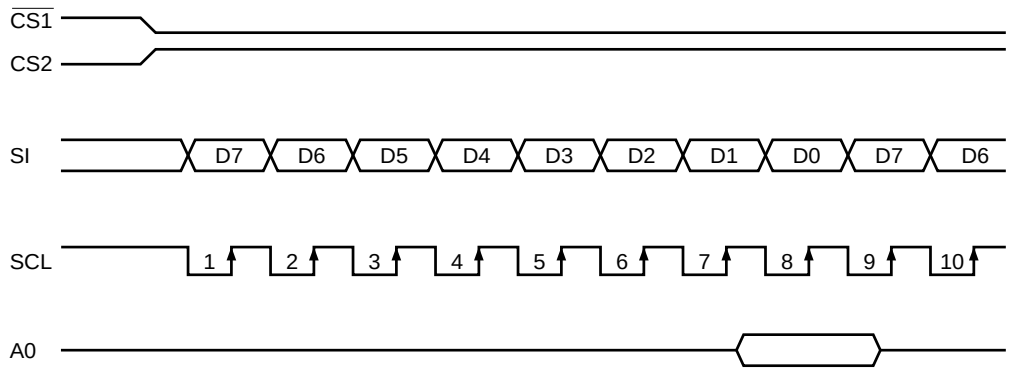


Figure 1. Serial interface timing

Chip select inputs

The SED1560 series has two chip select pins: $\overline{CS1}$ and CS2, and data exchange between the microprocessor and the SED1560 series is enabled when $\overline{CS1}$ is LOW and CS2 is HIGH. When these pins are set to any other combination, D0 to D7 are high impedance. The A0, $\overline{RD}$, $\overline{WR}$, SI and SCI inputs are disabled. If the serial input interface has been selected, the shift register and counter are reset. The Reset signal is entered independent from the $\overline{CS1}$ and CS2 status.

Data Transfer

To match the timing of the display data RAM and registers to that of the controlling microprocessor, the SED1560 series uses an internal data bus and bus buffer. A kind of pipeline processing takes place. When the microprocessor reads the contents of RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Likewise, when the microprocessor writes data to display data RAM, the data is first stored in the bus buffer before being written to RAM at the next write cycle.

When writing data from the microprocessor to RAM, there is no delay since data is automatically transferred from the bus buffer to the display data RAM. If the data rate is required to slow down, the microprocessor can insert an NOP instruction which has the same affect as executing a wait procedure.

When a sequence of address sets is executed, a dummy read cycle must be inserted between each pair of address sets. This is necessary because the addressed data from the RAM is delayed one cycle by the bus buffer, before it is sent to the microprocessor. A dummy read cycle is thus necessary after an address set and after a write cycle.

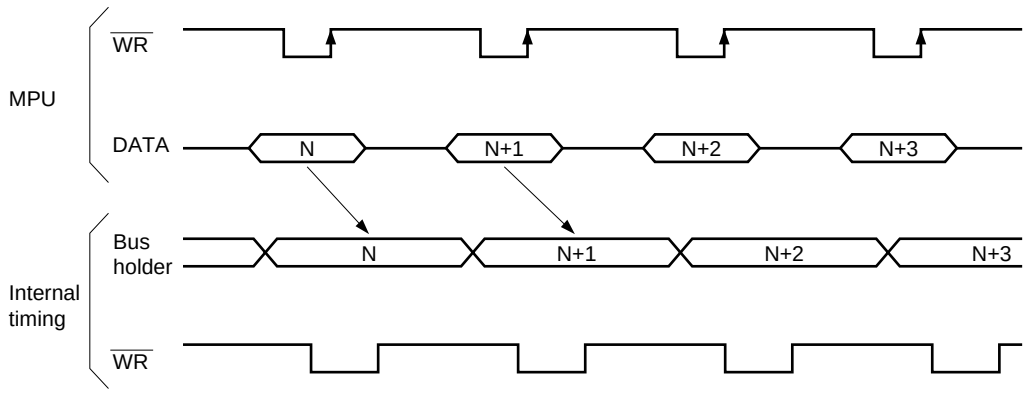


Figure 2. Write timing

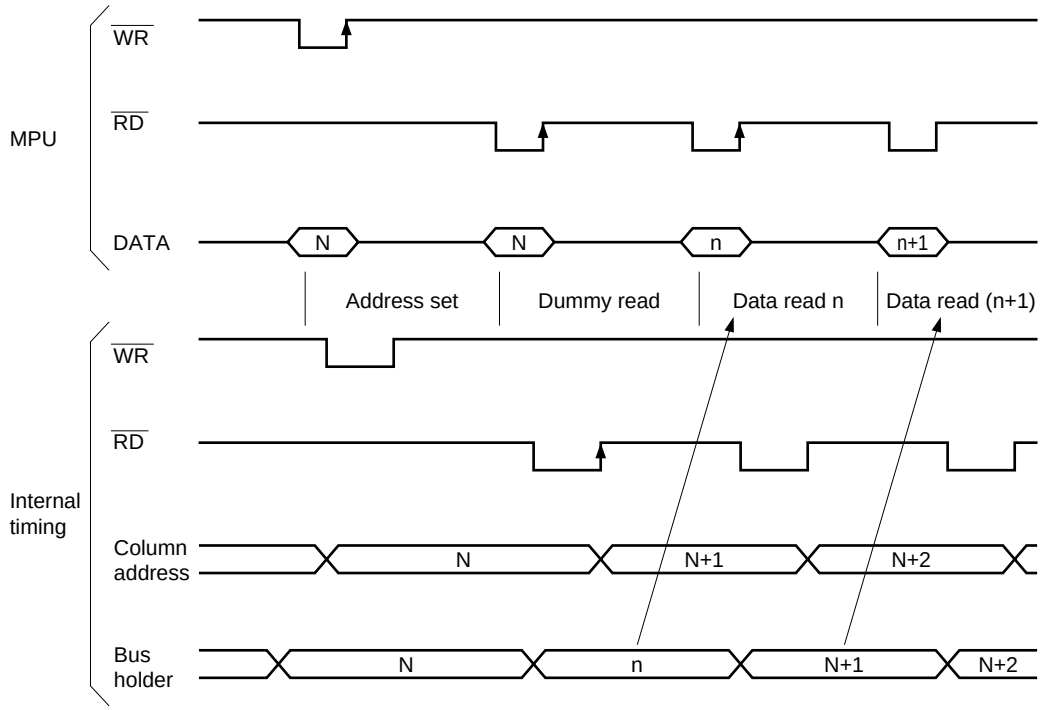


Figure 3. Read timing

Status Flag

The SED1560 series has a single bit status flag, D7. When D7 is HIGH, the device is busy and will only accept a Status Read command. If cycle times are monitored ed carefully, this flag does not have to be checked before each command, and microprocessor capabilities can be fully utilized.

Display Data RAM

The display data RAM stores pixel data for the LCD. It is a 166-column × 65-row addressable array as shown in figure 4.

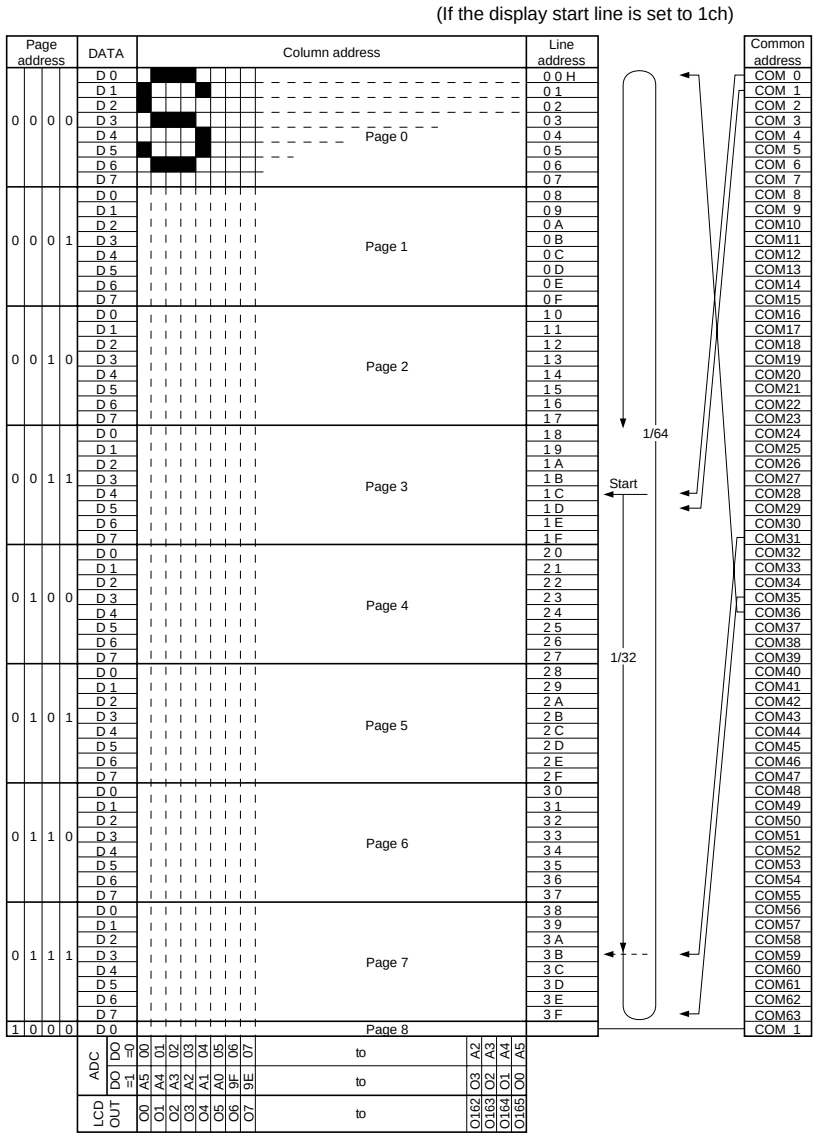


Figure 4. Display data RAM addressing

Note
For a 1/65 and 1/33 display duty cycles, page 8 is accessed following 1BH and 3BH, respectively.

The 65 rows are divided into 8 pages of 8 lines and a ninth page with a single line (D0 only). Data is read from or written to the 8 lines of each page directly through D0 to D7.

The time taken to transfer data is very short, because the microprocessor inputs D0 to D7 correspond to the LCD common lines as shown in figure 5. Large display configurations can thus be created using multiple SED1560s.

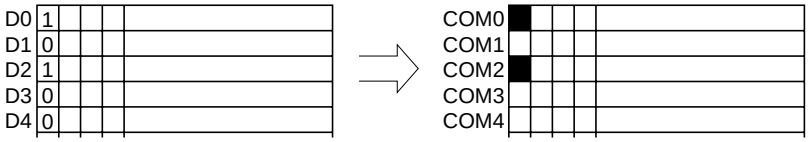


Figure 5. RAM-to-LCD data transfer

The microprocessor reads from and writes to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as data is being displayed, without causing the LCD to flicker.

Column Address Counter

The column address counter is an 8-bit presettable counter that provides the column address to display data RAM. See figure 4. It is incremented by 1 each time a read or write command is received. The counter automatically stops at the highest address, A6H. The contents of the column address counter are changed by the Column Address Set command. This counter is independent of the page address register.
When the Select ADC command is used to select inverse display operation, the column address decoder inverts the relationship between the RAM column data and the display segment outputs.

Page Address Register

The 4-bit page address register provides the page address to display data RAM. The contents of the register are changed by the Page Address Set command.
Page address 8 (D3 = H, D2, D1, D0 = L) is a special use RAM area for the indicator.

Initial Display Line Register

The initial display line register stores the address of the RAM line that corresponds to the first (normally the top) line (COM0) of the display. See figure 4. The contents of this 6-bit register are changed by the Initial Display Line command. At the start of each LCD frame, synchronized with SYNC, the initial line is copied to the line counter. The line counter is then incremented on the CL clock signal once for every display line. This generates the line addresses for the transfer of the 166 bits of RAM data to the LCD drivers.
If a 1/65 or 1/33 display duty cycle is selected by the Duty + 1 command, the line address corresponding to the 65th or 33rd SYNC signal is changed and the indicator special-use line address is selected. If the Duty + 1 command is not used, the indicator special-use line address is not selected.

Output Selection Circuit

The number of common (COM) and segment (SEG) driver outputs can be selected to fit different LCD panel configurations by the output selection circuit.
There are 70 segment-only outputs (O32 to O101) and 96 common or segment dual outputs (O0 to O31 and O102 to O165). A command select the status of the dual common/segment outputs. Figure 6 shows the six different LCD driver arrangements.
Necessary LCD driver voltage is automatically allocated to the COM/SEG dual outputs when their function is determined by the output selection circuit.
The SED1560 selects Case 1, 2 or 6 while the SED1561 selects Case 3, 4, 5 or 6. As to the SED1562, COM/SEG output status cannot be selected, being fixed.

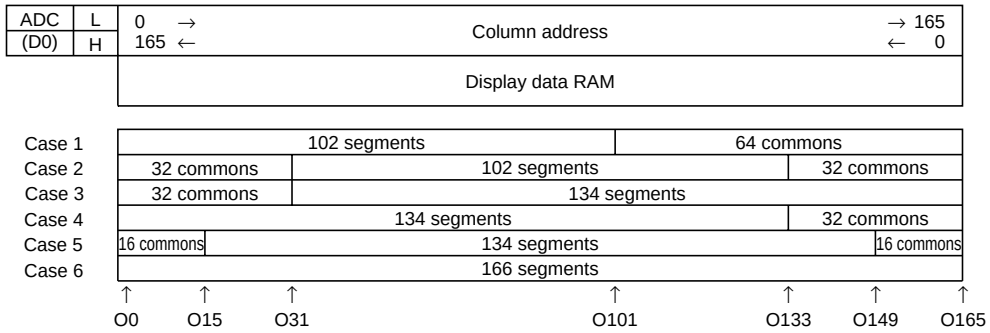


Figure 6. Output configuration selection

When COM outputs are assigned to the output drivers, the unused RAM area is not available. However, all RAM column addresses can still be accessed by the microprocessor.

Since duty setting and output selection are independent, the appropriate duty must be selected for each case. Cases 1 to 6 are determined according to the three lowest bits in the output status register in the output selection circuit. The COM output scanning direction can be selected by setting bit D3 in the output status register to "H" or "L".

Table 4

	SED1560		SED1561		SED1562
Duty	1/64	1/48	1/32	1/24	1/16
COM I function	COM64	COM48	COM32	COM24	COM16

When the DUTY + 1 command is executed, pin COM1 becomes as shown in Figure 4 irrelevant to output selection:

Since master/slave operation and the output selection circuit are completely independent in the SED1560 series, a chip either on the master or slave side can be allocated to the COM output function in multi-chip configuration.

The LCD driver outputs shown in Table 5 become ineffective when the SED1560 or SED1561 is used with 1/48 or 1/24 duty, respectively. In this case, ineffective outputs are used in the open state.

Table 5

		Output status register				Ineffective output
		D3	D2	D1	D0	
SED1560	Case 1	0	1	0	1	O150 to O165
		1	1	0	1	O102 to O117
	Case 2	0	1	0	0	O150 to O165
		1	1	0	0	O16 to O31
SED1561	Case 3	0	0	1	1	O0 to O7
		1	0	1	1	O23 to O31
	Case 4	0	0	1	0	O158 to O165
		1	0	1	0	O134 to O141
	Case 5	0	0	0	1	O158 to O165
		1	0	0	1	O8 to O15

SED1560 Output Status

The SED1560 selects any output status from Cases 1, 2 and 6.

1/64 duty (Display Area 64 × 102)

Case	Status register				LCD driver output																
	D3	D2	D1	D0	O0				O31	O32			O101	O102			O133	O134			O165
1	0	1	0	1	SEG102									COM0	→						COM63
	1	1	0	1	SEG102									COM63	←						COM0
2	0	1	0	0	COM31	←			COM0	SEG102								COM32	→		COM63
	1	1	0	0	COM32	→			COM63	SEG102								COM31	←		COM0
6	–	0	0	0	SEG166																

1/48 duty (Display Area 48 × 102)

Case	Status register				LCD driver output																
	D3	D2	D1	D0	O0				O31	O32			O101	O102			O133	O134			O165
1	0	1	0	1										COM0	→				COM47		
	1	1	0	1											COM47	←					COM0
2	0	1	0	0	COM31	←			COM0	SEG102								COM32	→47		
	1	1	0	0	COM32	→47				SEG102								COM31	←		COM0
6	–	0	0	0	SEG166																

SED1561 Output Status

The SED1561 selects any output status from Cases 3, 4, 5 and 6.

1/32 duty (Display Area 32 × 134)

Case	Status register				LCD driver output																
	D3	D2	D1	D0	O0			O15	O16			O31	O32				O133	O134		149	150	O165
3	0	0	1	1	COM31	←				COM0	SEG134											
	1	0	1	1	COM0	→				COM31	SEG134											
4	0	0	1	0	SEG134													COM0	→			COM31
	1	0	1	0	SEG134													COM31	←			COM0
5	0	0	0	1	15←COM0					SEG134												COM16→31
	1	0	0	1	COM16→31					SEG134												15←COM0
6	–	0	0	0	SEG166																	

1/24 duty (Display Area 24 × 134)

Case	Status register				LCD driver output																
	D3	D2	D1	D0	O0			O15	O16			O31	O32				O133	O134		149	150	O165
3	0	0	1	1		COM23	←			COM0	SEG134											
	1	0	1	1	COM0	→				COM23		SEG134										
4	0	0	1	0	SEG134													COM0	→			COM23
	1	0	1	0	SEG134														COM23	←		COM0
5	0	0	0	1	15←COM0					SEG134												16→23
	1	0	0	1	16→23					SEG134												15←COM0
6	–	0	0	0	SEG166																	

SED1562 Output Status

COM/SEG output status of the SED1562 is fixed.
1/16 duty (16 × 150)

LCD driver output			
00	0149	150	0165
SEG150		15 ◄—	COM0

Display Timers

Line counter and display data latch timing

The display clock, CL, provides the timing signals for the line counter and the display data latch. The RAM line address is generated synchronously using the display clock. The display data latch synchronizes the 166-bit display data with the display clock.
The timing of the LCD panel driver outputs is independent of the timing of the input data from the microprocessor.

FR and SYNC

The LCD AC signal, FR, and the synchronization signal, SYNC, are generated from the display clock. The FR controller generates the timing for the LCD panel driver outputs. Normally, 2-frame wave patterns are generated, but *n*-line inverse wave patterns can also be generated. These produce a high-quality display if *n* is based on the LCD panel being used.
SYNC synchronizes the timing of the line counter and common timers. It is also needed to synchronize the frame period and a 50% duty clock.

In a multiple-chip configuration, FR and SYNC are inputs. The SYNC signal from the master synchronizes the line counter and common timing of the slave.

Common timing signals

The internal common timing and the special-use common driver start signal, DYO, are generated from CL. As shown in figures 7 and 8, DYO outputs a HIGH-level pulse on the rising edge of the CL clock pulse that precedes a change on SYNC. DYO is generated by both the SED1560D0B, regardless of whether the device is in master or slave mode. However, when operating in slave mode, the device duty and the external SYNC signal must be the same as that of the master. In a multiple-chip configuration, FR and SYNC must be supplied to the slave from the master.

Table 6. Master and slave timing signal status

Part number	Mode	FR	SYNC	CLO	DYO
SD156✻D✻B	Master	Output	Output	CL output	Output
	Slave	Input	Input	High impedance	Output

2-frame AC driver waveform

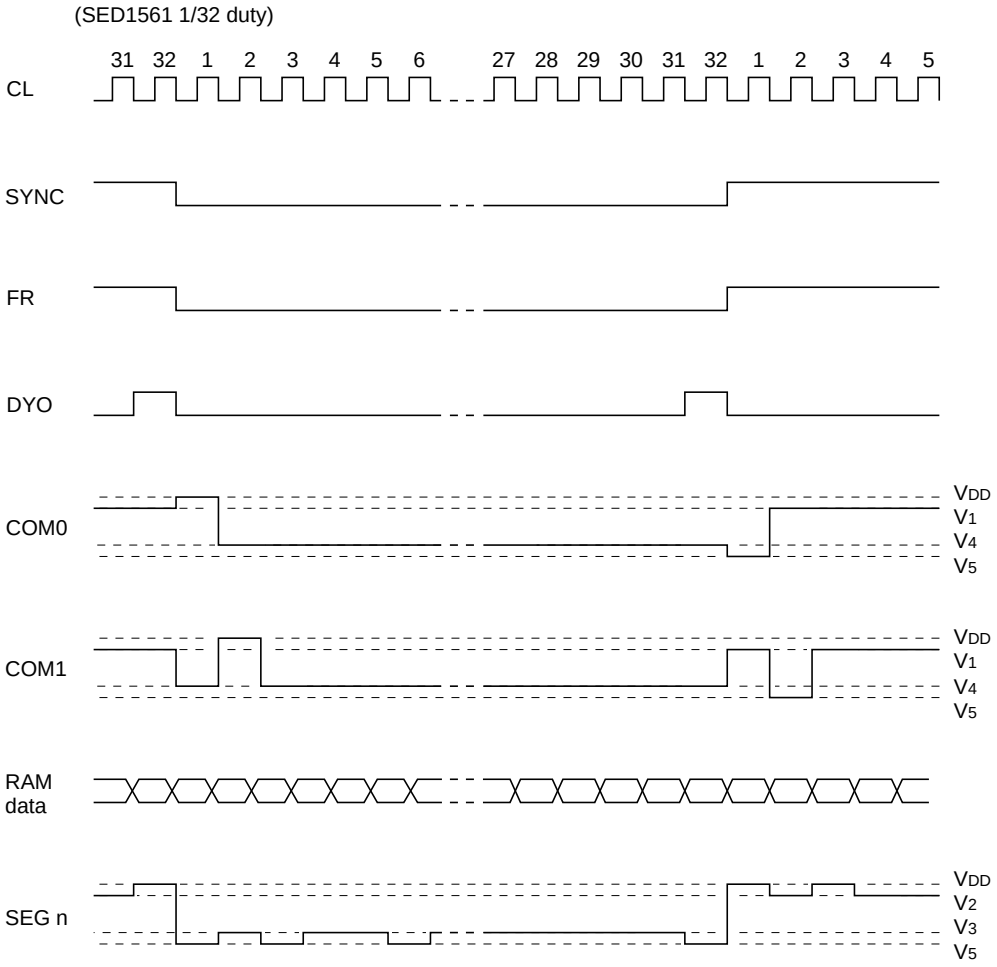


Figure 7. Frame driver timing

n line inverse driver waveform (n = 5, line inverse register 4)

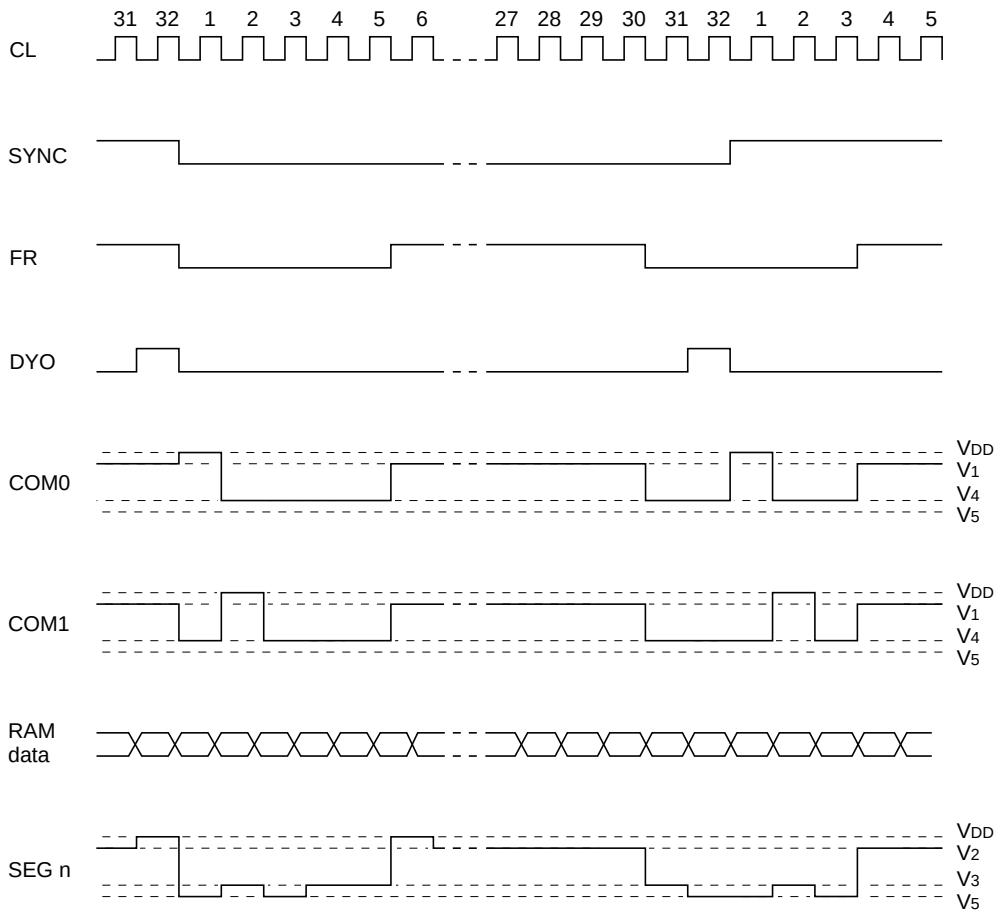


Figure 8. Line inverse driver timing

Note
When *n* = 5, the line inversion register is set to 4.

LCD Driver

The LCD driver converts RAM data into the 167 outputs that drive the LCD panel. There are 70 segment outputs, 96 segment or common dual outputs, and a COM1 output for the indicator display.

Two shift registers for the common/segment drivers are used to ensure that the common outputs are output in the correct sequence. The driver output voltages depend on the display data, the common scanning signal and FR.

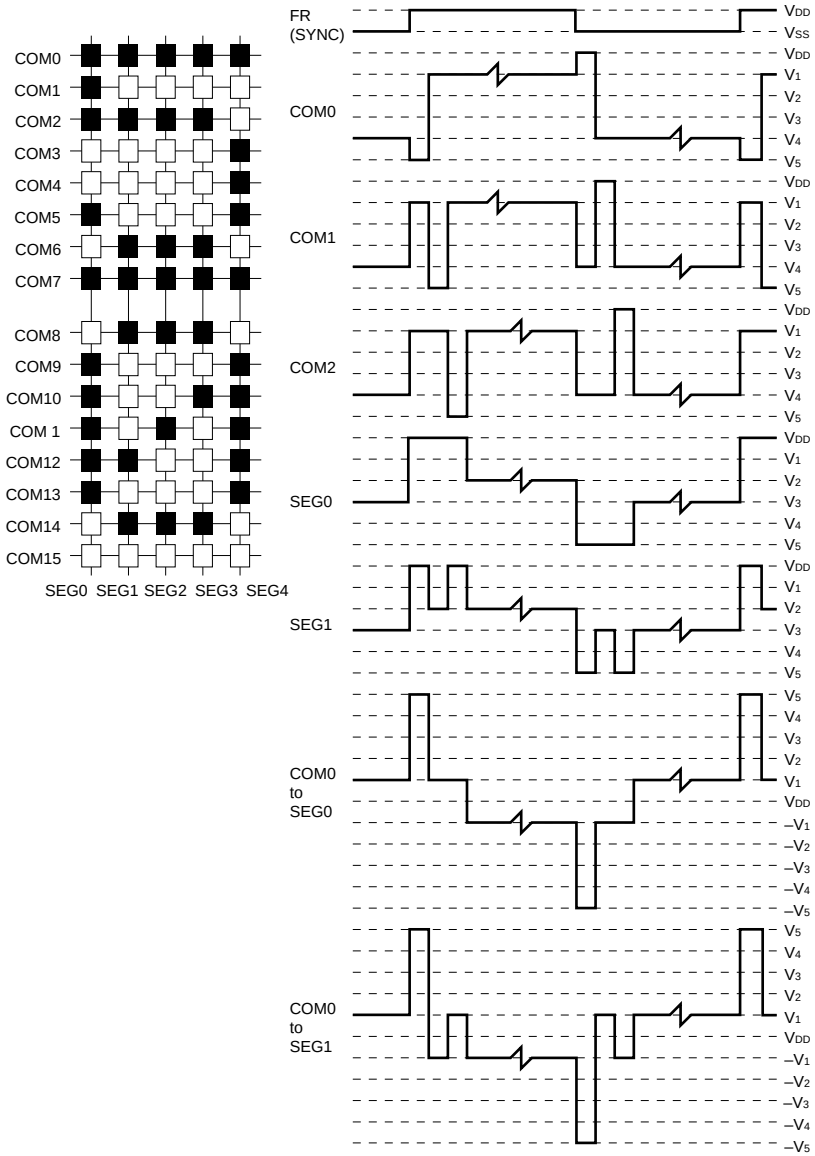


Figure 9. Example of segment and common timing

Display Data Latch Circuit

The display data latch circuit temporarily stores the output display data from the display data RAM to the LCD driver circuit in each common period. Since the Normal/Inverse Display, Display ON/OFF and Display All Points ON/OFF commands control the data in this latch, the data in the display data RAM is remains unchanged.

LCD Driver Circuit

This multiplexer generates 4-value levels for the LCD driver, having 167 outputs of 70 SEG outputs, 96 SEG/COM dual outputs and a COM output for the indicator display. The SEG/COM dual outputs have a shift register and sequentially transmits COM scanning signals. The LCD driver voltage is output according to the combination of display data, COM scanning signal and FR signal. Figure 9 shows a typical SEG/COM output waveform.

Oscillator Circuit

The low power consumption type CR oscillator adjusting the oscillator frequency by use of only oscillator resistor Rf is used as a display timing signal source or clock for the voltage raising circuit of the LCD power supply.
The oscillator circuit is only available in the master operation mode. When a signal from the oscillator circuit is used for display clock, fix the CL pin to the V_{SS} level. When the oscillator circuit is not used, fix the OSC1 or OSC2 pin to the V_{DD} or V_{SS} level, respectively.
The oscillator signal frequency is divided and output from the CLO pin as display clock. The frequency is divided to one-fourth, one-eighth or one-sixteenth in the SED1560, SED1561 or SED1562, respectively.

FR Control Circuit

The LCD driver voltage supplied to the LCD driver outputs is selected using FR signal.

Power Supply Circuit

This is a power circuit to produce voltage needed to drive liquid crystals at a low power consumption. This circuit is valid only when the SED156*D*B master is in operation. The power circuit consists of voltage tripler, voltage regulator and the voltage follower.
The power circuit built into SED1560*D*B is set for smaller scale liquid crystal panels and it is not too suitable when the picture element is larger or to drive a liquid crystal panel with lager indication capacity using multiple chips. With liquid crystal panels with a larger load capacity, the quality of display may become very bad. Use an external power in such cases. (If an external amp circuit is configured, we recommend to use the SCI7660 and SCI7661.)
The power circuit can be controlled by the built-in power ON/OFF command. When the built-in power is turned off, all of the boosting circuit, voltage regulation circuit and voltage follower circuit goes open. In this case, the liquid crystal driving voltage V_1, V_2, V_3, V_4 and V_5 should be supplied from outside and the terminals CAP1+, CAP1-, CAP2+, CAP2-, Vout and V_R should be kept opened.
If the built-in power supply is turned on, you must always enter this command after the wait time of the built-in power supply turn-on completion command.
Various functions of the power circuit may be selected by combinations of the setting of the T1 and T2. It is also possible to make a combined use of the external power

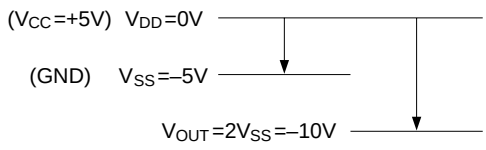
T1	T2	Voltage tripler	Voltage regulator	voltage follower	External voltage input	Voltage tripler terminals	V_R terminals
L	L	○	○	○	–		
L	H	○	○	○	–		
H	L	×	○	○	V_{OUT}	OPEN	
H	H	×	×	○	V_5	OPEN	OPEN

supply and a portion of the functions of the built-in power supply.
When (T1, T2) = (H, L), the boosting circuit does not work and open the boosting circuit terminals (CAP1+, CAP1-, CAP2+ and CAP2-) and apply liquid crystal driving voltage to the Vout terminals from outside.

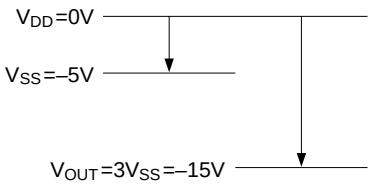
When (T1, T2) = (H. H), the boosting circuit and voltage regulation circuit do not work and open the boosting circuit terminals and the VR terminals and apply liquid crystal driving voltage connecting the V_5 terminals.

Voltage tripler

By connecting capacitors C1 between CAP1+ and CAP1-, CAP2+ and CAP2- and VSS-Vout, the electric potential between VDD-VSS is boosted to the triple toward negative side and outputted from the Vout terminal. When a double boosting is required, disconnect the capacitor between CAP2+ and CAP2- and short-circuit the CAP2- and Vout terminals to obtain output boosted to the double out of the Vout (or CAP2-) terminal.
Signals from the oscillation circuit are used in the boosting circuit and it then is necessary that the oscillation circuit is in operation.
Electric potentials by the boosting functions are given below.



Electric potentials of double boosting



Electric potentials of triple boosting

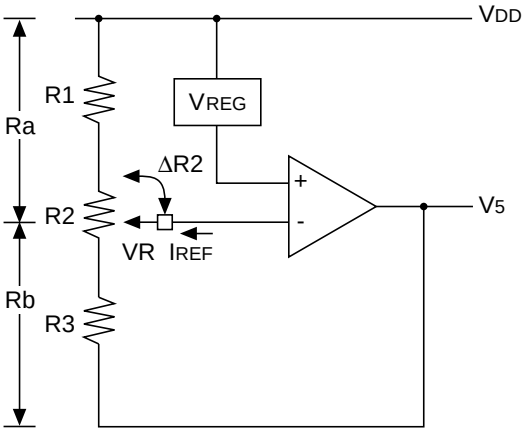
Voltage Regulator

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator, and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V_5| < |V_{OUT}|$.

$$V_5=\left(1+\frac{Rb}{Ra}\right) V_{REG}+I_{REF} \cdot Rb$$

$$=\left(1+\frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) V_{REG}$$

$$+I_{REF} \cdot (R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and it is constant and $V_{REG} \fallingdotseq -2.5 \pm 0.15$ V (if V_{DD} is 0 V). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3: (In case of Type 1)

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots\cdots\cdots \textcircled{1}$$

(As $I_{REF} = 0$ A)

- R1 + R2 + R3 = 5MΩ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 V_5 = –6 to –10 V
  (Determined by the LCD characteristics)
  ΔR2 = OΩ, V_{REG} = –2.55V
  To obtain V_5 = -10 V, from equation ①:
  R2 + R3 = 2.92 × R1 ..... ③
  ΔR2 = R2, V_{REG} = –2.55V
  To obtain V_5 = -6 V, from equation ①:
  1.35 × (R1 + R2) = R3 ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the VR pin has a high input impedance, the shielded and short lines must be protected from a noise interference.
In case of Type 2, similarly preset R1, R2 and R3 on the basis of $V_{REG} = V_{SS}$.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage. This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = (1 + \frac{Rb}{Ra})\, V_{REG} + Rb \times \Delta I_{REF} \quad \text{..... ⑤}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below.
Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.5V±0.15V } Type1
V_{REG} = –0.2%/˚C
V_{REG} = V_{SS} }Type2
V_{REG} = 0.00%/˚C
V_{REG} = –0.2%/°C
I_{REF} = –3.2µA±40% (For 16 levels)
I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)
0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

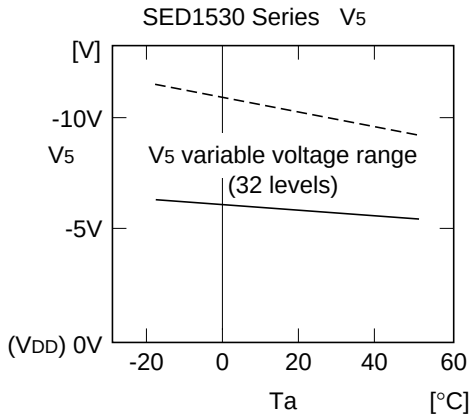
$$R3 = \frac{V_5 \text{ variable voltage range}}{|\, I_{REF} \,|} = \frac{4V}{6.5\mu A}$$

Rb = 625KΩ

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5 max}{V_{REG}} - 1} = \frac{625K\Omega}{\frac{-6V}{-2.55V} - 1}$$

Ra = 462KΩ



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (-2.55V)$
$= -6.0V$
$V_5min = V_5 max + Rb \times I_{REF}$
$= -6V + 625k \times (-6.5\mu A)$
$= -10.0V$

Ta=–10°C

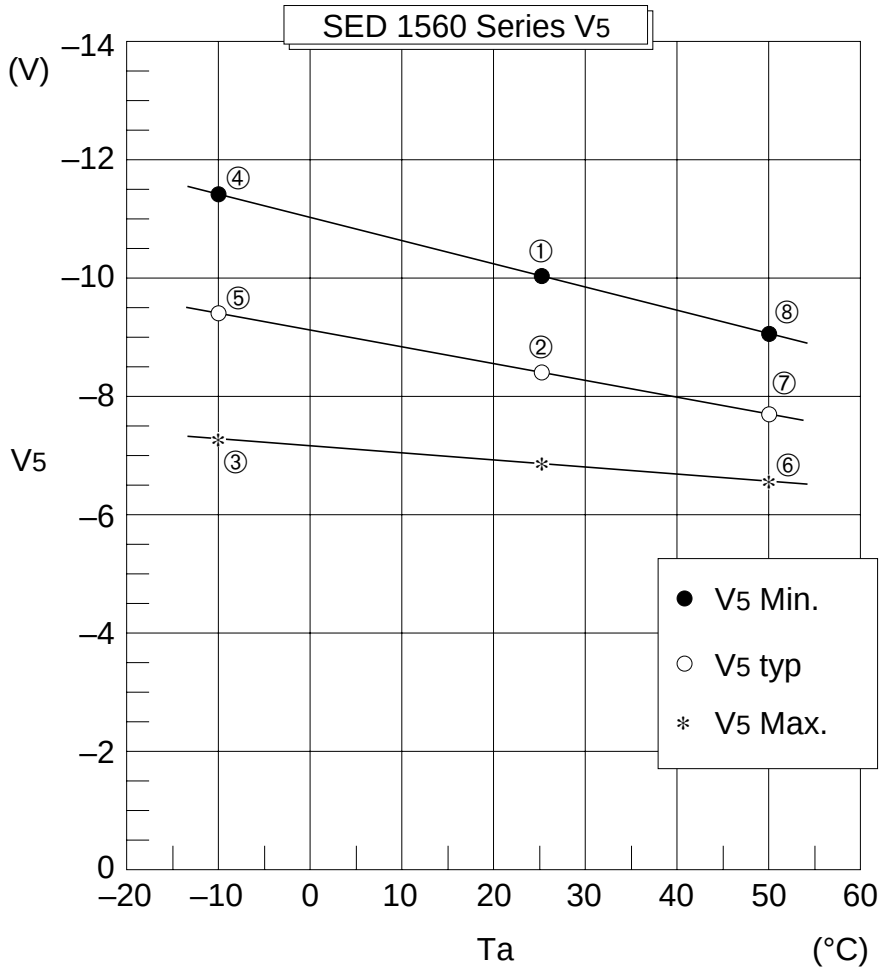
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (-10°C-25°C)\}$
$= -6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= -6.42V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times$
$(-10°C-25°C)\}$
$= -11.63V$

Ta=–50°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (50°C-25°C)\}$
$= -5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= -5.7V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times$
$(50°C-25°C)\}$
$= -8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.
In case of Type 2, it so becomes that $V_{REG} = V_{SS}$ (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

Example of V_5 Voltage When Using SED1560 Series Electronic Volume



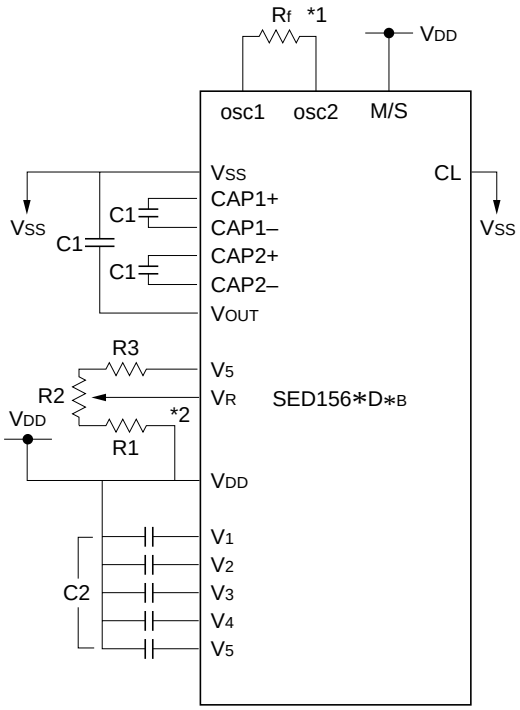
Liquid Crystal Voltage Generating Circuit

A V_5 potential is resistively divided within the IC to cause V_1, V_2, V_3 and V_4 potentials needed for driving of liquid crystals. The V_1, V_2, V_3 and V_4 potentials are further converted in the impedance by the voltage follower before supplied to the liquid crystal driving circuit. The liquid crystal driving voltage is fixed with each type.

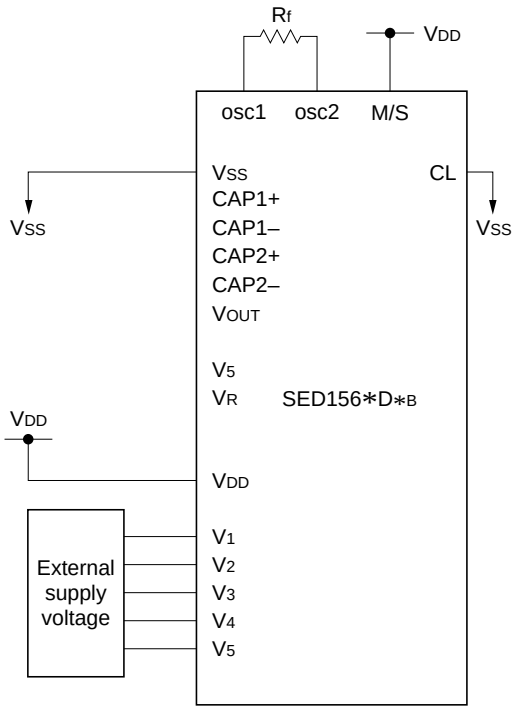
types	Liquid crystal driving voltage
SED1560D0B	1/9 bias voltage
SED1560DAB	1/7 bias voltage
SED1561D0B	1/7 bias voltage
SED1561DAB	1/5 bias voltage
SED1562D0B	1/5 bias voltage

As shown in Fig. 8, it needs to connect, externally voltage stabilizing capacitors C2 to the liquid crystal power terminals. When selecting such capacitor C2 make actual liquid crystal displays matching to the display capacity of the liquid crystal display panel, before determining on the capacitance as the constant value for voltage stabilization.

When the built-in power circuit is used



When the built-in power circuit is not used



Reference set values:

SED1560 V_5 ≒ –11~–13 V
SED1561 V_5 ≒ –7~ –9 V
SED1562 V_5 ≒ –5~ –7 V (Variable)

	SED1560	SED1561	SED1562
C1	4.7 µF	2.2 to 4.7 µF	2.2 to 4.7 µF
C2	0.1 to 0.47 µF	0.1 to 0.47 µF	0.1 µF
R1	1 MΩ	700 KΩ	500 KΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	4 MΩ	1.6 MΩ	700 KΩ
LCD SIZE	32×51 mm	16×67 mm	8×75 mm
DOT	64×102	32×134	16×150

*1 Connect oscillator feedback resistor Rf as short as possible and place it close to the IC for preventing a malfunction.

*2 Use short wiring or shielded cables for the VR pin due to high input impedance.

*3 Determine C1, C2 depending on the size of LCD panel driven. You must set these values so that the LCD driving voltage becomes stable. Set (T1, T2)=(H, L) and supply an external voltage to VOUT. Display the LCD heavy load pattern and determine C2 so that the LCD driving voltages (V1 to V5) become stable. Then, set (T1, T2)=(L, L) and determine C1.
Set the same capacitance for C2.

*4 The "LCD SIZE" indicates the vertical and horizontal length of the LCD panel display area.

Reset

When power is turned ON, the SED1560 is initialized on the rising edge of $\overline{RES}$. Initial settings are as follows.

1. Display : OFF
2. Display mode : Normal
3. *n*-line inversion : OFF
4. Duty cycle : 1/64 (SED1560)
   1/32 (SED1561)
5. ADC select : Normal (D0 = L)
6. Read/write modify : OFF
7. Internal power supply : OFF
8. Serial interface register data : Cleared
9. Display initial line register : Line 1
10. Column address counter : 0
11. Page address register : Page 0
12. Output selection circuit : Case 6
13. *n*-line inversion register : 16
14. Set the electronic control register to zero (0).

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 µs to correctly reset the SED1560. Normal operation starts 1 µs after the rising edge on $\overline{RES}$.

If the built-in LCD power circuit of the SED156✻D✻B is not used, the $\overline{RES}$ signal must be low when the external LCD power supply is turned on. When the $\overline{RES}$ goes low, each register is cleared to the above listed initial status. However, the oscillation circuit and output pins (OSC2, FR, SYNC, CLD, DYO, D0 to D7 pins) are not affected.

If the SED1560 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

Although SED1560 Series devices maintain the operation status under commands, when external noise of excessive levels enters, their internal statys may be changed. Consequently, it is necessary to provide means to suppress noise occurring from package or the system or orovide means to avoid influence of such noise.

Also, to cope with sudden noise, we suggest you to set up the software so the operation status can be periodically refreshed.

When the Reset command is used, only initial settings 9 to 14 are active.

COMMANDS

The Command Set

A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed.

For the 80-series MPU interface, the command is activated when a low pulse is entered in the $\overline{RD}$ pin during read or when a low pulse is entered in the $\overline{WR}$ pin during write. While the 68-series MPU interface is set to the read status when a high pulse is entered in the R/$\overline{W}$ pin, and it is set to the write status when a low pulse is entered in this pin. The command is activated when a high pulse is entered in the E pin. (For their timings, see Section 10 "Timing Characteristics.") Therefore, the 68-series MPU interface differs from the 80-series MPU interface in the point where the $\overline{RD}$ (or E) signal is 1 (or high) during status read and during display data read explained in the command description and on the command table. The following command description uses an 80-series MPU interface example.

If the serial interface is selected, data is sequentially entered from D7.

Table 7. SED1560 series command table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LCD display ON and OFF 0 : OFF 1 : ON
Display START Line set	0	1	0	0	1	Dispaly start address						Determines the RAM display line for COM 0
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register.
Column address set; high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high-order 4 bits of the display RAM column address in the register.
Column address set; low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RAM column address in the register.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Status read	0	0	1	Status				0	0	0	0	Reads the status information.
Display data write	1	1	0	Write Data								Writes data in the display RAM.
Display data read	1	0	1	Read Data								Reads data from the display RAM.
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Outputs the display RAM address for SEG. 0: Normal 1: Reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Displays the LCD image in normal or reverse mode. 0: Normal 1: Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all indicators. 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0:1/24, 48 1:1/32, 64
Duty +1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0: Normal 1: Duty+1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed n-lines				Sets the line reverse driving and No. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.
Read Modify write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address counter, and set to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indictors.

Commands

Display ON/OFF

Alternatively turns the display ON and OFF.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	1	1	D

Note
D = 0 Display OFF
D = 1 Display ON

Initial Display Line

Loads the RAM line address of the initial display line, COM0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
↓						↓
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Page Address Set

Loads the RAM page address from the microprocessor into the page address register. A page address, along with a column address, defines a RAM location for writing or reading display data. When the page address is changed, the display status is not affected.
Page address 8 is a special use RAM area for the indicator. Only D0 is available for data exchange.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

Column Address Set

Loads the RAM column address from the microprocessor into the column address register. The column address is divided into two parts-4 high-order bits and 4 low-order bits.
When the microprocessor reads or writes display data to or from RAM, column addresses are automatically incremented, starting with the address stored in the column address register and ending with address 166. The page address is not incremented automatically.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	1	A7	A6	A5	A4

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
↓								↓
1	0	1	0	0	1	0	1	165

Read status

Indicates to the microprocessor the four SED1560 status conditions.

A_0	$\overline{E}$ / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	Busy	ADC	ON/ OFF	RES- ET	0	0	0	0

BUSY Indicates whether or not the SED1560 will accept a command. If BUSY is 1, the device is currently executing a command or is resetting, and no new commands can be accepted. If BUSY is 0, a new command can be accepted. It is not necessary for the microprocessor to check the status of this bit if enough time is allowed for the last cycle to be completed.

ADC Indicates the relationship between RAM column addresses and the segment drivers. If ADC is 1, the relationship is normal and column address *n* corresponds to segment driver *n*. If ADC is 0, the relationship is inverted and column address (165 – *n*) corresponds to segment driver *n*.

ON/OFF Indicates whether the display is ON or OFF. If ON/OFF is 1, the display is OFF. If ON/OFF is 0, the display is ON. Note that this is the opposite of the Display ON/OFF command.

RESET Indicates when initialization is in process as the result of RES or the Reset command.

Write Display Data

Writes bytes of display data from the microprocessor to the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continuously write data to the addressed page.

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/W)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	Write data							

Read Display Data

Sends bytes of display data to the microprocessor from the RAM location specified by the column address and page address registers. The column address is incremented automatically so that the microprocessor can continously read data from the addressed page. A dummy read is required after loading an address into the column address register.

Display data cannot be read through the serial interface.

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/W)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Read data							

Select ADC

Selects the relationship between the RAM column addresses and the segment drivers. When reading or writing display data, the column address is incremented as shown in figure 4.

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/W)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	0	0	D

Note
D = 0 Rotate right (normal direction)
D = 1 Rotate left (reverse direction)

The output pin relationship can also be changed by the microprocessor. There are very few restrictions on pin assignments when constructing an LCD module.

Normal/Inverse Display

Determines whether the data in RAM is displayed normally or inverted.

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/W)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	1	D

Note
D = 0 LCD segment is ON when RAM data is 1 (normal).
D = 1 LCD segment is ON when RAM data is 0 (inverse).

Display All Points ON/OFF

Turns all LCD points ON independently of the display data in RAM. The RAM contents are not changed. This command has priority over the normal/inverse display command.

A_0	$\overline{RD}$ (E)	$\overline{WR}$ (R/W)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	0	1	0	D

Note
D = 0 Normal display status
D = 1 All display segments ON

If this command is received when the display status is OFF, the Power Save command is executed.

Select Duty

Selects the LCD driver duty.
Since this is independent from contents of the output status register, the duty must be selected according to the LCD output status.
In multi-chip configuration, the master and slave devices must have the same duty.

A_0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	0	0	D

Model	D	Duty
SED1560	0 1	1/48 1/64
SED1561	0 1	1/24 1/32
SED1562	0 1	1/16 1/16

Duty + 1

Increases the duty by 1. If 1/48 or 1/64 duty is selected in the SED1560 for example, 1/49 or 1/65 is set, respectively and COM1 functions as either the COM48 or COM64 output. The display line always accesses the RAM area corresponding to page address 8, D0. (Refer to Figure 4.)
In multi-chip configuration, the Duty + 1 command must be executed to both the master and slave sides.

A_0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	0	1	0	1	D

Model	D	Duty
SED1560	0 1	1/48 or 1/64 1/49 or 1/65
SED1561	0 1	1/24 or 1/32 1/25 or 1/33
SED1562	0 1	1/16 1/17

Set *n*-lineE Inversion

Selects the number of inverse lines for the LCD AC controller. The value of *n* is set between 2 to 16 and is stored in the *n*-line inversion register.

A_0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Number of inverted lines
0	0	0	0	–
0	0	0	1	2
0	0	1	0	3
↓				↓
1	1	1	0	15
1	1	1	1	16

Do not use this command when using the votage follower of the built-in power supply, the characteristics of the built-in power supply cannot then be guaranteed to stay within the specification.

Cancel *n*-line Inversion

Cancels *n*-line inversion and restores the normal 2-frame AC control. The contents of the *n*-line inversion register are not changed.

A_0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	1	0	0	0	0	0

Modify Read

Following this command, the column address is no longer incremented automatically by a Read Display Data command. The column address is still incremented by the Write Display Data command. This mode is cancelled by the End command. The column address is then returned to its value prior to the Modify Read command. This command makes it easy to manage the duplication of data from a particular display area for features such as cursor blinking.

A_0	$\overline{E}$ $\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	1	0	0	0	0	0

Note that the Column Address Set command cannot be used in modify-read mode.

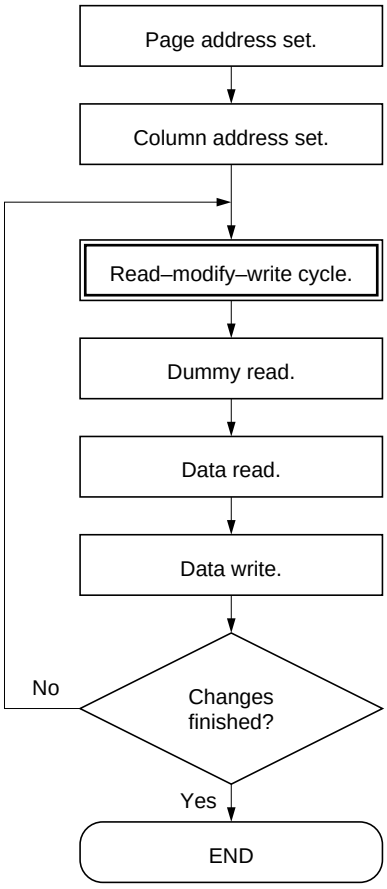


Figure 13. Command sequence for cursor blinking

End

Cancels the modify read mode. The column address prior to the Modify Read command is restored.

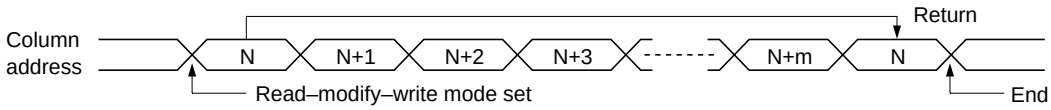
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

Resets the initial display line, column address, page address, and *n*-line inversion registers to their initial values. This command does not affect the display data in RAM.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset command does not initialize the LCD power supply. Only RES can be used to initialize the supplies.



Output Status Register

Available only in the SED1560 and SED1561.
This command selects the role of the COM/SEG dual pins and determines the LCD driver output status.
The COM output scanning direction can be selected by setting A3 to "H" or "L". For details, refer to the Output Status Circuit in each function description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	A3	A2	A1	A0

A3: Selection of the COM output scanning direction

A_2 A_1 A_0	Output Status	Number of COM/SEG Output pins	Remarks
0 0 0	Case 6	SEG 166	Applies to the SED1560/61
0 0 1	Case 5	SEG 134, COM 32	Applies to the SED1561
0 1 0	Case 4	SEG 134, COM 32	
0 1 1	Case 3	SEG 134, COM 32	
1 0 0	Case 2	SEG 102, COM 64	Applies to the SED1560
1 0 1	Case 1	SEG 102, COM 64	
1 1 0	Case 6	SEG 166	Applies to the SED1560/61
1 1 1	Case 6	SEG 166	

LCD Power Supply ON/OFF

Turns the SED156∗D∗B internal LCD power supply ON or OFF. When the power supply is ON, the voltage converter, the voltage regulator circuit and the voltage followers are operating. For the converter to function, the oscillator must also be operating.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0

Note
D = 0 Supply OFF
D = 1 Supply ON

When an external power supply is used with the SED156∗D∗B, the internal supply must be OFF.
If the SED156∗D∗B is used in a multiple-chip configuration, an external power supply that meets the specifications of the LCD panel must be used. An SED1560 operating as a slave must have its internal power supply turned OFF.

Completion of Built-in Power On

This command turns on the built-in power supply.

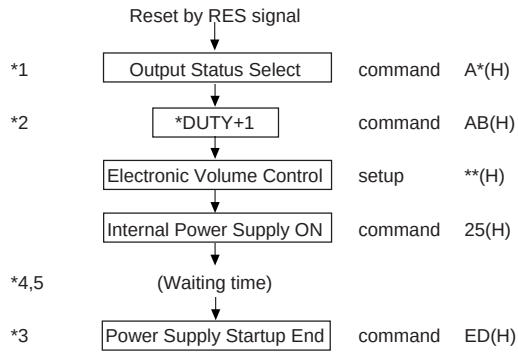
A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	0	1

The SED1560 series has the built-in, low-power LCD driving voltage generator circuit which can cut almost all currents except those required for LCD display. This is the primary advantage of the SED1560 series product. However, it has the low power and you need perform the following power-on sequence when turning on the built-in power supply:

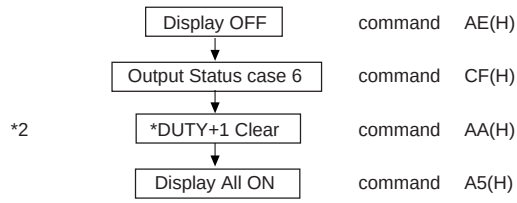
Sequence in the Built-in Power supply ON/OFF Status

To turn on built-in power supply, execute the above built-in power supply ON sequence. To turn off internal power supply execute the power save sequence as shown in the following power supply OFF status. Accordingly, to turn on built-in power supply again after turn it off (power save), execute the "Power Save Clear Sequence" that will be described afterwards.

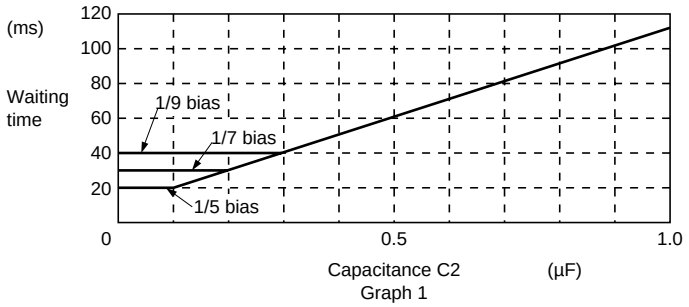
Built-in power supply ON status



Built-in power supply OFF status



*1: Regarding the SED 1562, it is not necessary to execute a command to decide an output status.
*2: When the COMI pin is not used, it is not necessary to enter the DUTY+1 and DUTY+1 Clear commands.
*3: When the built-in power supply startup end command is not executed, current is consumed stationarily.
Built-in power supply startup end command must always be used in a pair with built-in power supply ON command.
*4: The waiting time depends on the externally-installed capacitance C2 (refer to 4-35). After the waiting time shown in Graph 1, the power supply can be started surely.



Graph 1

V5 voltage conditions
1/9 bias V5 = –6.0 to –16.0 V
1/7 bias V5 = –5.0 to –12.0 V
1/5 bias V5 = –4.5 to –8.0 V

*5: Within the waiting time in built-in power supply ON status, any command other than built-in power supply control commands such as Power Save, and display ON/OFF command, display normal rotation/reverse command, display all ON command, output status select command and DUTY+1 clear command can accept another command without any problem. RAM read and write operations can be freely performed.

Electronic Volume Control Register

Through these commands, the liquid crystal driving voltage V5 being outputted from the voltage regulation circuit of the built-in liquid crystal power supply, in order to adjust the contrast of the liquid crystal display.
By setting data to the 4 bit register, one of the 16 voltage status may be selected for the liquid crystal driving voltage V5. External resistors are used for setting the voltage regulation range of the V5. For details refer to the paragraph of the voltage regulation circuit in the Clause for the explanation of functions.

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	A5	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	| V5 |
0	0	0	0	0	Small (as the absolute value)
		:			
1	1	1	1	1	Large (as the absolute value)

When not using the electronic volume control function, set to (0, 0, 0, 0, 0).

Power Save (Complex Command)

If the Display All Points ON command is specified in the display OFF state, the system enters the power save status, reducing the power consumption to approximate the static power consumption value. The internal state in the power save status is as follows:

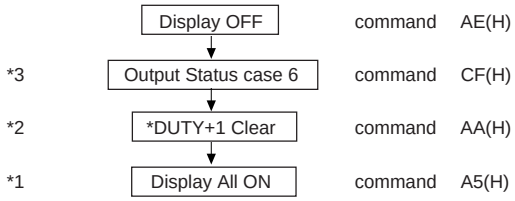
(a) The oscillator and power supply circuits are stopped.
(b) The LCD driver is stopped and segment and common driver outputs output the VDD level.
(c) An input of an external clock is inhibited and OSC2 enters the high-impedance state.
(d) The display data and operation mode before execution of the power save command are held.
(e) All LCD driver voltages are fixed to the VDD level.

The power save mode is cancelled by entering either the Display ON command or the Display All Points OFF command (display operation state). When external voltage driver resistors are used to supply the LCD driver voltage level, the current through them must be cut off by the power save signal.
If an external power supply is used, it must be turned OFF using the power save signal in the same manner and voltage levels must be fixed to the floating or VDD level.

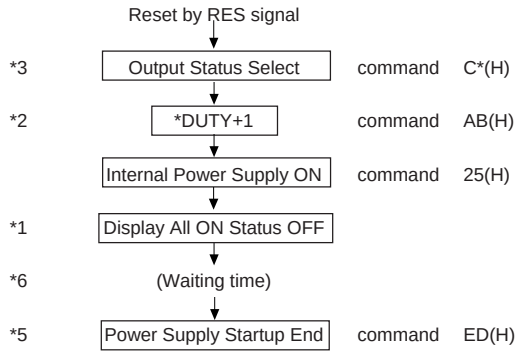
Sequence in the Power Save Status

Power Save and Power Save Clear must be executed according to the following sequence.
To give a liquid crystal driving voltage level by the externally-installed resistance dividing circuit, the current flowing in this resistance must be cut before or concurrently with putting the SED1560 series into the power save status so that it may be fixed to the floating or VDD level.
When using an external power supply, likewise, its function must be stopped before or concurrently with putting the SED1560 series ino the power save status so that it may be fixed to the floating or VDD level. In a configurationinwhich an exclusive common driver such as SED1630 is combined with the SED1560 series, it is necessary to stop the external power supply function after putting all the common output into non-selection level.

Power save sequence



Power save clear sequence



*1: In the power save sequence, the power save status is provided after the display all ON command. In the power save clear sequence, the power save status is cleared after the display all ON status OFF command.

*2 When the COMI pin is not used, it is not necessary to eneter the DUTY+1 command and DUTY+1 clear command.

*3 In the SED1562, it is not necessary to execute a command to decide an output status.

*4 The display ON command can be executed anywhere if it is later than the display all ON status OFF command.

*5 When internal power supply startup end command is not executed, current is consumed stationarily. Internal power supply startup end command must always be used in a pair with internal power supply ON command.

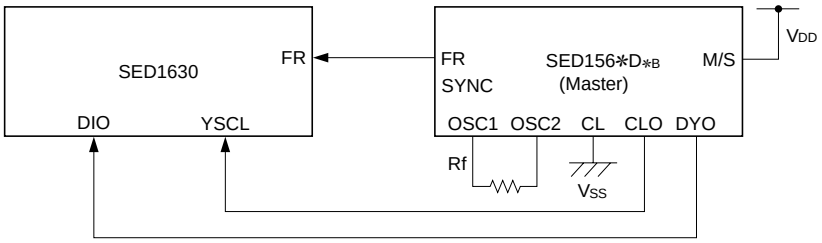
*6 The waiting time depends on the Externally-installed capacitance C2 (refer to 4-35). After the waiting time shown in the above Graph 1, the power supply can be started surely.

Connection between LCD drivers

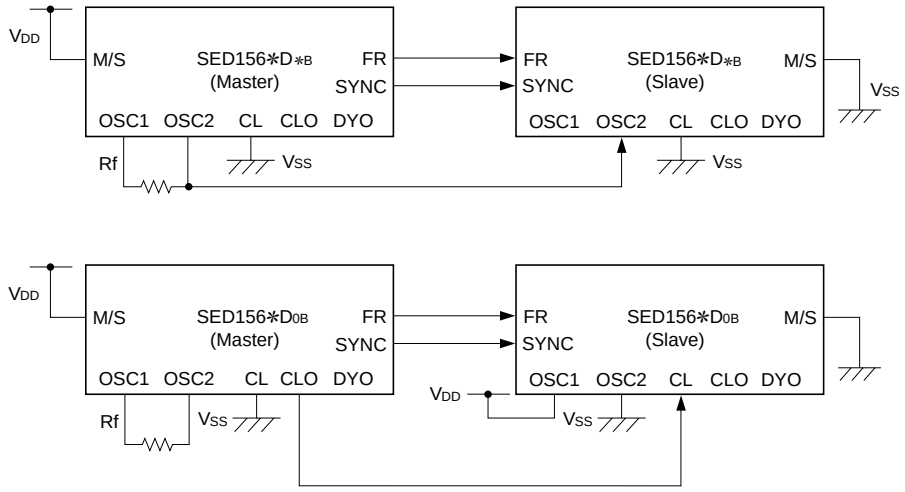
The LCD display area can be increased by using the SED1560 series in a multiple-chip configuration or with

Application with external Driver

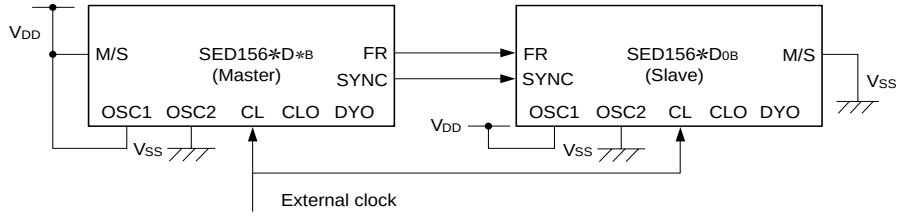
SED156*D*B–SED1630



SED156✻D✻B–SED156✻D✻B
(when oscillator circuit is used)



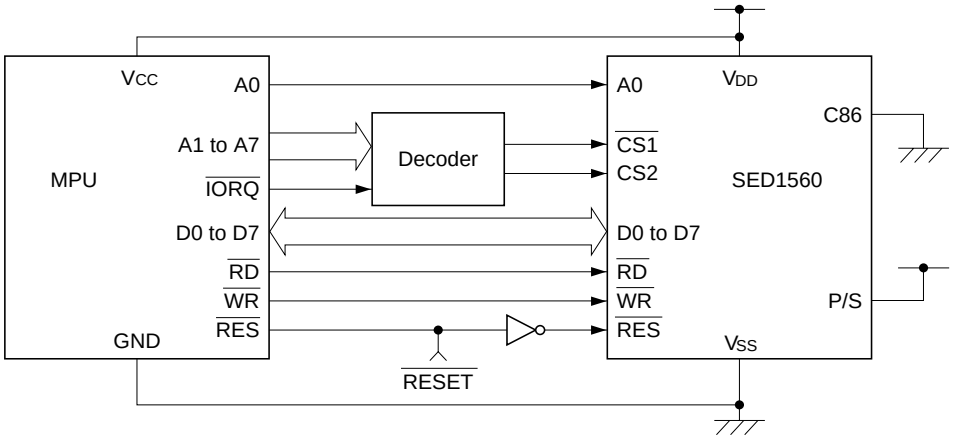
SED156✻D✻B–SED156✻D✻B (External clock)



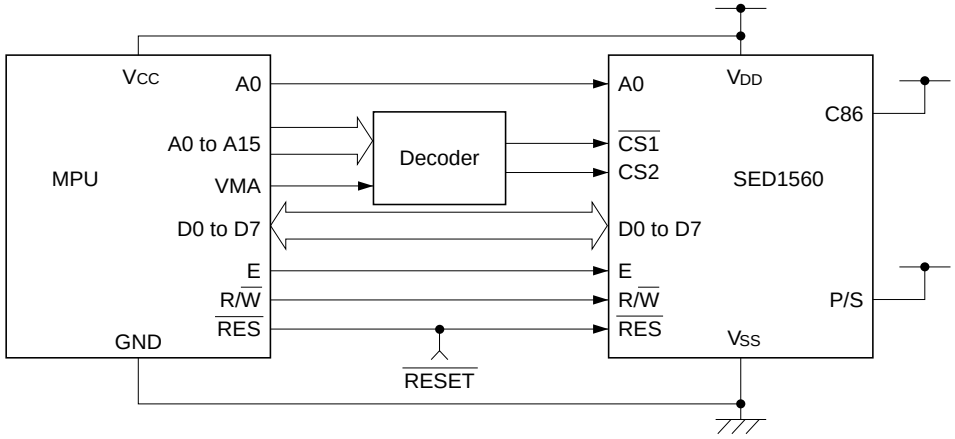
Microprocessor Interface

The SED1560 series interfaces to either 8080- or 6800-series microprocessors. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the SED1560 is controlled by the chip select signals from the microprocessor.

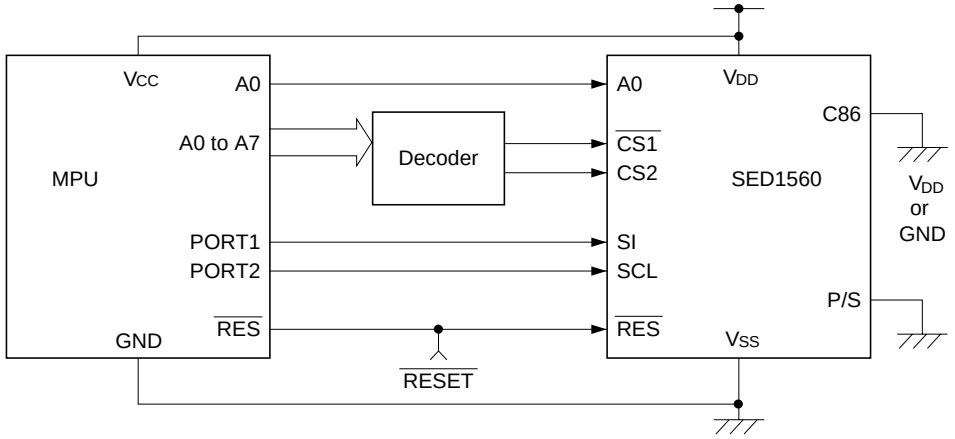
8080-series microprocessors



6800-series microprocessors

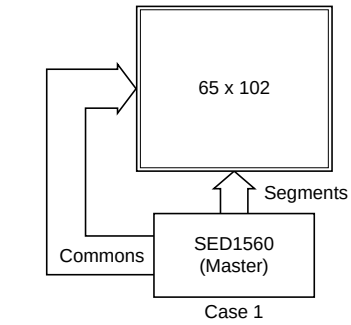


Serial interface

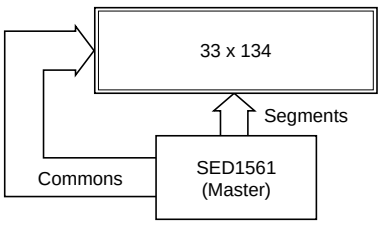


LCD Panel Interface Examples

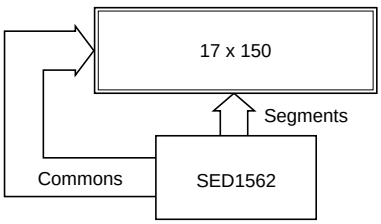
Single-chip configurations



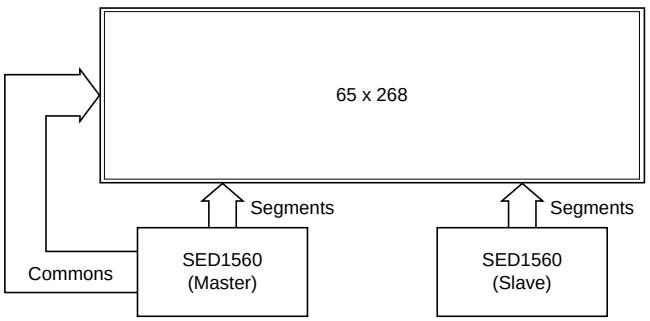
Case 1



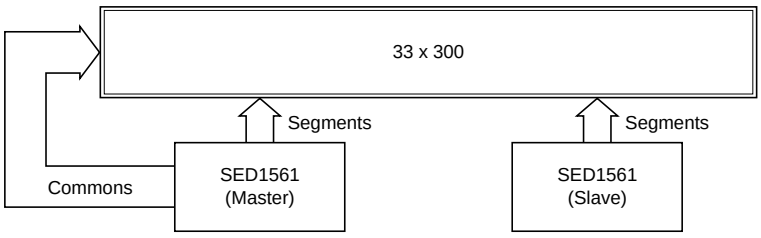
Case 4



Multiple-chip configurations

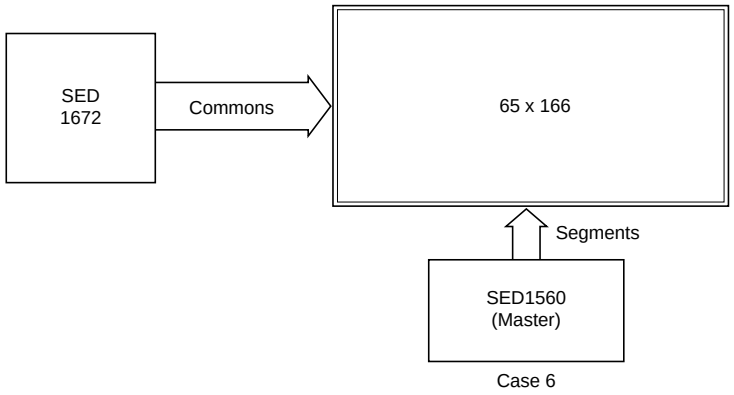


Case 1 Case 6



Case 4 Case 6

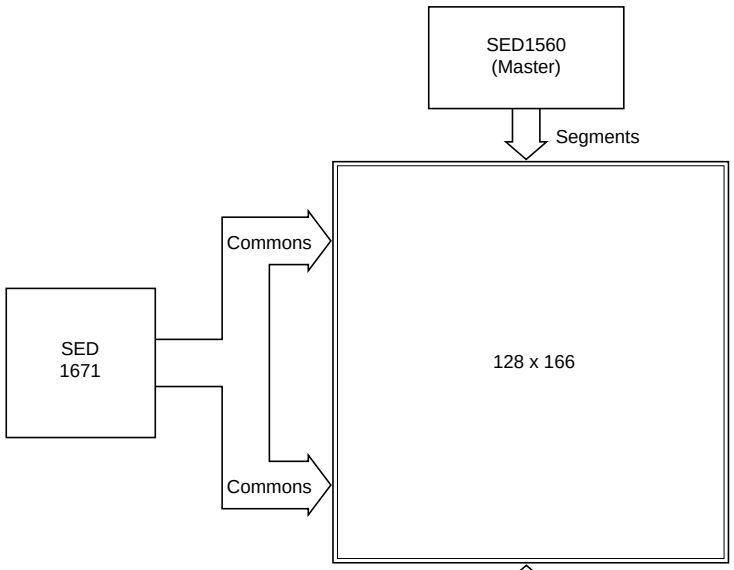
Special Common Driver Configurations



Case 6

* If an external amp circuit is configured, we recommend to use the SCI7660 and SCI7661.

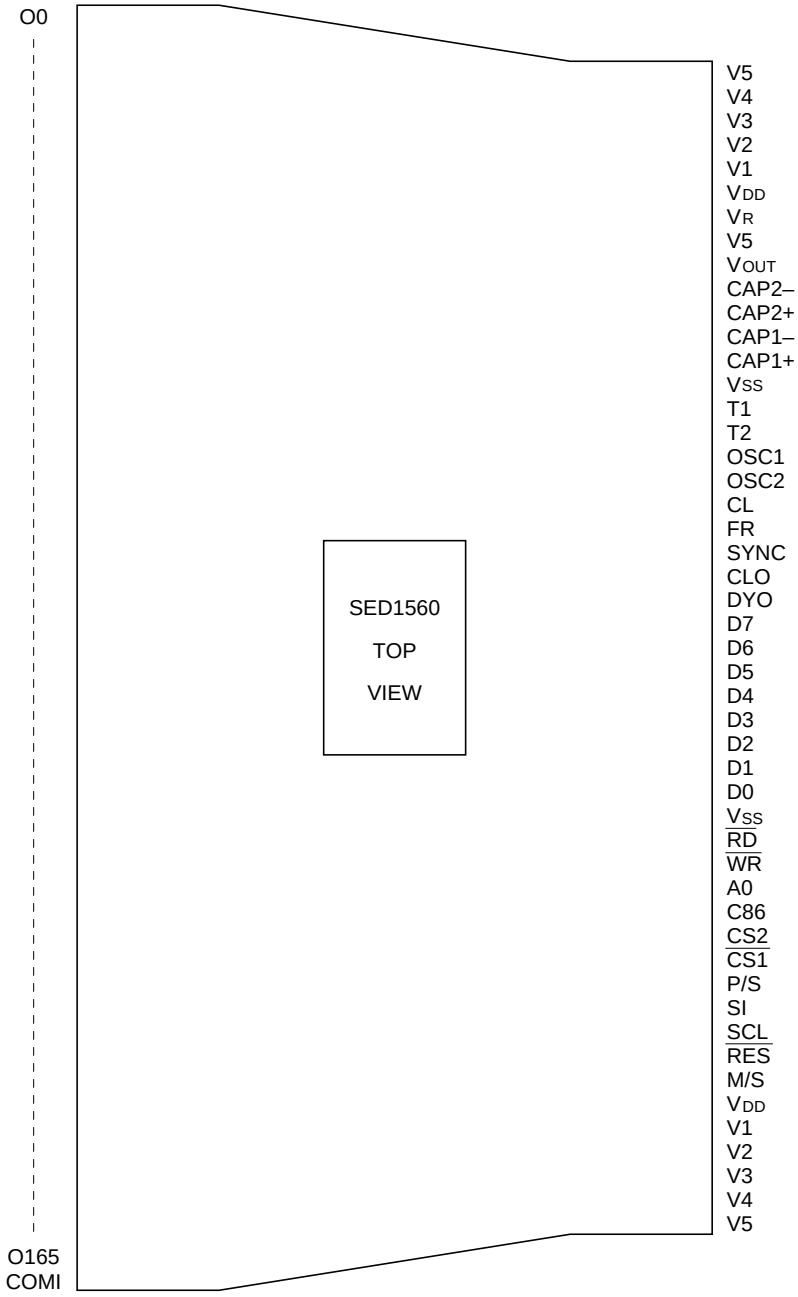
Case 6



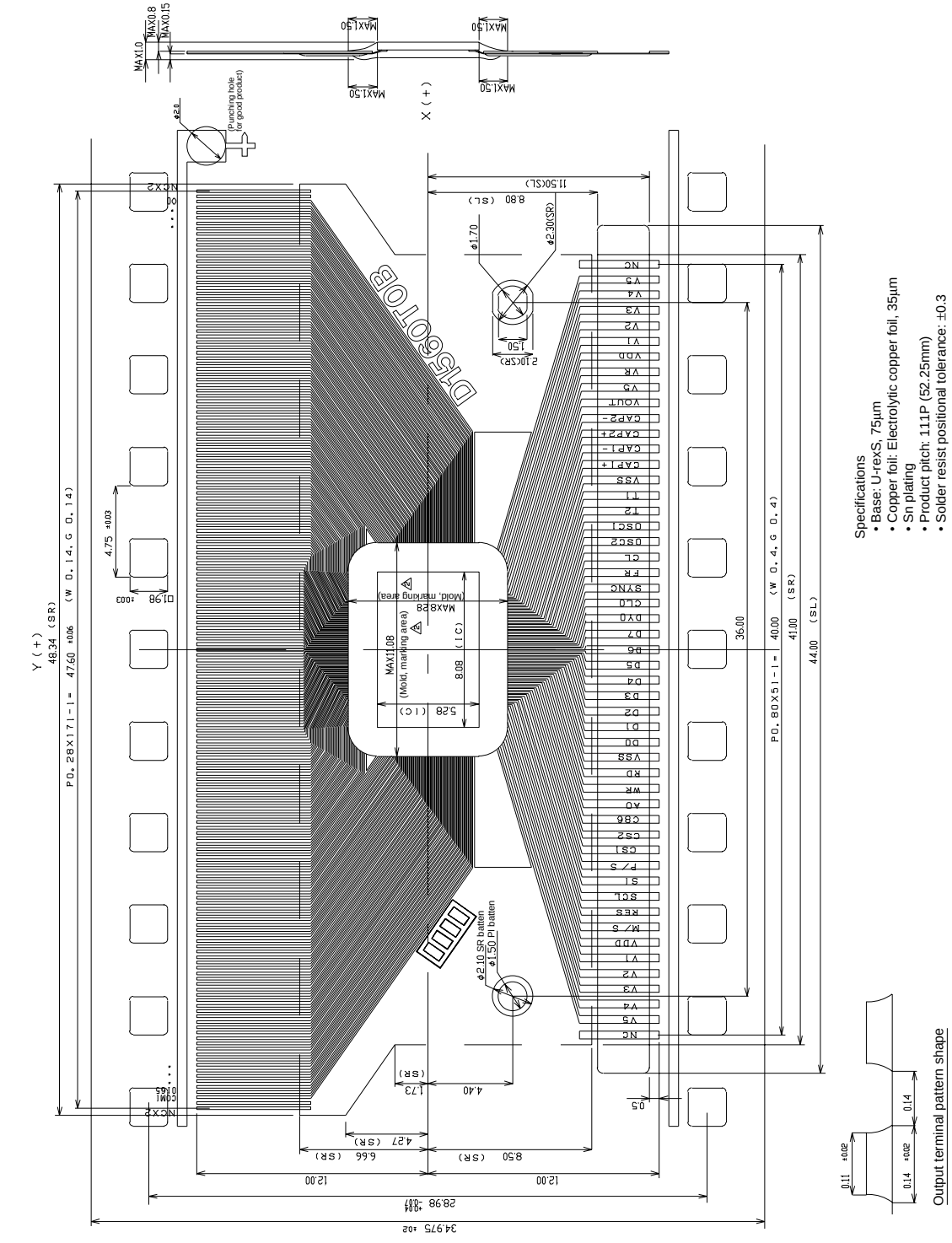
Case 6

SED1560T TAB Pin Layout

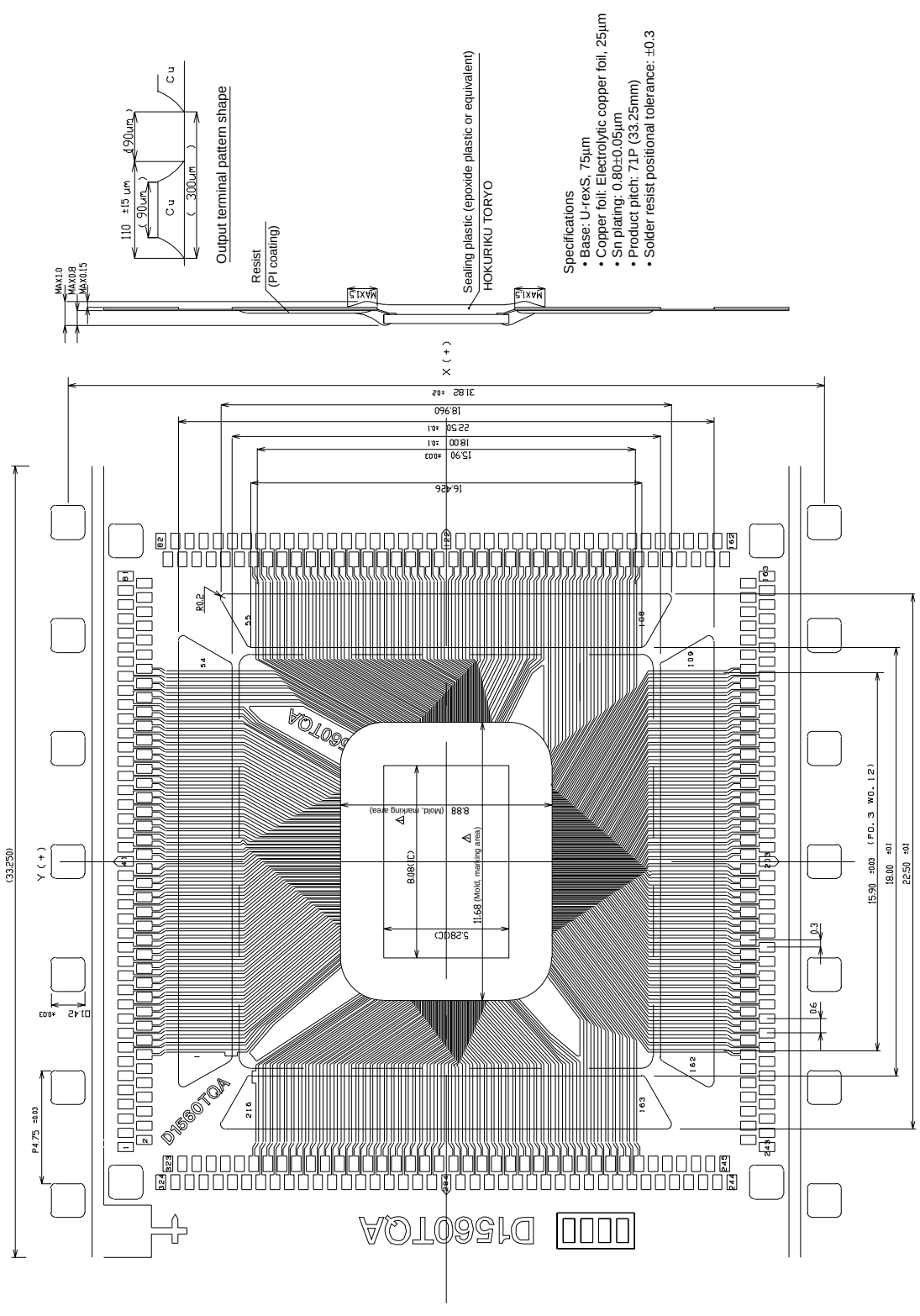
This drawing is not for specifying the TAB outline shape.



TCP DIMENSIONS (2 ways)



TCP DIMENSIONS (4 ways)



8. SED1565 Series

(Rev. 1.2)

Contents

GENERAL DESCRIPTION

The SED1565 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the SED1565 Series contain 65 × 132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The SED1565 Series chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65 × 132 dot display (capable of displaying 8 columns × 4 rows of a 16 × 16 dot kanji font). The SED1567 Series chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33 × 132 dot display (capable of displaying 8 columns × 2 rows of 16 × 16 dot kanji fonts). Thanks to the built-in 55 common output circuits and 132 segment output circuits, the SED1568*** is capable of displaying 55 × 132 dots (11 columns × 4 lines using 11 × 12 dots Kanji font) with a single chip. The SED1569 Series chips contain 53 common output circuits and 132 segment output circuits, so that a single chip can drive 53 × 132 dot display (capable of displaying 11 columns × 4 rows of 11 × 12 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the SED1565 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity
  65 × 132 = 8580 bits
- Display driver circuits
  SED1565***: 65 common output and 132 segment outputs
  SED1566***: 49 common output and 132 segment outputs
  SED1567***: 33 common outputs and 132 segment outputs
  SED1568***: 55 common outputs and 132 segment outputs
  SED1569***: 53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C or –0.2%/°C or external input)
  V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)
  SED1565D0B 81 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Quad voltage, $V_5 – V_{DD}$ = –11.0 V)
  SED1566D0B 43 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1567D0B 29 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1568D0B/SED1569D0B 46μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  Conditions: When all displays are in white and the normal mode is selected (see page 60 *12 for details of the conditions).
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply $V_{DD} – V_{SS}$ = 1.8 V to –5.5 V
  Boost reference voltage: $V_{DD} – V_{SS2}$ = 1.8 V to –6.0 V
  Liquid crystal drive power supply: $V_{DD} – V_5$ = –4.5 V to –16.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or resistance to radiation.

Series Specifications

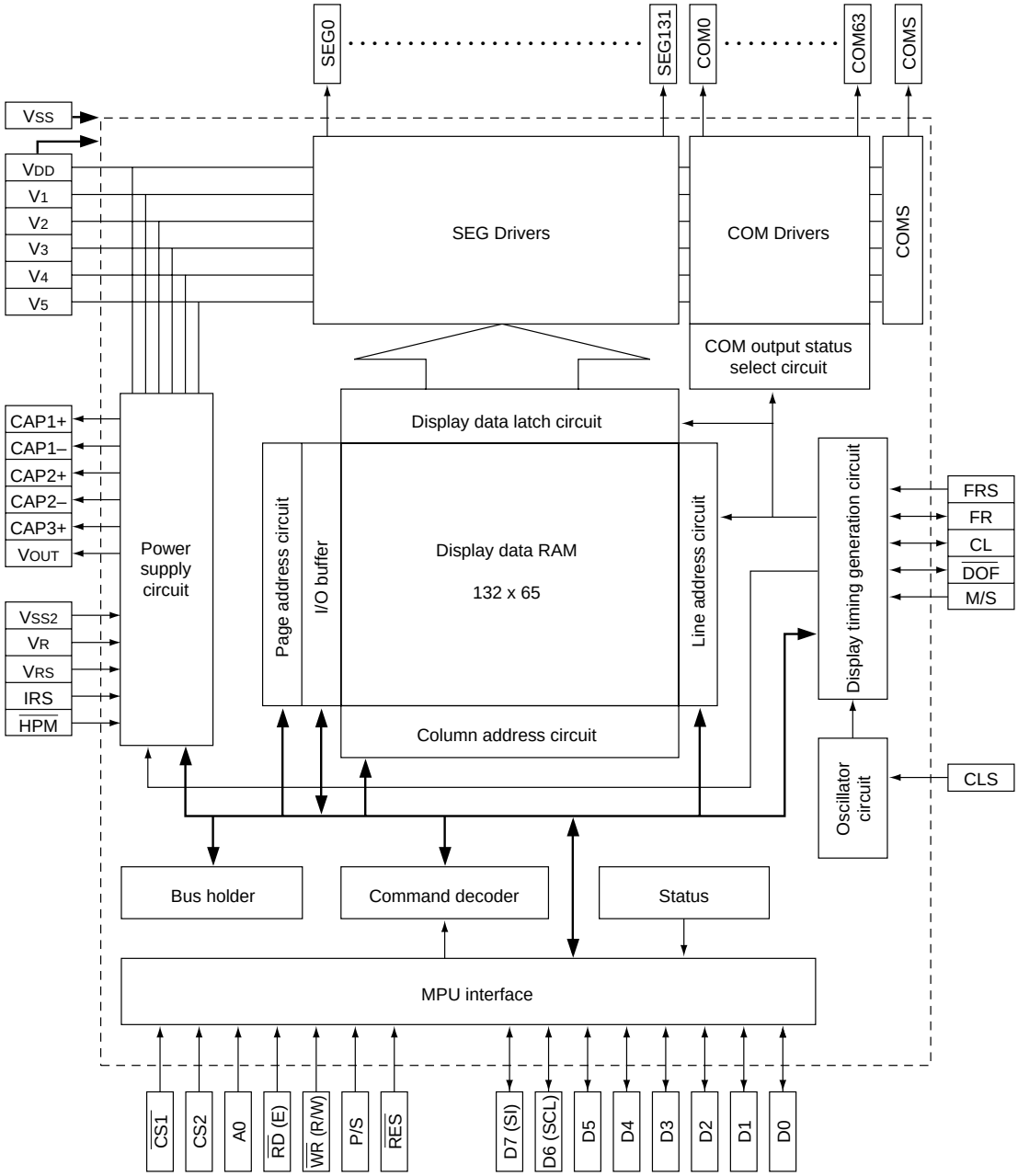
Product Name	Duty	Bias	SED Dr	COM Dr	V_{REG} Temperature Gradient	Shipping Forms
SED1565D0*	1/65	1/9, 1/7	132	65	–0.05%/°C	Bare Chip
SED1565T0*	1/65	1/9, 1/7	132	65	–0.05%/°C	TCP
* SED1565D1*	1/65	1/9, 1/7	132	65	–0.2%/°C	Bare Chip
* SED1565T1*	1/65	1/9, 1/7	132	65	–0.2%/°C	TCP
SED1565D2*	1/65	1/9, 1/7	132	65	External Input	Bare Chip
SED1565T2*	1/65	1/9, 1/7	132	65	External Input	TCP
SED1566D0*	1/49	1/8, 1/6	132	49	–0.05%/°C	Bare Chip
SED1566T0*	1/49	1/8, 1/6	132	49	–0.05%/°C	TCP
* SED1566D1*	1/49	1/8, 1/6	132	49	–0.2%/°C	Bare Chip
* SED1566T1*	1/49	1/8, 1/6	132	49	–0.2%/°C	TCP
SED1566D2*	1/49	1/8, 1/6	132	49	External Input	Bare Chip
SED1566T2*	1/49	1/8, 1/6	132	49	External Input	TCP
SED1567D0*	1/33	1/6, 1/5	132	33	–0.05%/°C	Bare Chip
SED1567T0*	1/33	1/6, 1/5	132	33	–0.05%/°C	TCP
* SED1567D1*	1/33	1/6, 1/5	132	33	–0.2%/°C	Bare Chip
* SED1567T1*	1/33	1/6, 1/5	132	33	–0.2%/°C	TCP
SED1567D2*	1/33	1/6, 1/5	132	33	External Input	Bare Chip
SED1567T2*	1/33	1/6, 1/5	132	33	External Input	TCP
SED1568D0*	1/55	1/8, 1/6	132	55	–0.05%/°C	Bare Chip
SED1569D0*	1/53	1/8, 1/6	132	53	–0.05%/°C	Bare Chip
* SED1569T0*	1/53	1/8, 1/6	132	53	–0.05%/°C	TCP

Note: The circuit for the V_{REG} temperature gradient –0.2%/°C and the external input is under preparation.

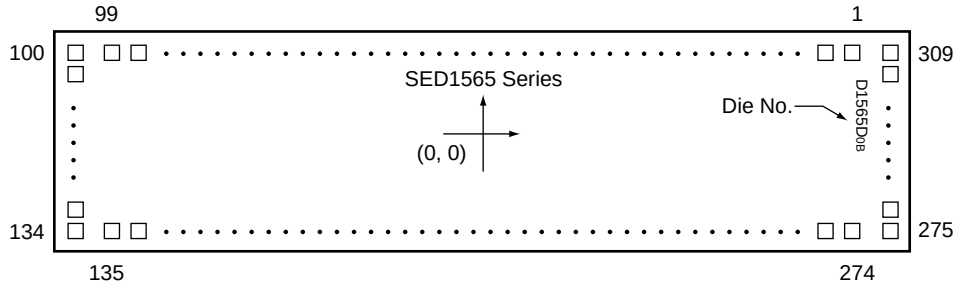
* : Under development

BLOCK DIAGRAM

Example: SED1565***



PIN DIMENSIONS



Chip Size	10.82 mm × 2.81 mm	
Bump Pitch	71 µm (Min.)	
Bump Size	PAD No. 1~24	85 µm × 85 µm
	PAD No. 25~82	64 µm × 85 µm
	PAD No. 83~99	85 µm × 85 µm
	PAD No. 100	85 µm × 73 µm
	PAD No. 101~133	85 µm × 47 µm
	PAD No. 134	85 µm × 73 µm
	PAD No. 135	73 µm × 85 µm
	PAD No. 136~273	47 µm × 85 µm
	PAD No. 274	73 µm × 85 µm
	PAD No. 275	85 µm × 73 µm
	PAD No. 276~308	85 µm × 47 µm
	PAD No. 309	85 µm × 73 µm
Bump Height	17 µm (Typ.)	
Chip Thickness	625 µm	

SED1565*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM31		1163
102	COM30		1090
103	COM29		1017
104	COM28		945
105	COM27		872
106	COM26		799
107	COM25		727
108	COM24		654
109	COM23		581
110	COM22		509
111	COM21		436
112	COM20		363
113	COM19		291
114	COM18		218
115	COM17		145
116	COM16		73
117	COM15		0
118	COM14		–73
119	COM13		–145
120	COM12		–218

Units: µm

PAD No.	PIN Name	X	Y
121	COM11	–5252	–291
122	COM10		–363
123	COM9		–436
124	COM8		–509
125	COM7		–581
126	COM6		–654
127	COM5		–727
128	COM4		–800
129	COM3		–872
130	COM2		–945
131	COM1		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM32		–1163
277	COM33		–1090
278	COM34		–1018
279	COM35		–945
280	COM36		–872

PAD No.	PIN Name	X	Y
281	COM37	5252	–800
282	COM38		–727
283	COM39		–654
284	COM40		–581
285	COM41		–509
286	COM42		–436
287	COM43		–363
288	COM44		–291
289	COM45		–218
290	COM46		–145
291	COM47		–73
292	COM48		0
293	COM49		73
294	COM50		145
295	COM51		218
296	COM52		291
297	COM53		363
298	COM54		436
299	COM55		509
300	COM56		581
301	COM57		654
302	COM58		727
303	COM59		799
304	COM60		872
305	COM61		945
306	COM62		1017
307	COM63		1090
308	COMS		1163
309	(NC)		1248

SED1566*** Pad Center Coordinates

Units: µm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	HPM	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	(NC)		1090
103	COM23		1017
104	(NC)		945
105	COM22		872
106	(NC)		799
107	COM21		727
108	COM20		654
109	COM19		581
110	COM18		509
111	COM17		436
112	COM16		363
113	COM15		291
114	COM14		218
115	COM13		145
116	COM12		73
117	COM11		0
118	COM10		–73
119	COM9		–145
120	COM8		–218

Units: µm

PAD No.	PIN Name	X	Y
121	COM7	–5252	–291
122	COM6		–363
123	COM5		–436
124	COM4		–509
125	COM3		–581
126	COM2		–654
127	COM1		–727
128	(NC)		–800
129	COM0		–872
130	(NC)		–945
131	COMS		–1018
132	(NC)		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	(NC)		–1090
278	COM24		–1018
279	(NC)		–945
280	COM25		–872

PAD No.	PIN Name	X	Y
281	(NC)	5252	–800
282	COM26		–727
283	COM27		–654
284	COM28		–581
285	COM29		–509
286	COM30		–436
287	COM31		–363
288	COM32		–291
289	COM33		–218
290	COM34		–145
291	COM35		–73
292	COM36		0
293	COM37		73
294	COM38		145
295	COM39		218
296	COM40		291
297	COM41		363
298	COM42		436
299	COM43		509
300	COM44		581
301	COM45		654
302	COM46		727
303	(NC)		799
304	COM47		872
305	(NC)		945
306	COMS		1017
307	(NC)		1090
308	(NC)		1163
309	(NC)		1248

SED1567*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM15		1163
102	COM15		1090
103	COM14		1017
104	COM14		945
105	COM13		872
106	COM13		799
107	COM12		727
108	COM12		654
109	COM11		581
110	COM11		509
111	COM10		436
112	COM10		363
113	COM9		291
114	COM9		218
115	COM8		145
116	COM8		73
117	COM7		0
118	COM7		–73
119	COM6		–145
120	COM6		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM5	–5252	–291
122	COM5		–363
123	COM4		–436
124	COM4		–509
125	COM3		–581
126	COM3		–654
127	COM2		–727
128	COM2		–800
129	COM1		–872
130	COM1		–945
131	COM0		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM16		–1163
277	COM16		–1090
278	COM17		–1018
279	COM17		–945
280	COM18		–872

PAD No.	PIN Name	X	Y
281	COM18	5252	–800
282	COM19		–727
283	COM19		–654
284	COM20		–581
285	COM20		–509
286	COM21		–436
287	COM21		–363
288	COM22		–291
289	COM22		–218
290	COM23		–145
291	COM23		–73
292	COM24		0
293	COM24		73
294	COM25		145
295	COM25		218
296	COM26		291
297	COM26		363
298	COM27		436
299	COM27		509
300	COM28		581
301	COM28		654
302	COM29		727
303	COM29		799
304	COM30		872
305	COM30		945
306	COM31		1017
307	COM31		1090
308	COMS		1163
309	(NC)		1248

SED1568*** Pad Center Coordinates

Units: µm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM26		1090
103	(NC)		1017
104	COM25		945
105	COM25		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: µm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM27		–1090
278	(NC)		–1018
279	COM28		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM29	5252	–800
282	COM30		–727
283	COM31		–654
284	COM32		–581
285	COM33		–509
286	COM34		–436
287	COM35		–363
288	COM36		–291
289	COM37		–218
290	COM38		–145
291	COM39		–73
292	COM40		0
293	COM41		73
294	COM42		145
295	COM43		218
296	COM44		291
297	COM45		363
298	COM46		436
299	COM47		509
300	COM48		581
301	COM48		654
302	COM50		727
303	COM51		799
304	COM52		872
305	COM53		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

SED1569*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM25		1090
103	(NC)		1017
104	COM24		945
105	(NC)		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM26		–1090
278	(NC)		–1018
279	COM27		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM28	5252	–800
282	COM29		–727
283	COM30		–654
284	COM31		–581
285	COM32		–509
286	COM33		–436
287	COM34		–363
288	COM35		–291
289	COM36		–218
290	COM37		–145
291	COM38		–73
292	COM39		0
293	COM40		73
294	COM41		145
295	COM42		218
296	COM43		291
297	COM44		363
298	COM45		436
299	COM46		509
300	COM47		581
301	COM48		654
302	COM49		727
303	COM50		799
304	(NC)		872
305	COM51		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

PIN DESCRIPTIONS

Power Supply Pins

Pin Name	I/O	Function	No. of Pins
V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.	13
V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.	9
V_{SS2}	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4
V_{RS}	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. These are only enabled for the models with the VREG external input option.	2
V_1, V_2, V_3, V_4, V_5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. $V_{DD} (= V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.	10

	SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
V_1	1/9•V_5 1/7•V_5	1/8•V_5 1/6•V_5	1/6•V_5 1/5•V_5	1/8•V_5 1/6•V_5	1/8•V_5 1/6•V_5
V_2	2/9•V_5 2/7•V_5	2/8•V_5 2/6•V_5	2/6•V_5 2/5•V_5	2/8•V_5 2/6•V_5	2/8•V_5 2/6•V_5
V_3	7/9•V_5 5/7•V_5	6/8•V_5 4/6•V_5	4/6•V_5 3/5•V_5	6/8•V_5 4/6•V_5	6/8•V_5 4/6•V_5
V_4	8/9•V_5 6/7•V_5	7/8•V_5 5/6•V_5	5/6•V_5 4/5•V_5	7/8•V_5 5/6•V_5	7/6•V_5 5/6•V_5

LCD Power Supply Circuit Terminals

Pin Name	I/O	Function	No. of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.	2
V_R	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = “L”). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = “H”).	2

System Bus Connection Terminals

Pin Name	I/O	Function	No. of Pins
D7 to D0 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	8
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.	1
$\overline{RES}$	I	When $\overline{RES}$ is set to "L," the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	This is the chip select signal. When $\overline{CS1}$ = "L" and CS2 = "H," then the chip select becomes active, and data/command I/O is enabled.	2
$\overline{RD}$ (E)	I	• When connected to an 8080 MPU, this is active LOW. This pin is connected to the $\overline{RD}$ signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L". • When connected to a 6800 Series MPU, this is active HIGH. This is the 68000 Series MPU enable clock input terminal.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ = "H": Read. When R/$\overline{W}$ = "L": Write.	1
C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: **P/S** | **Data/Command** | **Data** | **Read/Write** | **Serial Clock** "H" | A0 | D0 to D7 | $\overline{RD}$, $\overline{WR}$ | "L" | A0 | SI (D7) | Write only | SCL (D6) When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.	1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = “H”: Internal oscillator circuit is enabled
CLS = “L”: Internal oscillator circuit is disabled (requires external input)
When CLS = “L”, input the display clock through the CL terminal.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the SED1565 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Output
Input</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Input
Input</td></tr>
</table>When the SED1565 Series chips are used in master/slave mode, the various CL terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>1</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various $\overline{\text{DOF}}$ terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>$\overline{\text{HPM}}$</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{\text{HPM}}$ = “H”: Normal mode
$\overline{\text{HPM}}$ = “L”: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_{DD}, V_2, V_3, and V_5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>SED1565*** </td><td>COM 0 ~ COM 63</td></tr>
<tr><td>SED1566*** </td><td>COM 0 ~ COM 47</td></tr>
<tr><td>SED1567*** </td><td>COM 0 ~ COM 31</td></tr>
<tr><td>SED1568*** </td><td>COM 0 ~ COM 53</td></tr>
<tr><td>SED1569*** </td><td>COM 0 ~ COM 51</td></tr>
</table>
<table>
<tr><th>Part No.</th><th></th></tr>
<tr><td>SED1565*** </td><td>64</td></tr>
<tr><td>SED1566*** </td><td>48</td></tr>
<tr><td>SED1567*** </td><td>32</td></tr>
<tr><td>SED1568*** </td><td>54</td></tr>
<tr><td>SED1569*** </td><td>52</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_{DD}, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
</table>

Test Terminals

Pin Name	I/O	Function	No. of Pins
TEST0 to 4 TEST7 to 9	I/O	These are terminals for IC chip testing. They are set to OPEN.	12
TEST5, 6	I	These are terminals for IC chip testing. They are set to V_{DD}.	2

Total: 288 pins for the SED1565***.
272 pins for the SED1566***.
256 pins for the SED1567***.

DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the SED1565 Series chips, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
H: Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
L: Serial Input	CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either "H" or to "L"

The Parallel Interface

When the parallel interface has been selected (P/S = "H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

Table 2

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0
H: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7~D0
L: 8080 MPU Bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0

Moreover, data bus signals are recognized by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state ($\overline{CS1}$ = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

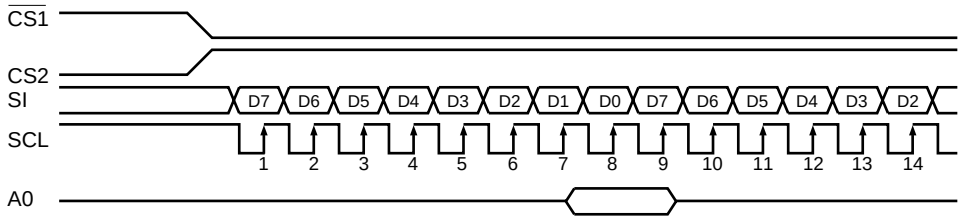


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The SED1565 Series chips have two chip select terminals: $\overline{CS1}$ and CS2. The MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H".
When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, $\overline{RD}$, and $\overline{WR}$ inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the SED1565 Series. Wait time may not be considered.
And, in the SED1565 Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is "1" it indicates that the SED1565 Series chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

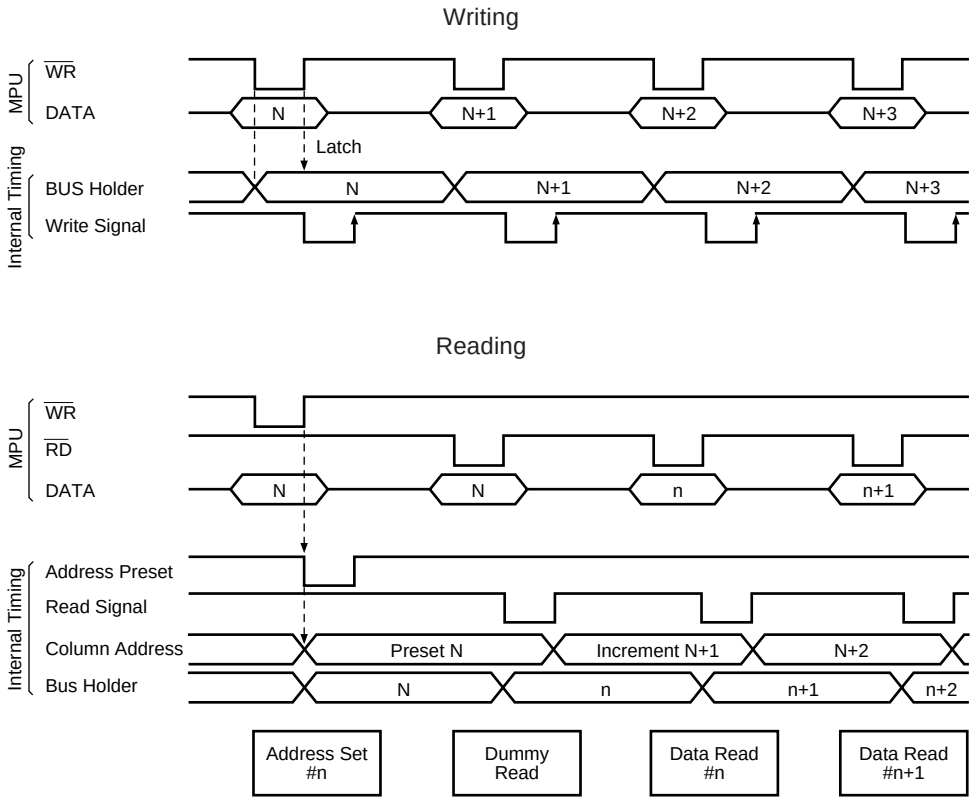


Figure 2

Display Data RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page x 8 bit +1) x 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple SED1565 series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

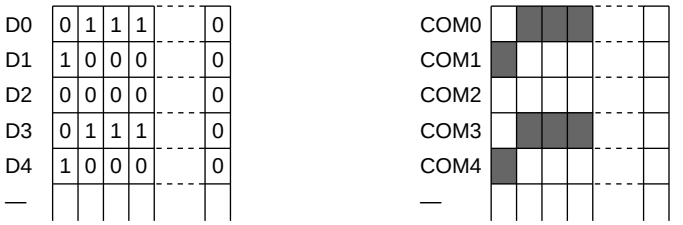


Figure 3

The Page Address Circuit

As shown in Figure 6-4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

The Column Addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementation of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG 131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
(D0) "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SED1565 Series, COM47 output for SED1566 Series and COM31 output for the SED1567 Series when the common output mode is reversed. The display area is a 65 line area for the SED1565 Series, a 49 line are for the SED1566 and a 33 line area for the SED1567 Series from the display start line address.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

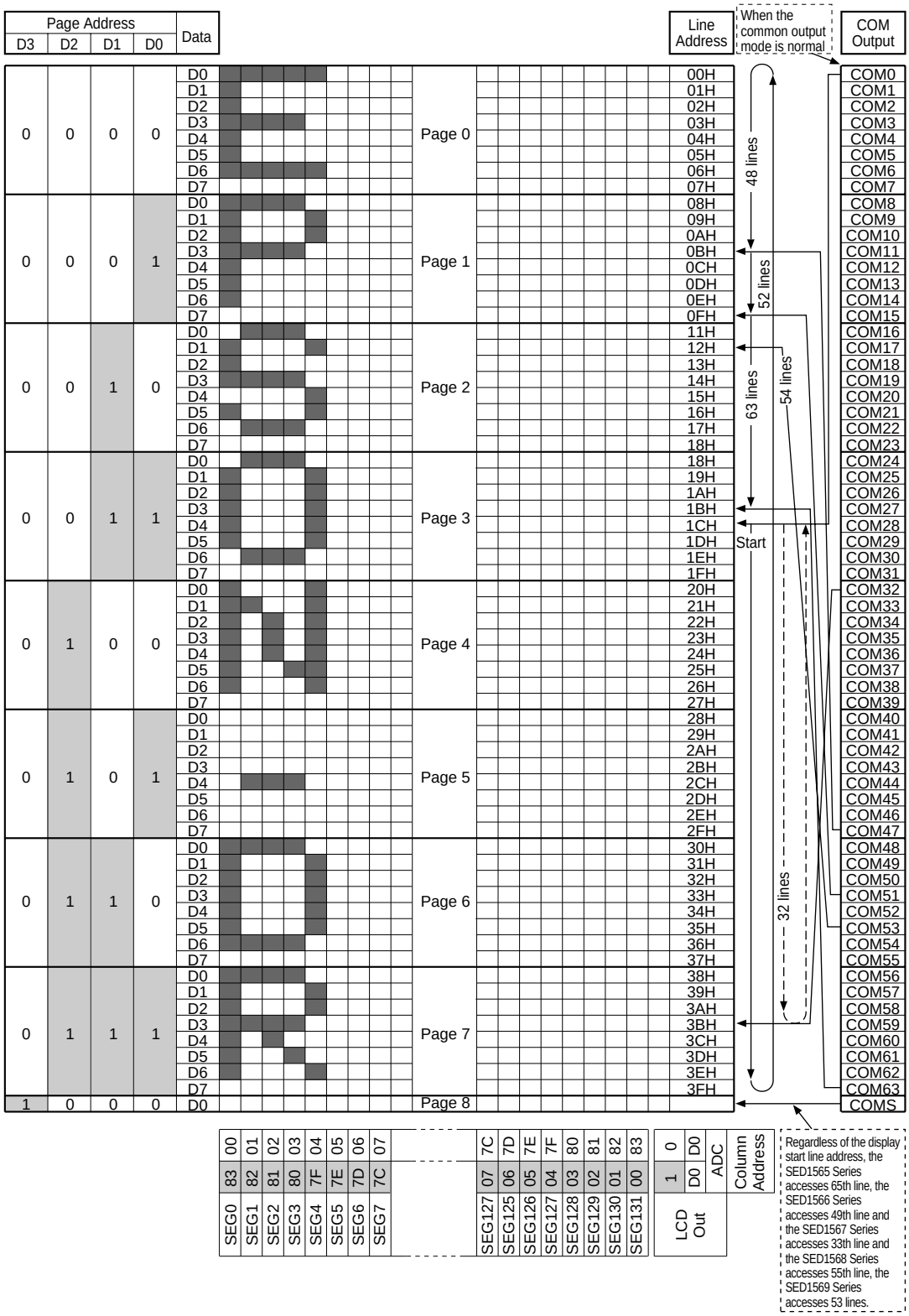

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output mode is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
63 lines
54 lines
32 lines
Start
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63 COMS
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG127 SEG125 SEG126 SEG127 SEG128 SEG129 SEG130 SEG131
LCD Out
Column Address
ADC
Regardless of the display start line address, the SED1565 Series accesses 65th line, the SED1566 Series accesses 49th line and the SED1567 Series accesses 33th line and the SED1568 Series accesses 55th line, the SED1569 Series accesses 53 lines.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H".
When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive wave form (SED1565***)

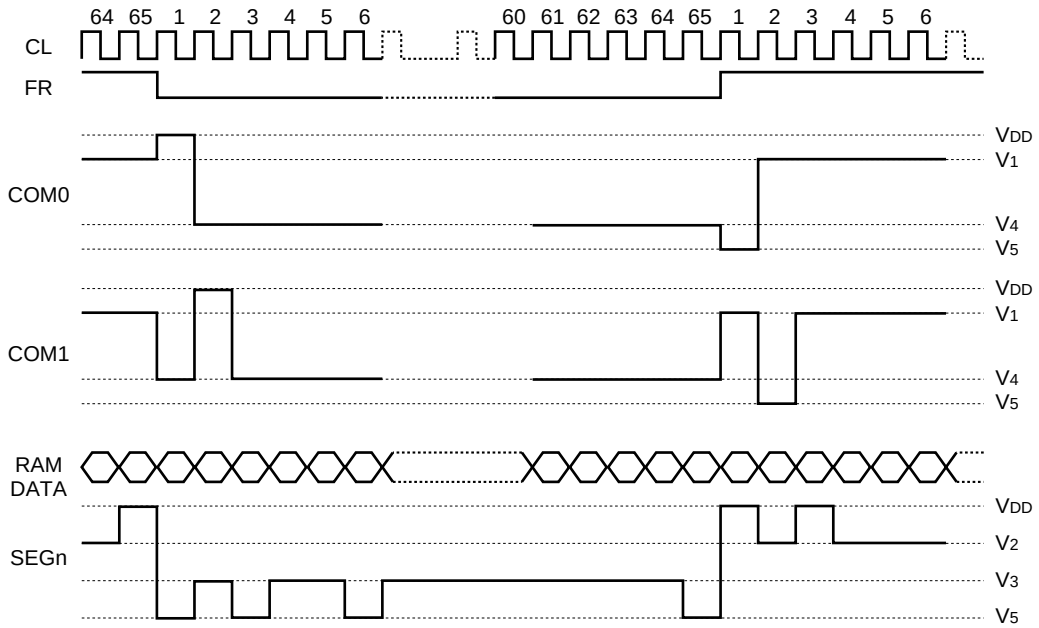


Figure 5

When multiple SED1565 Series chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip[s].
Table 5 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 5

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S = "H")	The internal oscillator circuit is enabled (CLS = "H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal oscillator circuit is enabled (CLS = "H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS = "L")	Input	Input	Input

The Common Output Status Select Circuit

In the SED1565 Series chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

The Liquid Crystal Driver Circuits

These are a 197-channel (SED1565 Series), a 181-channel (SED1566 Series) multiplexers 165-channel (SED1567 Series) and a 185-channel (SED1569 Series) that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.
Figure 6 shows examples of the SEG and COM output wave form.

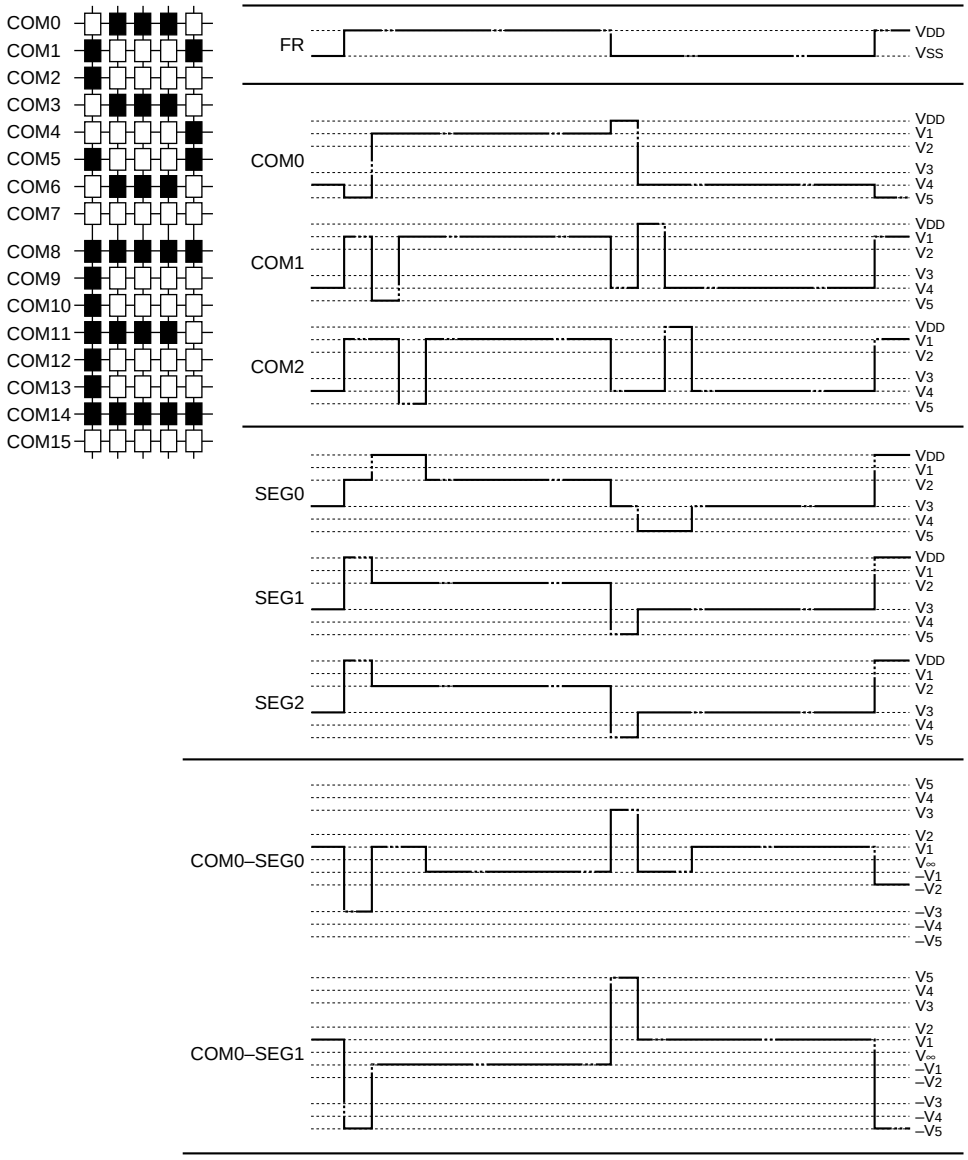

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V1
V2
V3
V4
V5
SEG0
SEG1
SEG2
COM0–SEG0
COM0–SEG1
V∞
–V1
–V2
–V3
–V4
–V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON of OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7 The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference Combinations

Use Settings	D2	D1	D0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
① Only the internal power supply is used	1	1	1	O	O	O	V_{SS2}	Used
② Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{SS2}	Open
③ Only the V/F circuit is used	0	0	1	X	X	O	V_5, V_{SS2}	Open
④ Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the SED1565 Series chips it is possible to product a Quad step-up, a Triple step-up, and a Double step-up of the $V_{DD} - V_{SS2}$ voltage levels.

Quad step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{SS2} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS2}.

Triple step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{SS2} and V_{OUT}, and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS2}.

Double step-up: Connect capacitor C1 between CAP1+ and CAP1–, and between V_{SS2} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that is twice the voltage between V_{DD} and V_{SS2}.

The step-up voltage relationships are shown in Figure 7.

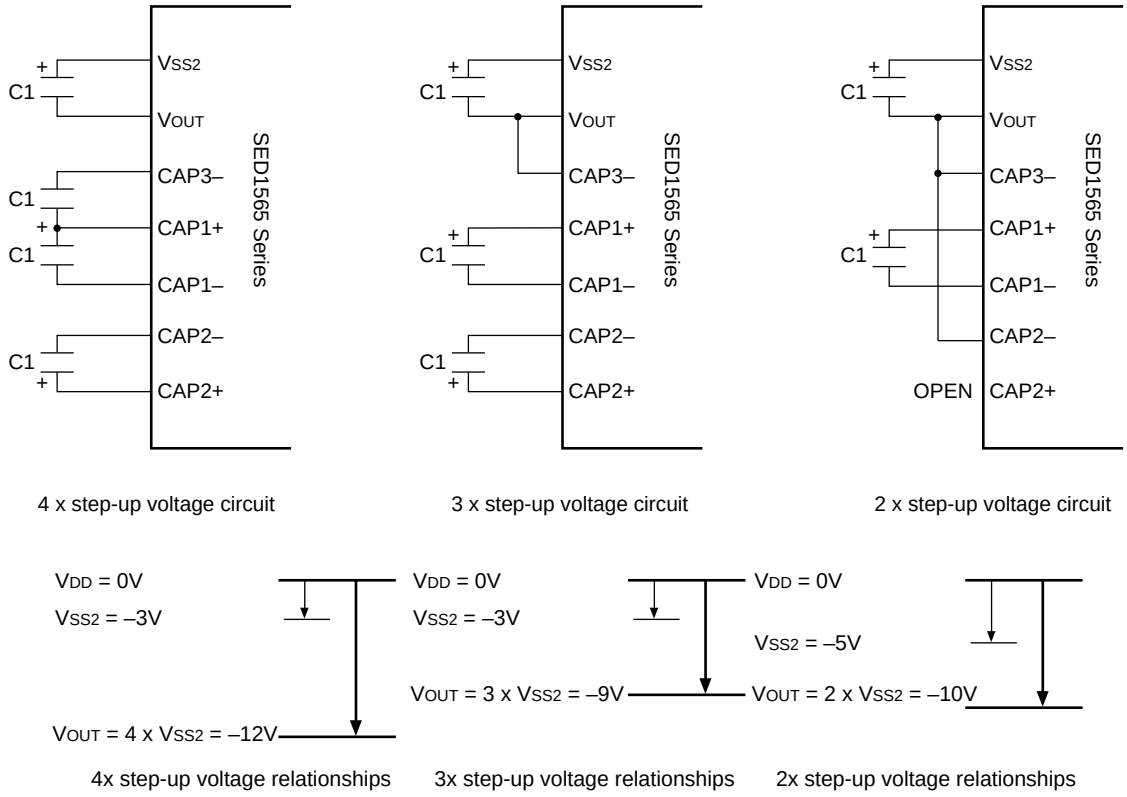


Figure 7

* The V_{SS2} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit.

Because the SED1565 Series chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, in the SED1565 Series, three types of thermal gradients have been prepared as V_{REG} options: (1) approximately -0.05%/°C (2) approximately -0.2%/°C, and (3) external input (supplied to the V_{RS} terminal).

(A) When the V_5 Voltage Regulator Internal Resistors Are Used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation A-1)}$$

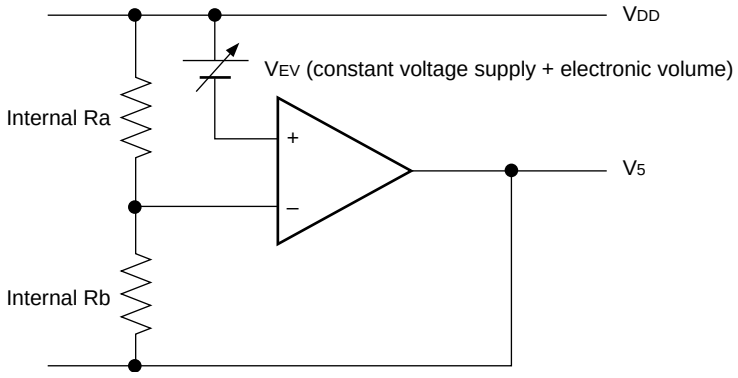


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
(1) Internal Power Supply	–0.05	[%/°C]	–2.1	[V]
(2) Internal Power Supply	–0.2	[%/°C]	–4.9	[V]
(3) External Input	—	—	VRS	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		⋮				⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			SED1565***			SED1566***		
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]		
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	(1) –0.05	(2) –0.2	(3) V_{REG} External Input
0	0	0	3.0	1.3	1.5	3.0	1.3	1.5
0	0	1	3.5	1.5	2.0	3.5	1.5	2.0
0	1	0	4.0	1.8	2.5	4.0	1.8	2.5
0	1	1	4.5	2.0	3.0	4.5	2.0	3.0
1	0	0	5.0	2.3	3.5	5.0	2.3	3.5
1	0	1	5.5	2.5	4.0	5.4	2.5	4.0
1	1	0	6.0	2.8	4.5	5.9	2.8	4.5
1	1	1	6.4	3.0	5.0	6.4	3.0	5.0

Register			SED1567***			SED1568***/SED1569***
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	–0.05
0	0	0	3.0	1.3	1.5	3
0	0	1	3.5	1.5	2.0	3.5
0	1	0	4.0	1.8	2.5	4
0	1	1	4.5	2.0	3.0	4.5
1	0	0	5.0	2.3	3.5	5
1	0	1	5.4	2.5	4.0	5.4
1	1	0	5.9	2.8	4.5	5.9
1	1	1	6.4	3.0	5.0	6.4

Figs. 9, 10, 11 (for SED1565 Series), 12, 13, 14 (for SED1566 Series) and Figs. 15, 16, 17 show V_5 voltage measured by values of the internal resistance ratio resistor for V_5 voltage adjustment and electric volume resister for each temperature grade model, when Ta = 25 °C.

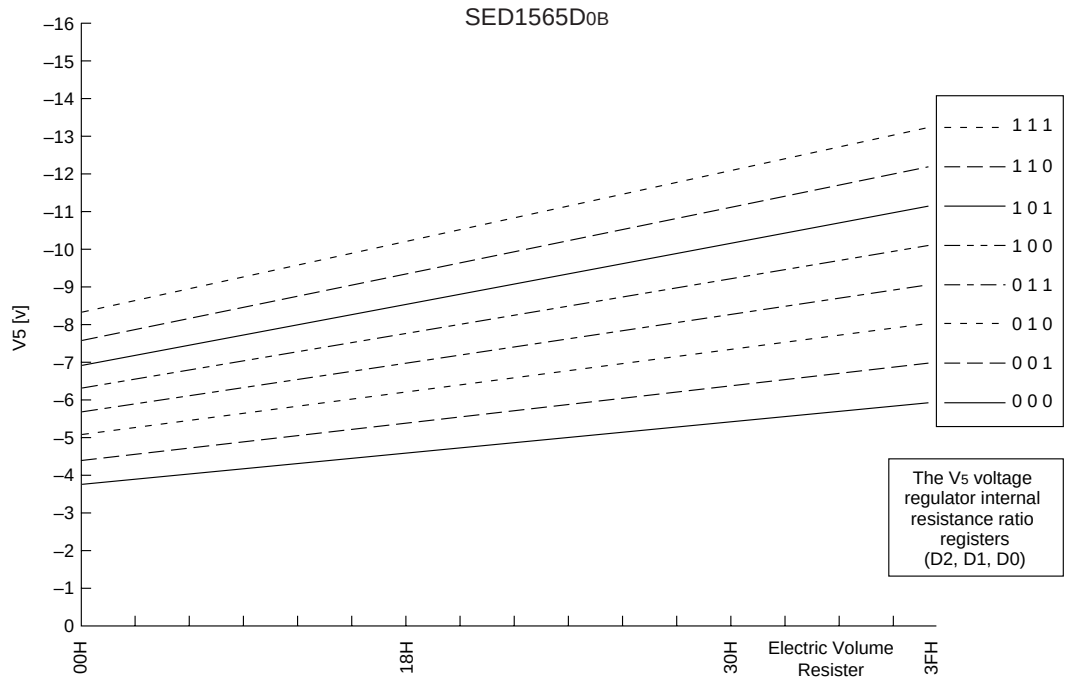


Figure 9: SED1565D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

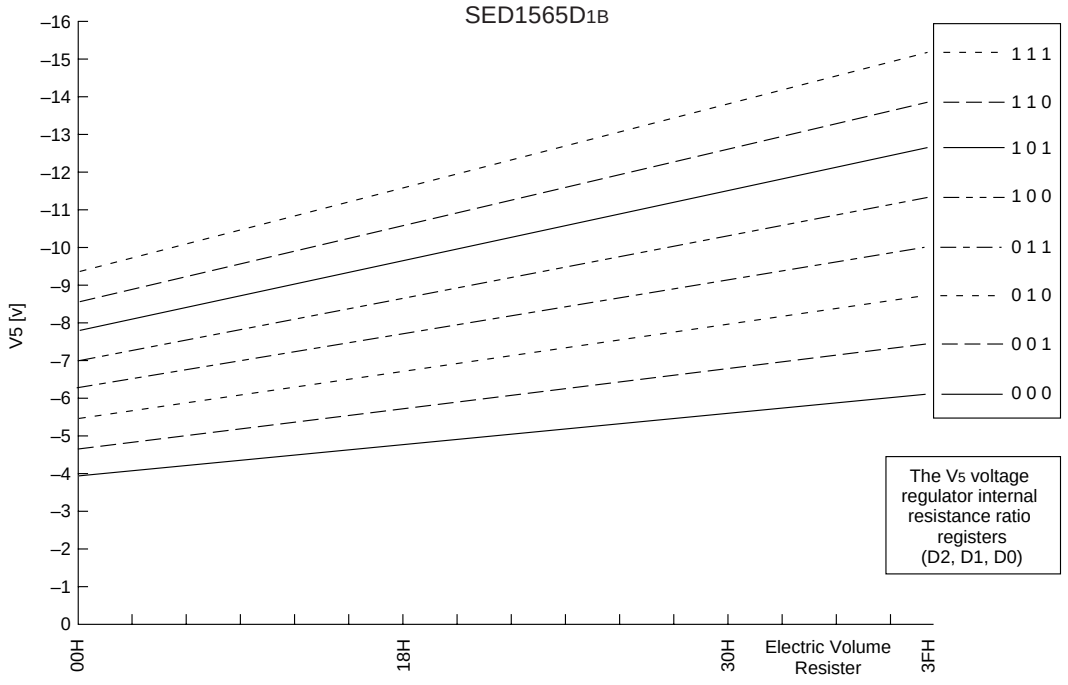


Figure 10: SED1565D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

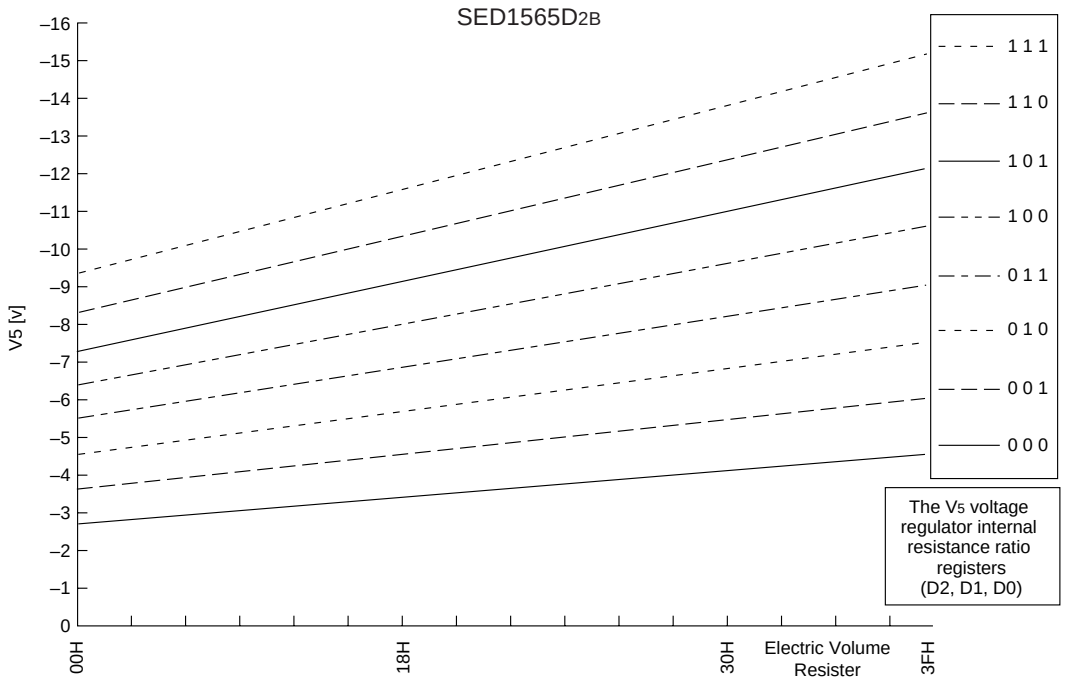


Figure 11: SED1565D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

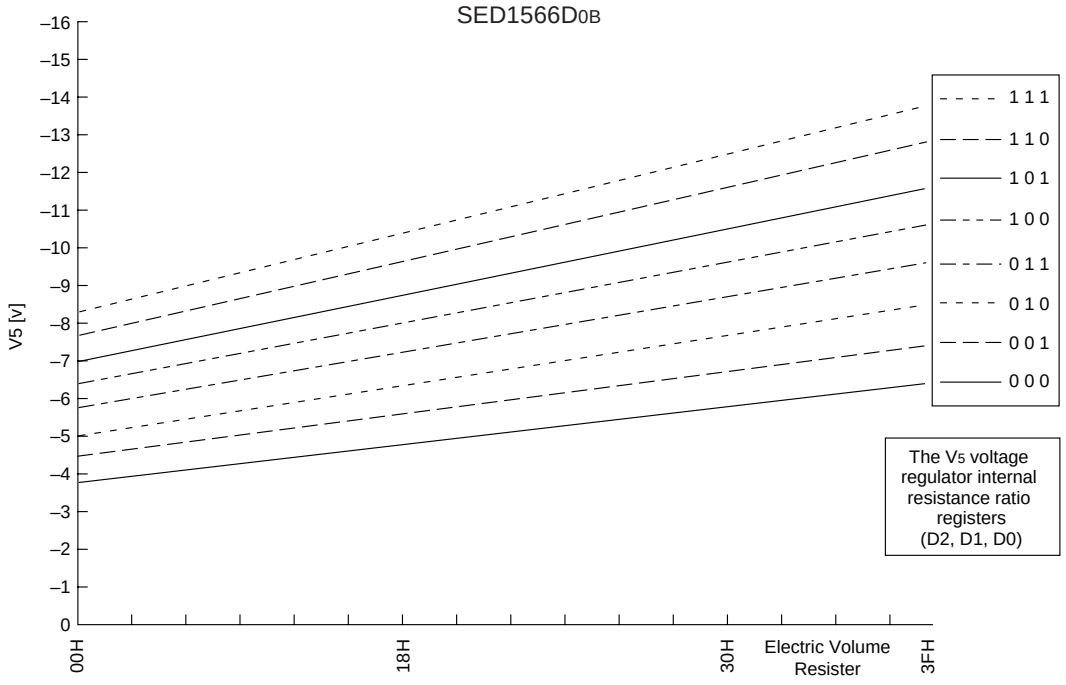


Figure 12: SED1566D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

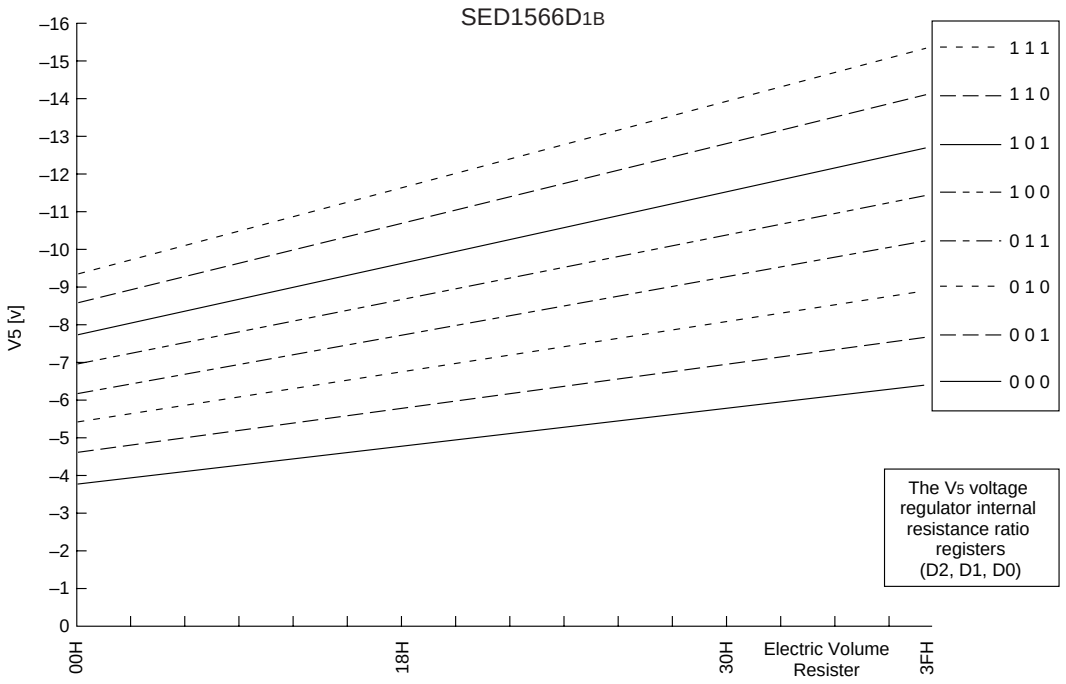


Figure 13: SED1566D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

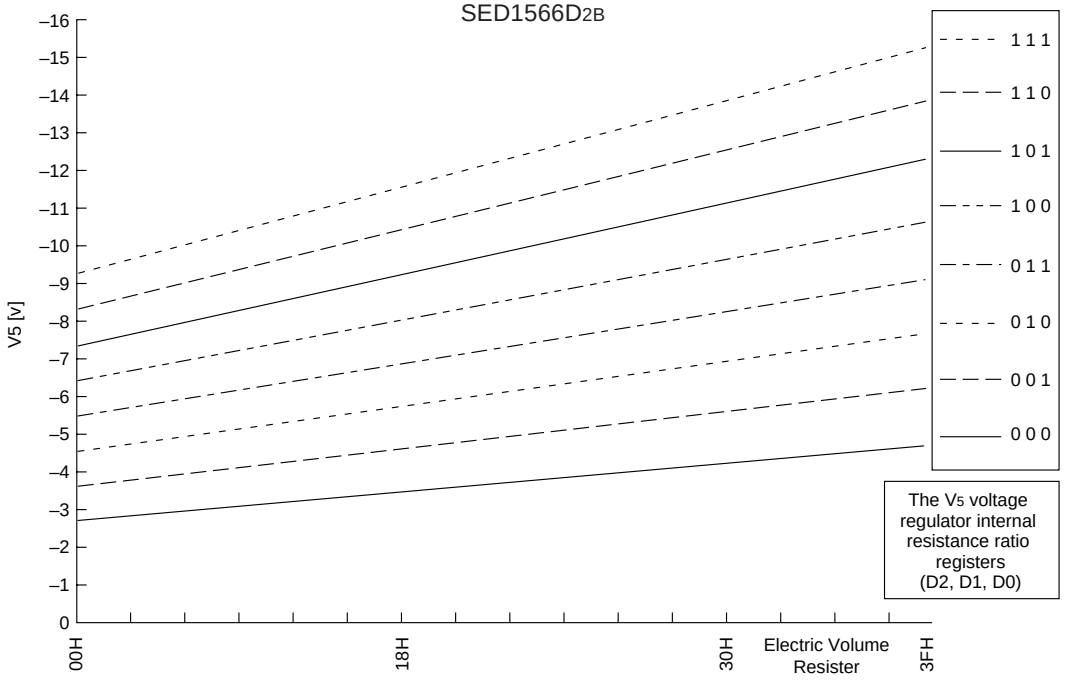


Figure 14: SED1566D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

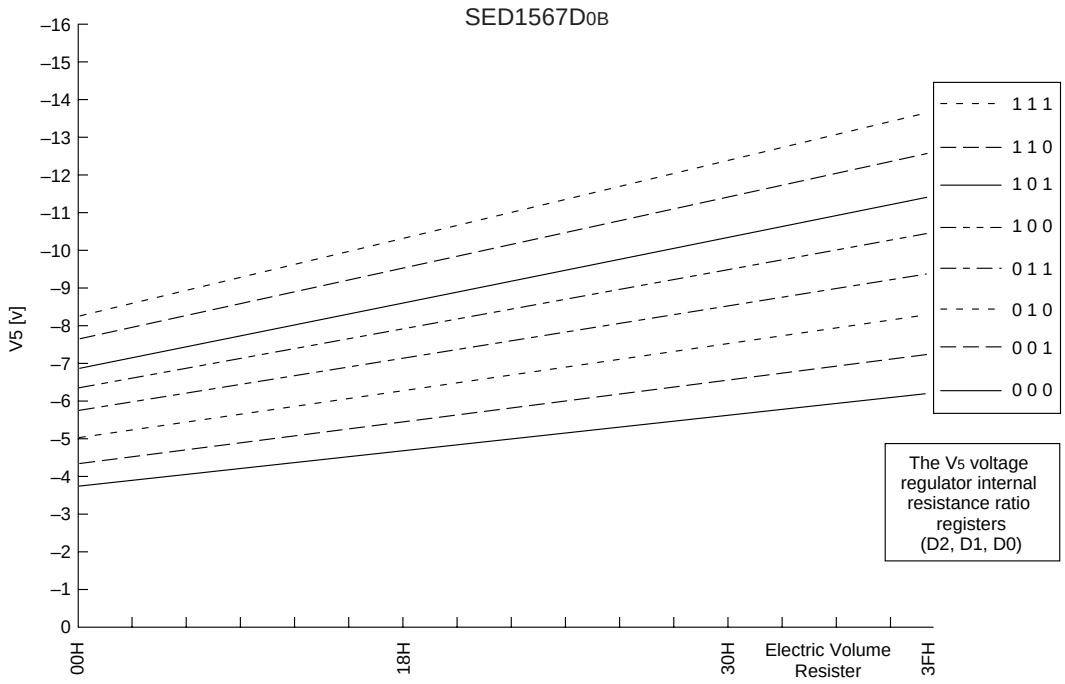


Figure 15: SED1567D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

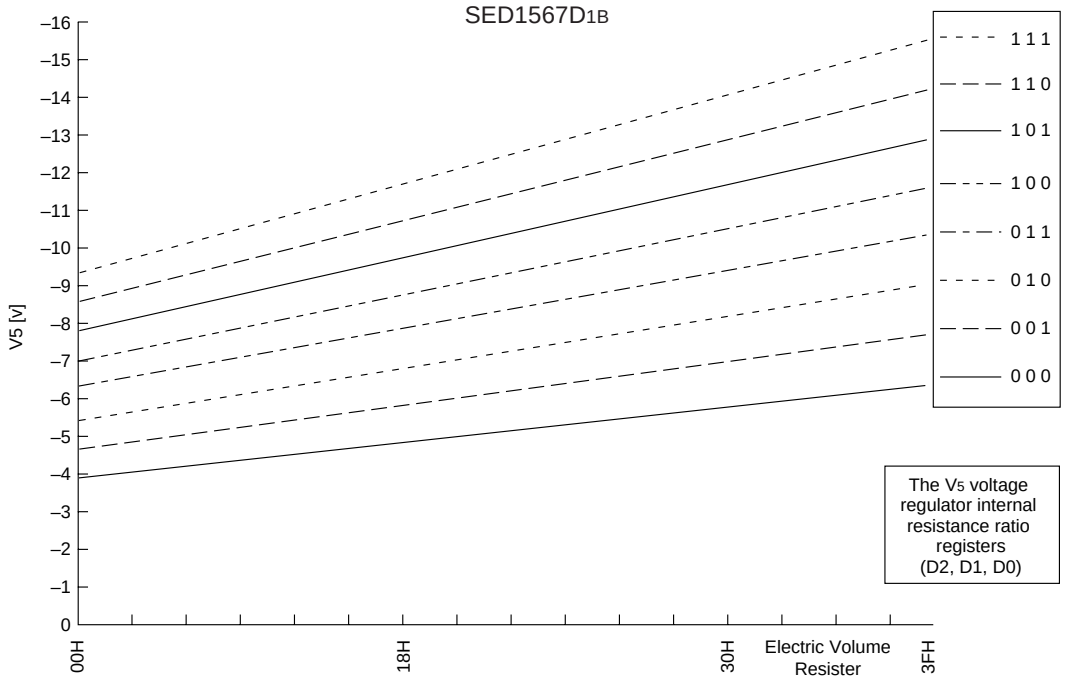


Figure 16: SED1567D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

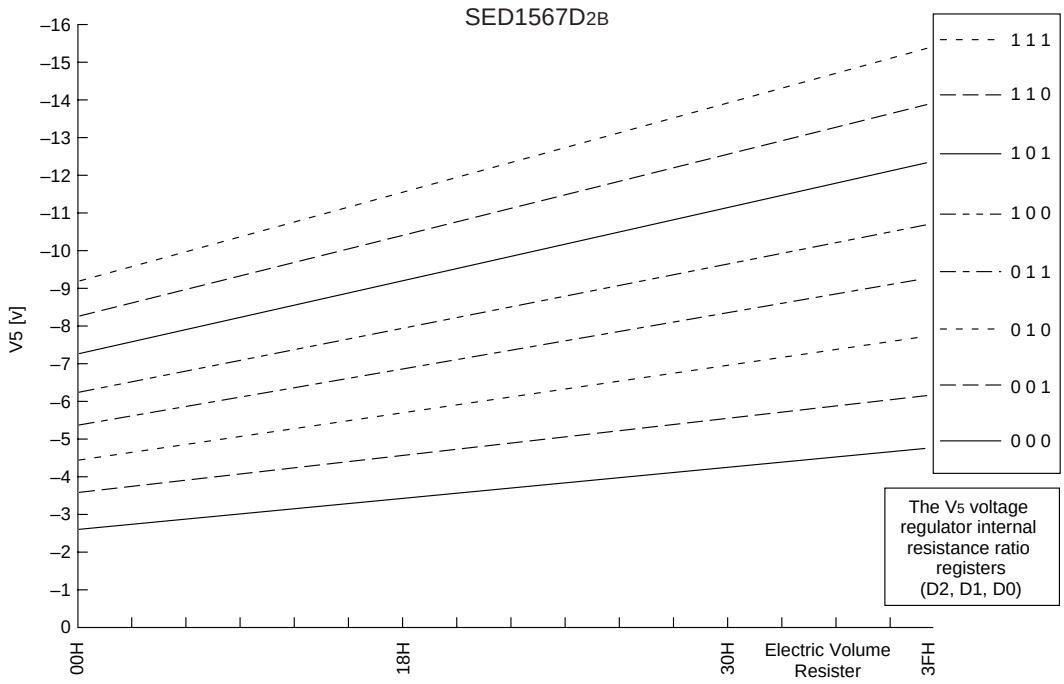


Figure 17: SED1567D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

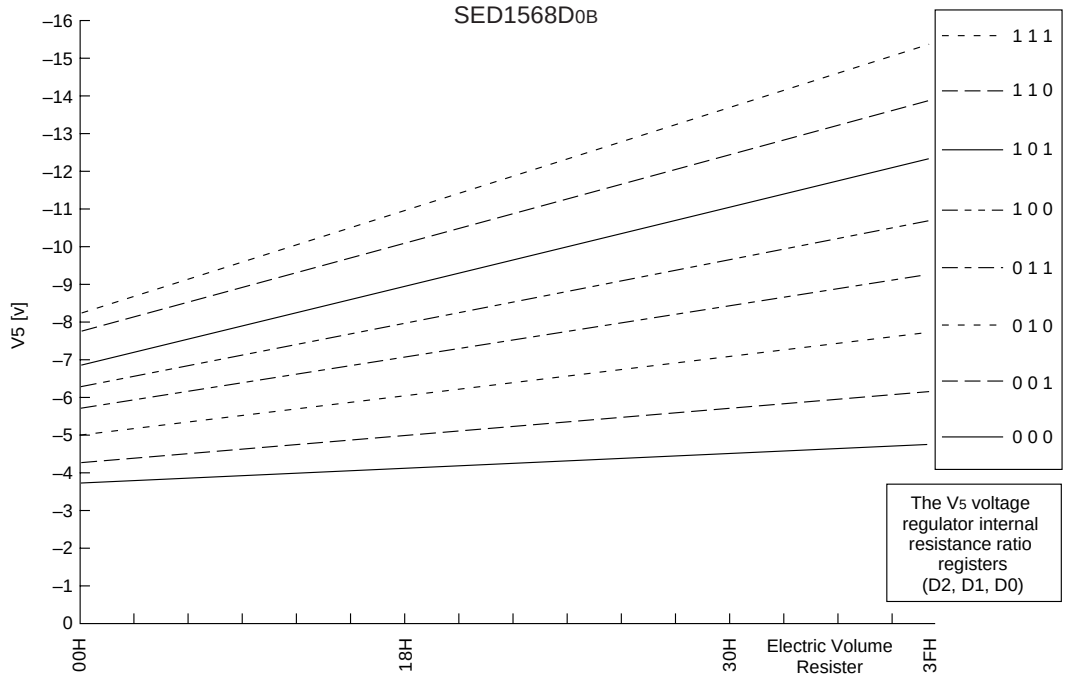


Figure 18: SED1568D0B (1) For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

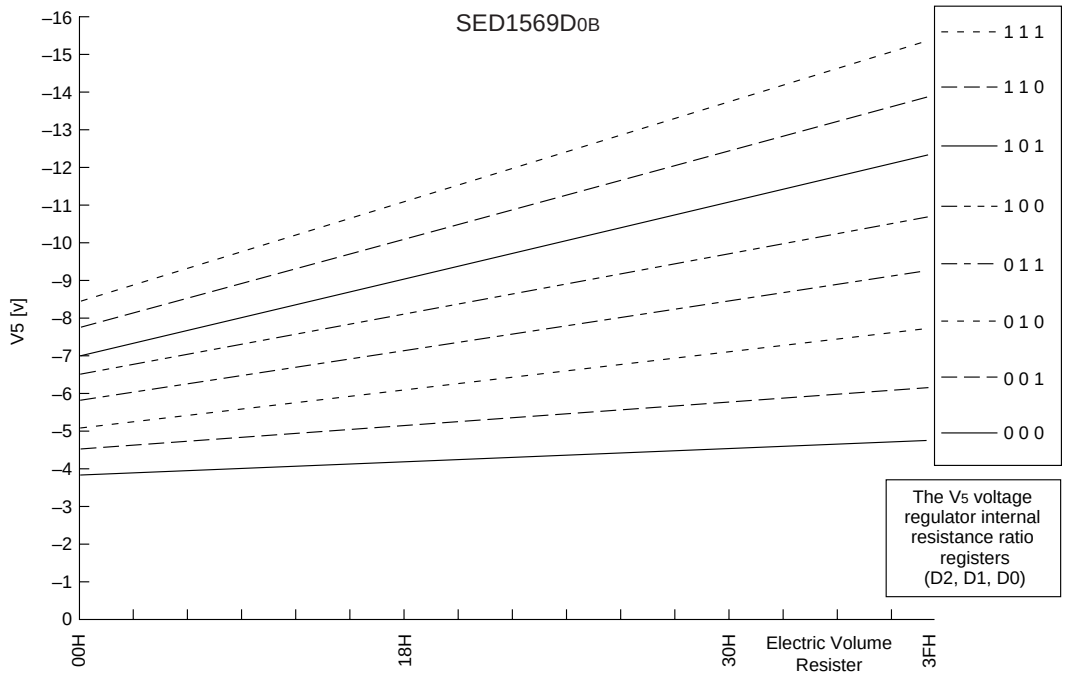


Figure 19: SED1569D0B (Temperature Gradient = –0.05%/°C Model

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_5 = 7 V for an SED1567 model on which Temperature gradient = –0.05%/°C.
Using Figure 15 and the equation A-1, the following setup is enabled.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

At this time, the variable range and the notch width of the V_5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 13

V_5	Min	Typ	Max	Units
Variable Range	–8.4 (63 levels)	–6.8 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (i.e., The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Equation B-1)}$$

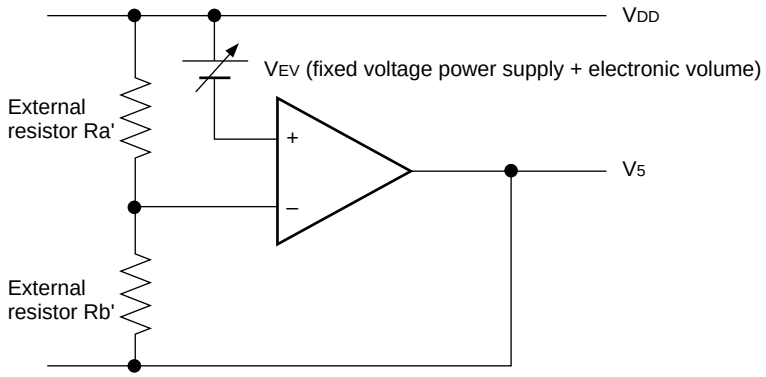


Figure 20

Setup example: When selecting Ta = 25°C and V5 = –7 V for an SED1567 Series model where the temperature gradient = –0.05%/°C.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1 V so, according to equation B-1,

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$-11V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1) \qquad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min	Typ	Max	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation C-1)}$$

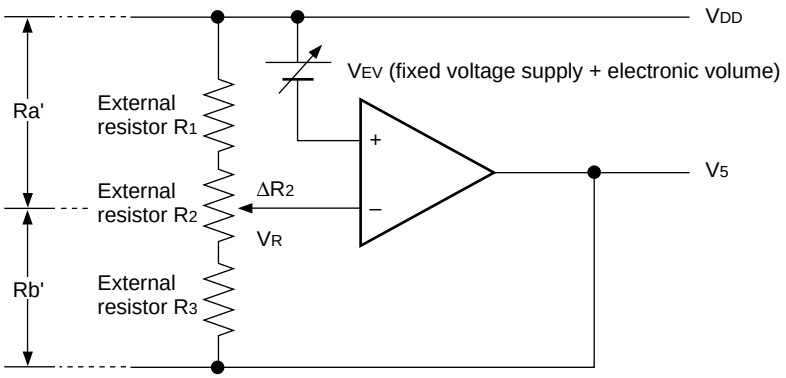


Figure 21

Setup example: When selecting Ta = 25°C and V_5 = –5 to –9 V (using R2) for an SED1567 model where the temperature gradient = –0.05%/°C.
When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0),

$$\alpha = 31$$

$$V_{REG} = -2.1V$$

so, according to equation C-1, when $\Delta R_2 = 0\ \Omega$, in order to make V_5 = –9 V,

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-2)

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

Moreover, when the current flowing V_{DD} and V_5 is set to 5 µA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R_1 = 264k\Omega$$

$$R_2 = 211k\Omega$$

$$R_3 = 925k\Omega$$

At this time, the V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V_5	Min	Typ	Max	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for SED1565 Series, 1/8 bias or 1/6 bias for SED1566 Series and 1/6 bias or 1/5 bias for the SED1567 Series can be selected.

High Power Mode

The power supply circuit equipped in the SED1565 Series chips has very low power consumption (normal mode: $\overline{HPM}$ = "H"). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.
Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 20 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	Command address D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)
↓										
Step2	Display all points ON	1	0	1	0	0	1	0	1	
↓										
End	Internal power supply OFF									

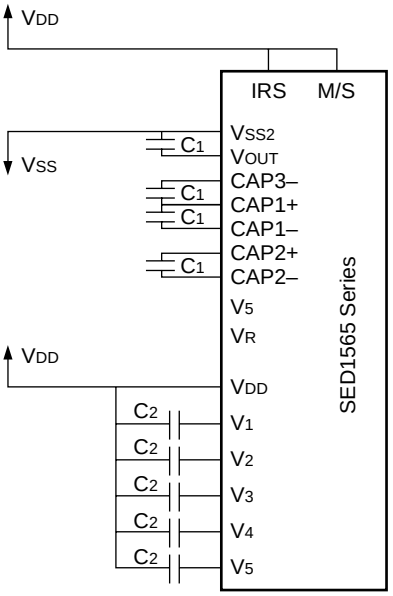
Figure 22

Reference Circuit Examples

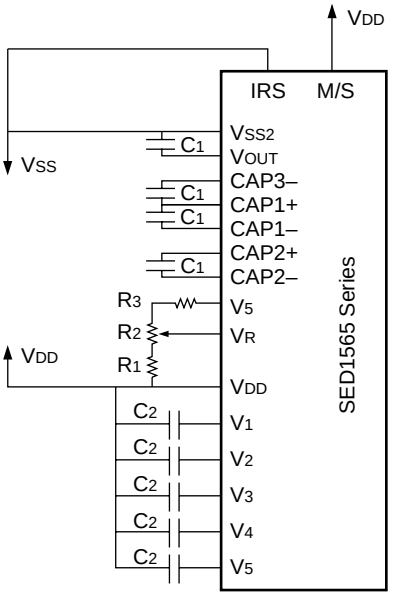
Figure 22 shows reference circuit examples.

① When used all of the step-up circuit, voltage regulating circuit and V/F circuit

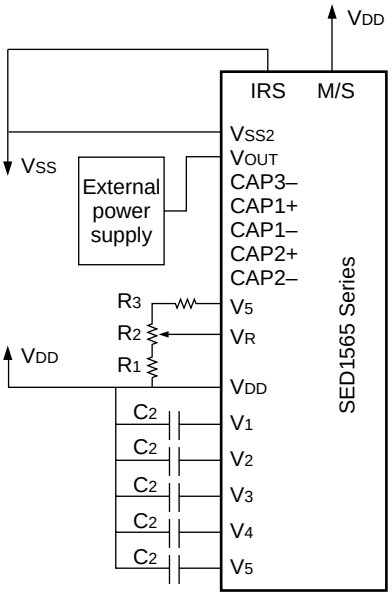
(1) When the voltage regulator internal resistor is used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)



(2) When the voltage regulator internal resistor is not used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

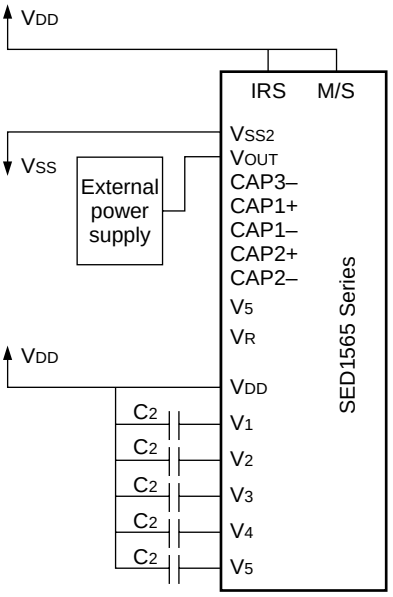


② When the voltage regulator circuit and V/F circuit alone are used
When the V_5 voltage regulator internal resistor is not used.

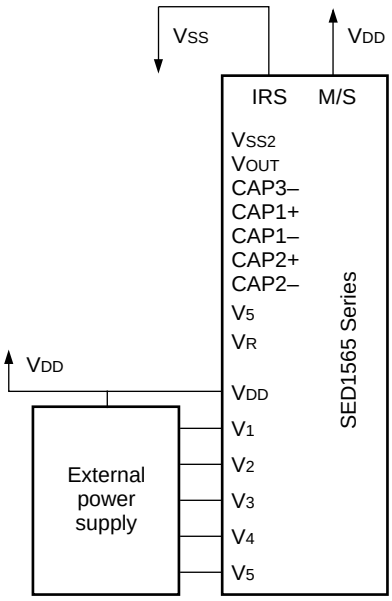


③ When the V/F circuit alone is used

When the V_5 voltage regulator internal resistor is used.



④ When the built-in power is not used



Examples of shared reference settings
When V_5 can vary between –8 and 12 V

Item	Set value	Units
C_1	1.0 ~ 4.7	µF
C_2	0.47 ~ 1.0	µF

Figure 23

* 1 Because the V_R terminal input impedance is high, use short leads and shielded lines.
* 2 C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_5). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

The Reset Circuit

When the $\overline{RES}$ input falls to "L", these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = "L")
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias ratio:
   SED1565*** ..... 1/9 bias
   SED1566*** ..... 1/8 bias
   SED1567*** ..... 1/6 bias
7. Read modify write OFF
8. Stack indicator OFF
   Stack indicator register: (D1, D2) = (0, 0)
9. Display start line set to first line
10. Column address set to address 0
11. Page address set to page 0
12. Common output status normal
13. V_5 voltage regulator internal power supply ratio set mode clear
    V_5 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = "L").
17. Output condition of COM, SEG.
    COM : V1
    SEG : V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect.

As is described in "11. The MPU Interface (Reference Example)," the $\overline{RES}$ terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the $\overline{RES}$ terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition to the IC. After applying a current, it is necessary to take measures to prevent the input terminal from entering a high impedance state.

In the SED1565 Series, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply a "L" signal to the $\overline{RES}$ terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the $\overline{RES}$ terminal is "L," the display timing generator circuit is stopped, and the FR, FRS, and $\overline{DOF}$ terminals are fixed to "H" and the CL pin is fixed to "H" only when the internal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

COMMANDS

The SED1565 Series chips identify the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{RD}$ terminal for reading, and inputting a low pulse to the $\overline{WR}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/$\overline{W}$ terminal and placed in a write mode when a "L" signal is input to the R/$\overline{W}$ terminal and then the command is launched by inputting a high pulse to the E terminal. (See "10. Timing Characteristics" regarding the timing.) Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read $\overline{RD}$ (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the page address circuit in the Function Description (page 1–20) for the detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a $\overline{RES}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (page 1–20) for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the (20) Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Select Status				
											SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.

• The sequence for cursor display

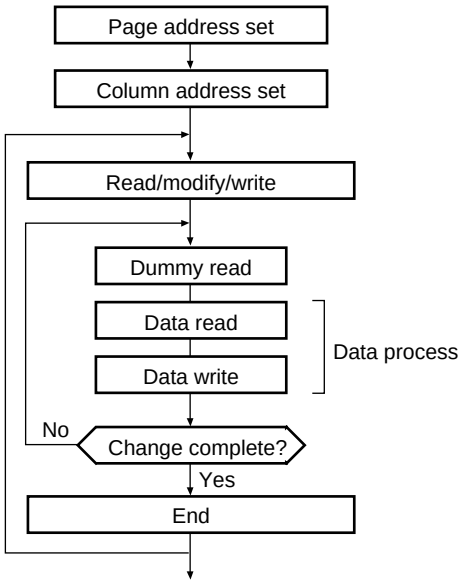


Figure 24

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

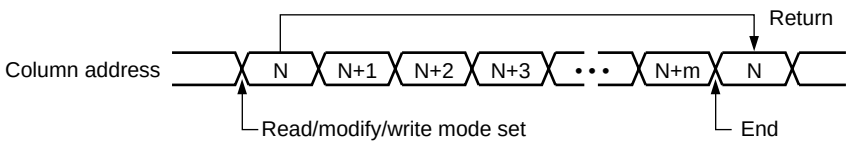


Figure 25

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		Selected Mode				
												SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

[Translator's Note: the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

V_5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the function explanation is "The Power Supply Circuits."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V_5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

• The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

* Inactive bit

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

• The Electronic Volume Register Set Sequence

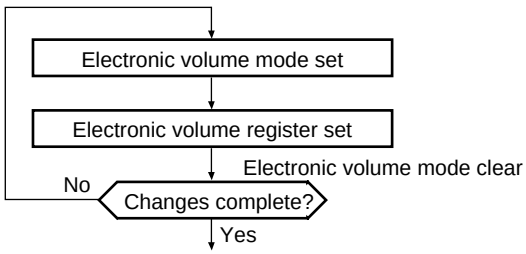


Figure 26

Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

• Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit

• Static Indicator Register Set Sequence

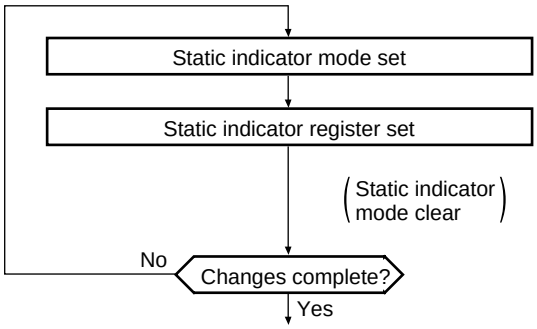


Figure 27

Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 26 for power save off sequence.

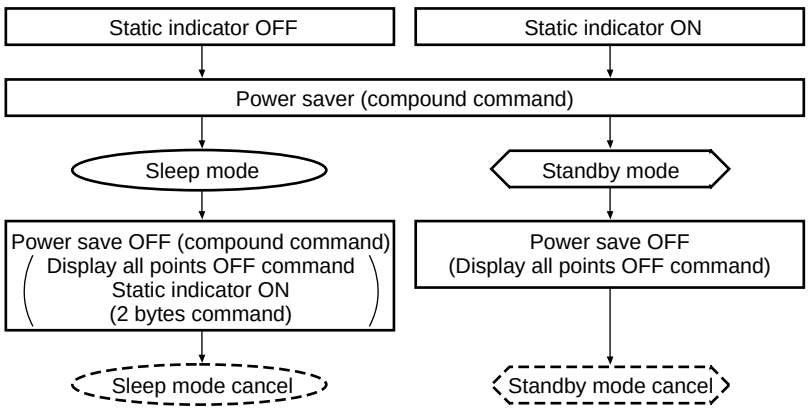


Figure 28

• Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

① The oscillator circuit and the LCD power supply circuit are halted.
② All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

• Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.
② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The SED1565 series chips have a liquid crystal display blanking control terminal $\overline{DOF}$. This terminal enters an "L" state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

NOP

Non-OPeration Command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the $\overline{RES}$ input by the reset command or by using an NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

Note: The SED1565 Series chips maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the SED1565 Series chip. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16 Table of SED1565 Series Commands

	Command	Command Code A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED1565*** ..... 0: 1/9, 1: 1/7 SED1566*** ..... 0: 1/8, 1: 1/6 SED1567*** 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command
(23)	Test mode reset	0	1	0	1	1	1	1	0	0	0	0	Enter during the refresh sequence.

(Note) *: disabled data

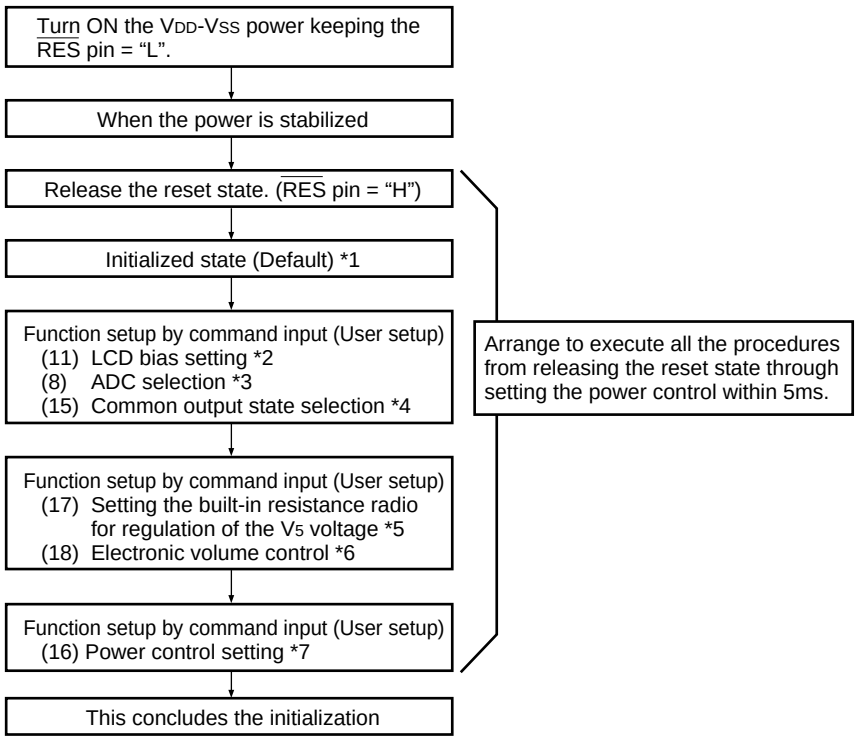
COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins ($V_1 \sim V_5$) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

① When the built-in power is being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

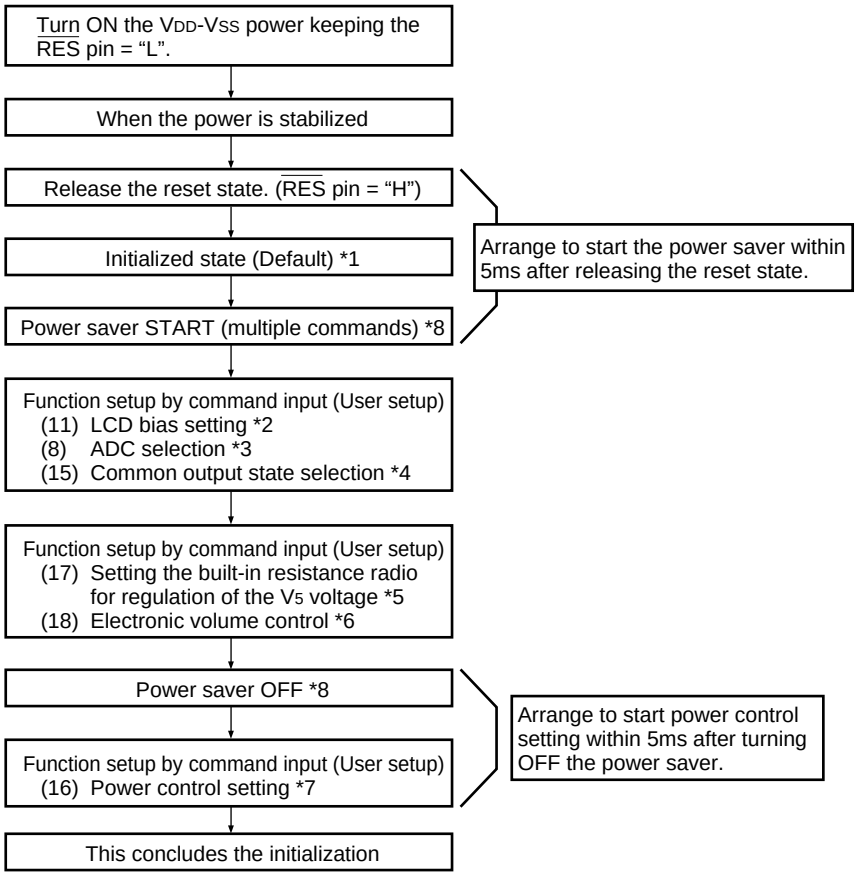
Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting

COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

② When the built-in power is not being used immediately after turning on the power:

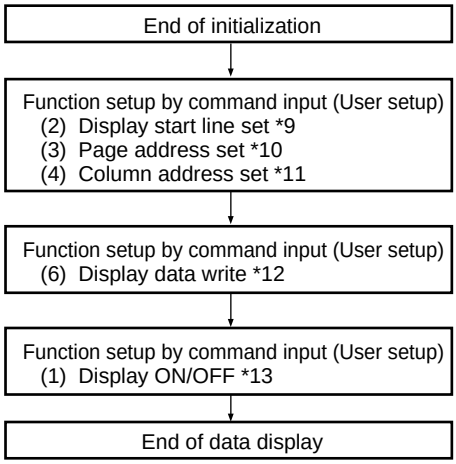


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

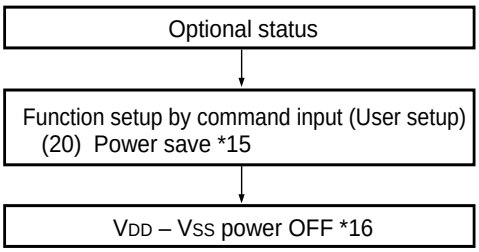
*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting
*8: The power saver ON state can either be in sleep state or stand-by state.
Command description; Power saver START (multiple commands)

(2) Data Display



Notes: Reference items
*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF

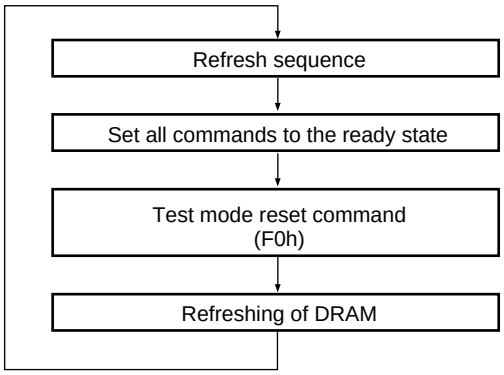
(3) Power OFF *14



Notes: Reference items
*14: After turning OFF the internal power supply, turn OFF the power supply of this IC. (Function Description — Power Supply Circuit)
When the power of this IC is turned OFF with the internal power supply is held in the ON status, since the status where the voltage is supplied, even though an only little, to the internal LCD drive circuit is still continued, it is feared to ill affect the display quality of the LCD panel. To avoid this, be sure to observe the power OFF sequence strictly.
*15: Command Description; Power save
*16: Do not hold RESET in the ON status when power supply is off.

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0 V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up With Quad step-up	V_{SS2}	–7.0 to +0.3 –6.0 to +0.3 –4.5 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C

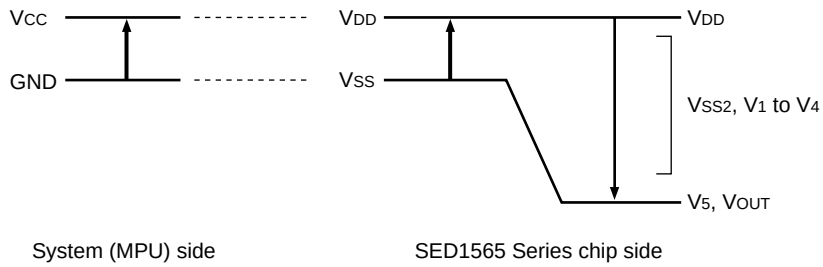


Figure 29

Notes and Cautions
1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	Recommended Voltage	V_{DD}		2.7	—	3.3	V	V_{DD}*1
	Possible Operating Voltage			1.8	—	5.5	V	V_{DD}*1
Operating Voltage (2)	Recommended Voltage	V_{SS2}	(Relative to V_{DD})	–3.3	—	–2.7	V	V_{SS2}
	Possible Operating Voltage	V_{SS2}	(Relative to V_{DD})	–6.0	—	–1.8	V	V_{SS2}
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to V_{DD})	–16.0	—	–4.5	V	V_5 *2
	Possible Operating Voltage	V_1, V_2	(Relative to V_{DD})	0.4 × V_5	—	V_{DD}	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to V_{DD})	V_5	—	0.6 × V_5	V	V_3, V_4
High-level Input Voltage		V_{IHC}		0.8 × V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}		V_{SS}	—	0.2 × V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA	V_{SS}	—	0.2 × V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –14.0 V	—	2.0	3.5	KΩ	SEGn
			V_5 = –8.0 V	—	3.2	5.4	KΩ	COMn *7
Static Consumption Current		I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output Leakage Current		I_{5Q}	V_5 = –18.0 V (Relative To V_{DD})	—	0.01	15	µA	V_5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz	—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C	18	22	26	kHz	*8
	External Input	f_{CL}	SED1565★★★/1567★★★	18	22	26	kHz	CL
	Internal Oscillator	f_{OSC}	Ta = 25°C	27	33	39	kHz	*8
	External Input	f_{CL}	SED1566★★★/1568★★★/1569★★★	14	17	20	kHz	CL

Table 19

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Internal Power	Input voltage	V_{SS2}	With Triple (Relative To V_{DD})		–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	With Quad (Relative To V_{DD})		–4.5	—	–1.8	V	V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{DD})		–18.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{DD})		–18.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to V_{DD})		–16.0	—	–4.5	V	V_5 *9
	Base Voltage	V_{REG0}	Ta = 25°C	–0.05%/°C	–2.04	–2.10	–2.16	V	*10
		V_{REG1}	(Relative to V_{DD})	–0.2%/°C	–4.65	–4.9	–5.15	V	*10

• Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
Current consumed by total ICs when an external power supply is used.

Table 20 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★★★	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	18	30	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	16	27		
SED1566★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	13	22		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	19		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	9	15		
SED1567★★★		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	8	13		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	7	12		
SED1568★★★/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
SED1569★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		

Table 21 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★★★	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	23	38	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	21	35		
SED1566★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	17	29		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	14	24		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
SED1567★★★		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	18		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		
SED1568★★★/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	15	25		
SED1569★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	13	22		

• Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Table 22 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SED1565★★★	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	67	112	µA	*12
			High-Power Mode	—	114	190		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	81	135		
			High-Power Mode	—	138	230		
SED1566★★★		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	35	59		
			High-Power Mode	—	64	107		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	43	72		
			High-Power Mode	—	84	140		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	72	121		
			High-Power Mode	—	128	214		
SED1567★★★		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	26	44		
			High-Power Mode	—	60	100		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	29	49		
			High-Power Mode	—	73	122		
SED1568★★★/		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	37	62		
SED1569★★★			High-Power Mode	—	67	112		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	46	77		
			High-Power Mode	—	87	145		

Table 23 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SED1565★★★	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	81	135	µA	*12
			High-Power Mode	—	127	212		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	96	160		
			High-Power Mode	—	153	255		
SED1566★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	41	69		
			High-Power Mode	—	71	119		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	51	85		
			High-Power Mode	—	92	154		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	85	142		
			High-Power Mode	—	142	237		
SED1567★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	32	53		
			High-Power Mode	—	62	103		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	73		
			High-Power Mode	—	89	148		
SED1568★★★/ SED1569★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	74		
			High-Power Mode	—	74	127		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	54	90		
			High-Power Mode	—	95	159		

• Consumption Current at Time of Power Saver Mode, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%

Table 24

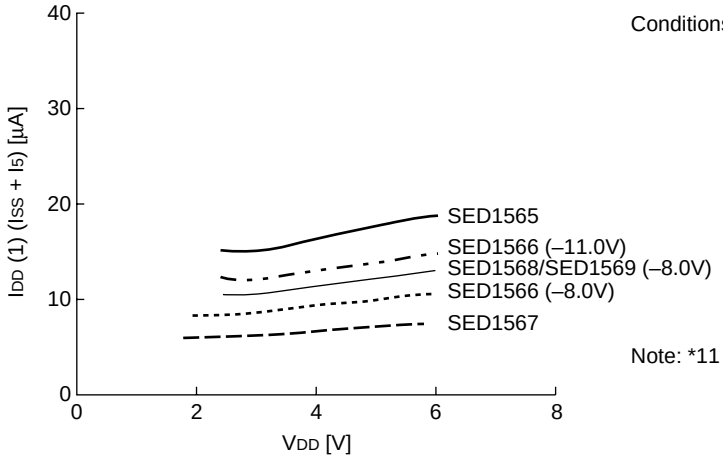
Ta = 25°C

Item		Symbol	Condition	Rating			Units	Notes
				Min.	Typ.	Max.		
Sleep mode	SED1565★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1565★★★	I_{DDS2}	—		4	8	µA	
Sleep mode	SED1566★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1566★★★	I_{DDS2}	—		4	8	µA	
Sleep mode	SED1567★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1567★★★	I_{DDS2}	—		3	6	µA	
Sleep mode	SED1568★★★/ SED1569★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1568★★★/ SED1569★★★	I_{DDS2}	—		4	8	µA	

TBD: To Be Determined

Reference Data 1

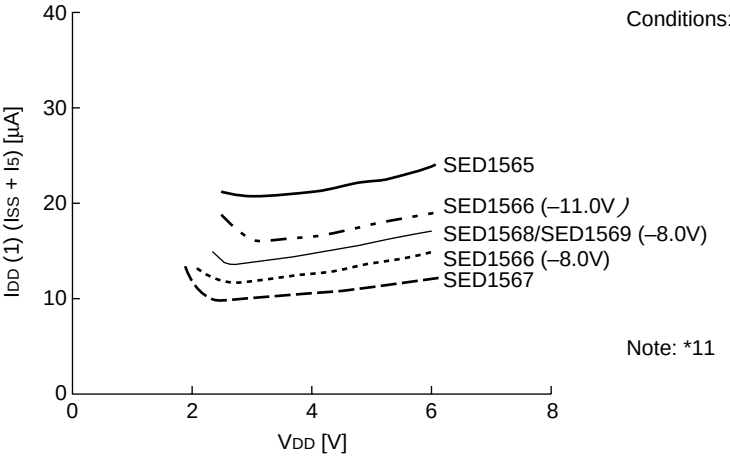
• Dynamic Consumption Current (1) During LCD Display Using an External Power Supply



Conditions: Internal power supply OFF
External power supply in use
SED1565/SED1566 (–11.0V):
$V_5 - V_{DD}$ = –11.0 V
SED1566 (–8.0V)/SED1567:
$V_5 - V_{DD}$ = –8.0 V
Display pattern: OFF
Ta = 25°C

Note: *11

Figure 30



Conditions: Internal power supply OFF
External power supply in use
SED1565/SED1566 (–11.0V):
$V_5 - V_{DD}$ = –11.0 V
SED1566 (–8.0V)/SED1567:
$V_5 - V_{DD}$ = –8.0 V
Display pattern: Checker
Ta = 25°C

Note: *11

Figure 31

Reference Data 2

- Dynamic Consumption Current (2) During LCD display using the internal power supply

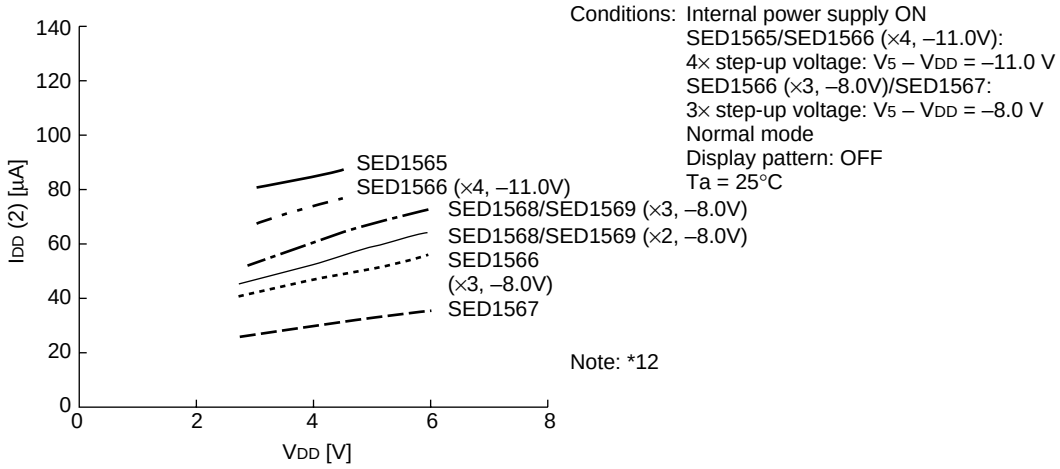


Figure 32

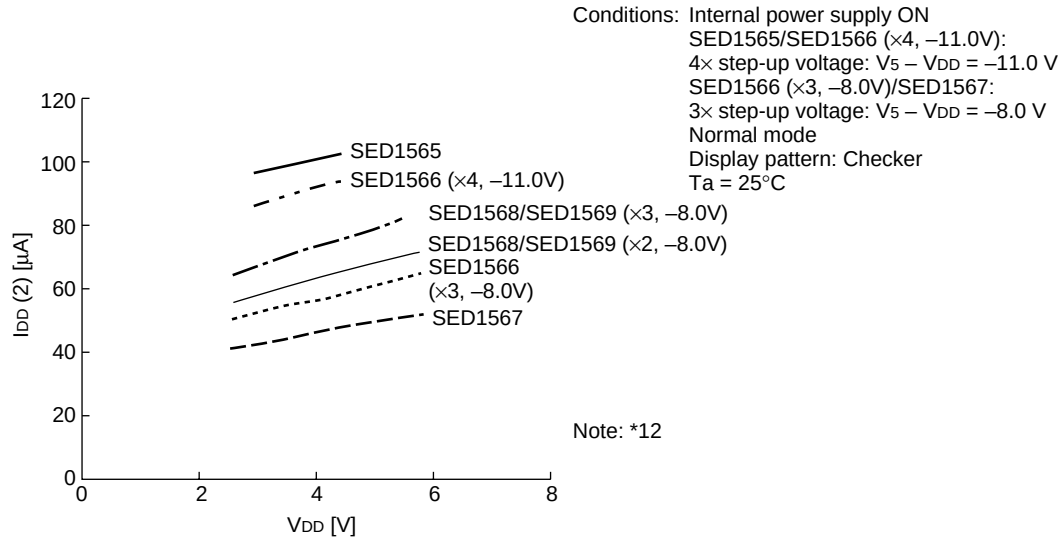
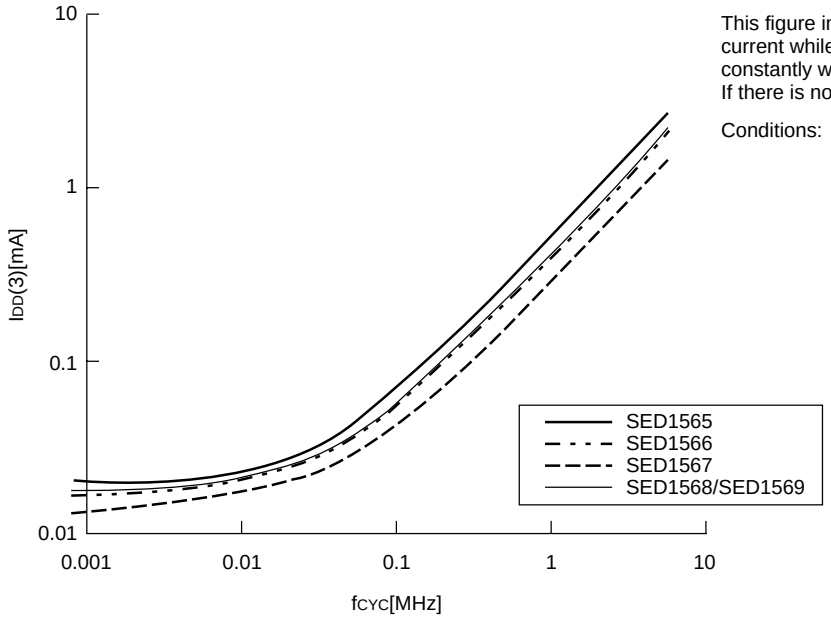


Figure 33

Reference Data 3

• Dynamic Consumption Current (3) During access



This figure indicates the consumption current while the checker pattern is constantly written through f_{CYC}.
If there is no access, then only (1) remains.

Conditions: Internal power supply OFF, external power supply used
SED1565:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–11.0 V
SED1566/SED1567:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–8.0 V
Ta = 25°C

Figure 34

Reference Data 4

• Operating voltage range of V_{SS} and V_5 systems

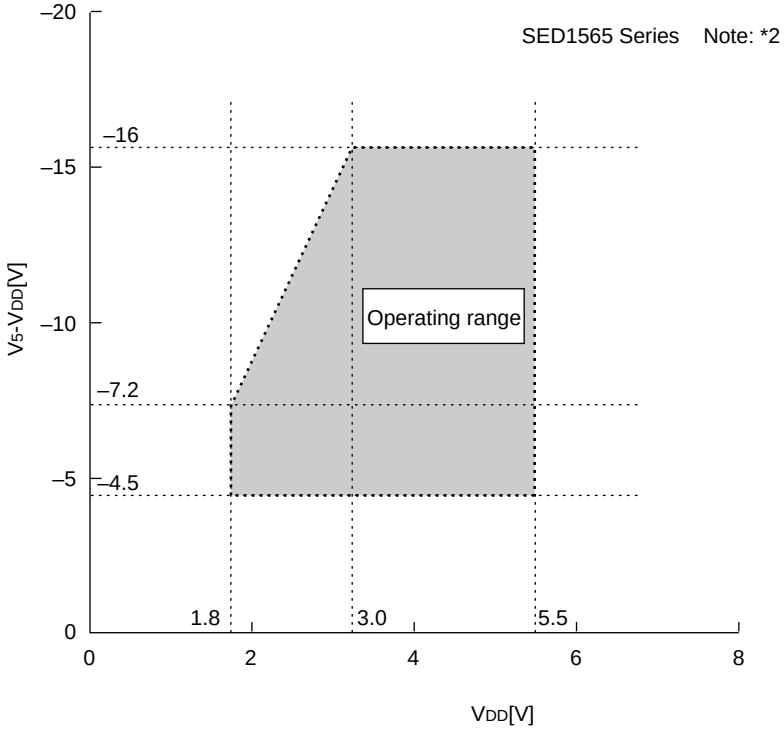


Figure 35

- The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 25

Item		f_{CL}	f_{FR}
SED1565***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4 \times 65}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{260}$
SED1566***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 49}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{196}$
SED1567***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 33}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{264}$
SED1568***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 55}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{220}$
SED1569***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 53}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{212}$

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{DD} system and the V_5 system is as shown in Figure 33. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*4 The D0 to D7, FR, FRS, $\overline{DOF}$, and CL terminals.

*5 The A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range.
R_{ON} = 0.1 V/Δ I (Where Δ I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 9-7 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the SED1565 Series chips, the temperature range can come in three types as V_{REG} options: (1) approximately –0.05%/°C, (2) –0.2%/°C, and (3) external input.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
The SED1565 is 1/9 biased, SED1566 is 1/8 biased and SED1567 is 1/6 biased.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

*12 It is the value on a model having the V_{REG} option temperature gradient is –0.05%/°C when the V_5 voltage regulator internal resistor is used.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

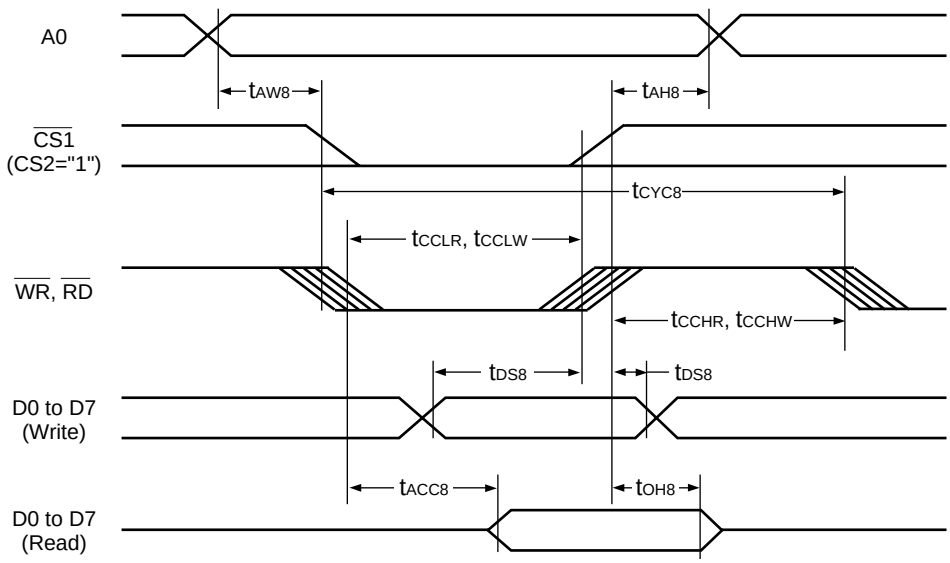


Figure 36

Table 26

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		166	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	ns
Data setup time	D0 to D7	t_{DS8}		30	—	ns
Address hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	70	ns
Output disable time		t_{OH8}		5	50	ns

Table 27

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

Table 28

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		1000	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Address hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

System Bus Read/Write Characteristics 2 (6800 Series MPU)

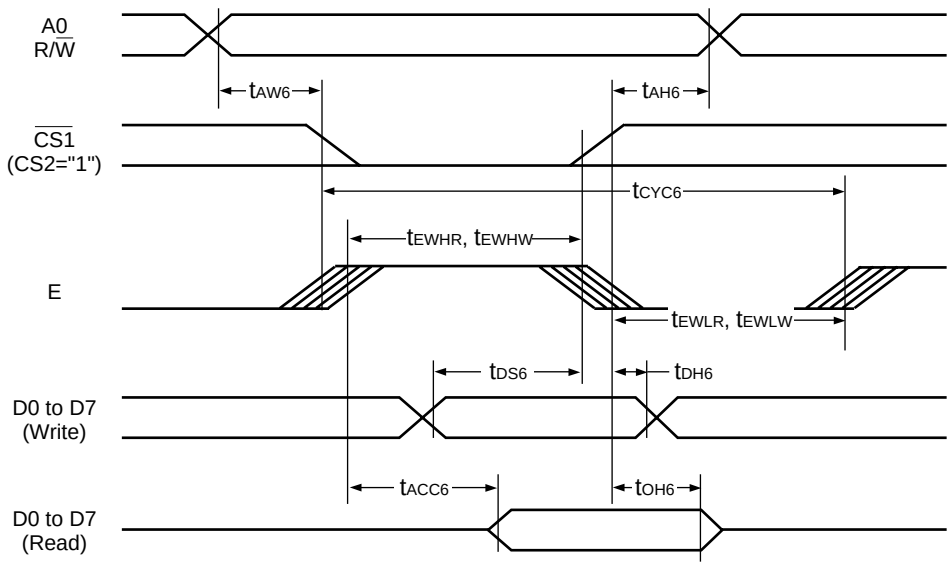


Figure 37

Table 29

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		166	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		30 10	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	70 50	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		70 30	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		30 30	— —	ns ns

Table 30

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		300	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	140 100	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

Table 31

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		1000	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	280 200	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

The Serial Interface

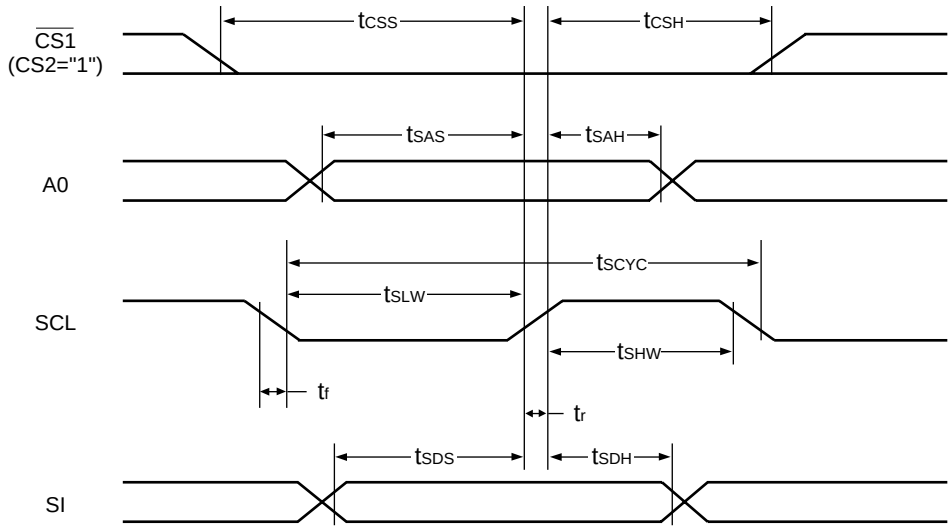


Figure 38

Table 32

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		200	—	ns
SCL “H” pulse width		t_{SHW}		75	—	ns
SCL “L” pulse width		t_{SLW}		75	—	ns
Address setup time	A0	t_{SAS}		50	—	ns
Address hold time		t_{SAH}		100	—	ns
Data setup time	SI	t_{SDS}		50	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}		100	—	ns
		t_{CSH}		100	—	ns

Table 33

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		250	—	ns
SCL “H” pulse width		t_{SHW}		100	—	ns
SCL “L” pulse width		t_{SLW}		100	—	ns
Address setup time	A0	t_{SAS}		150	—	ns
Address hold time		t_{SAH}		150	—	ns
Data setup time	SI	t_{SDS}		100	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		150	—	ns
		t_{CSH}		150	—	ns

Table 34

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL “H” pulse width		t_{SHW}		150	—	ns
SCL “L” pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Display Control Output Timing

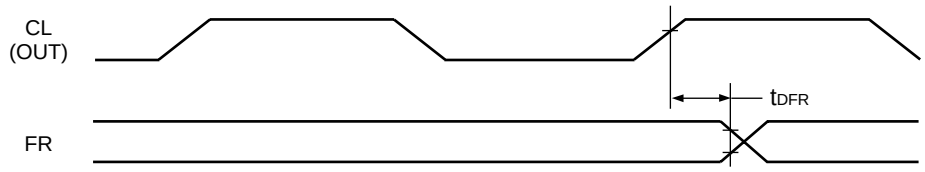


Figure 39

Table 35

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	10	40	ns

Table 36

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	20	80	ns

Table 37

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timing is based on 20% and 80% of V_{DD}.

Reset Timing

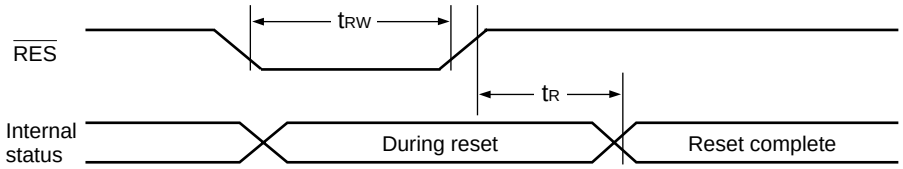


Figure 40

Table 38

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	0.5	µs
Reset “L” pulse width	RES	t_{RW}		0.5	—	—	µs

Table 39

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	1	µs
Reset “L” pulse width	RES	t_{RW}		1	—	—	µs

Table 40

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	1.5	µs
Reset “L” pulse width	RES	t_{RW}		1.5	—	—	µs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

THE MPU INTERFACE (REFERENCE EXAMPLES)

The SED1565 Series can be connected to either 80 × 86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the SED1565 series chips with fewer signal lines.
The display area can be enlarged by using multiple SED1565 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

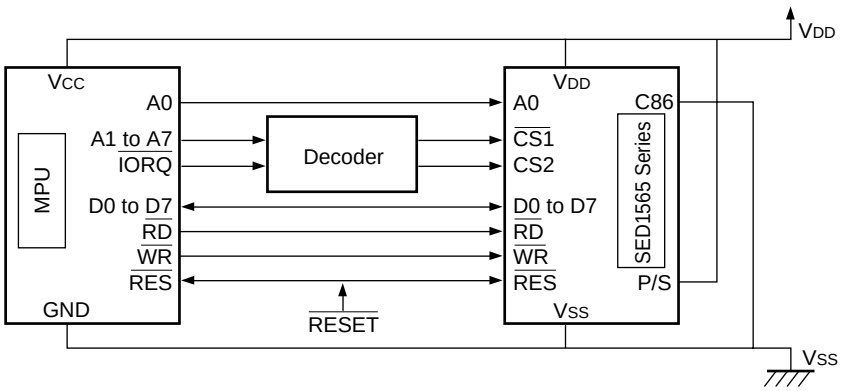


Figure 41-1

(2) 6800 Series MPUs

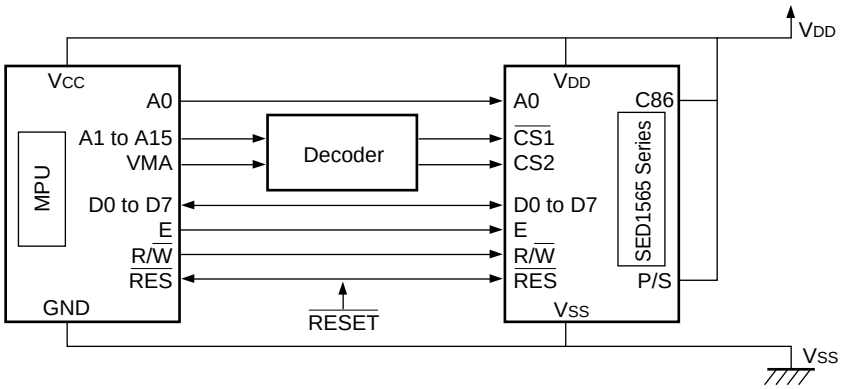


Figure 41-2

(3) Using the Serial Interface

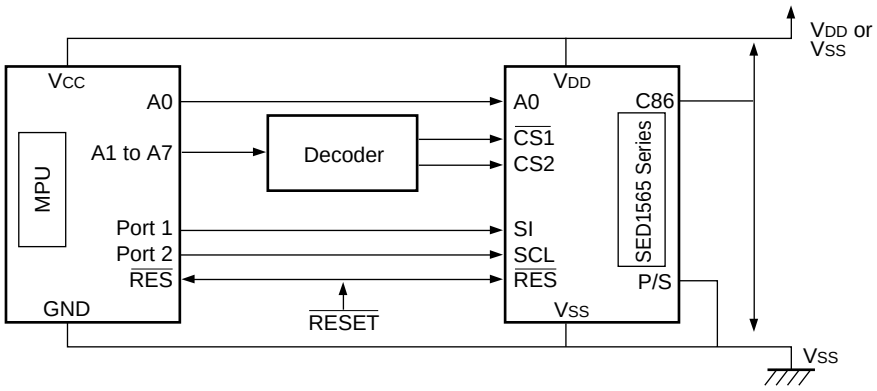


Figure 41-3

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The liquid crystal display area can be enlarged with ease through the use of multiple SED1565 Series chips. Use a same equipment type.

(1) SED1565 (master) ↔ SED1565 (slave)

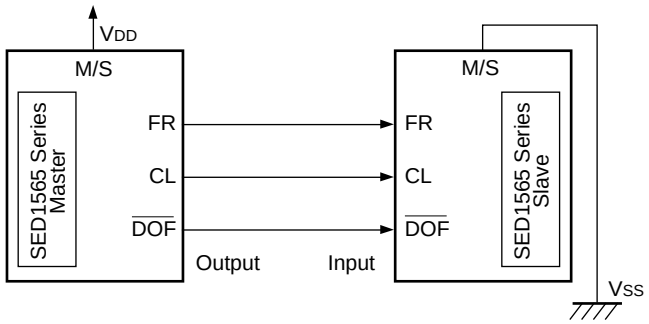


Figure 42

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLES)

The liquid crystal display area can be enlarged with ease through the use of multiple SED1565 Series chips. Use a same equipment type, in the composition of these chips.

(1) Single-chip Structure

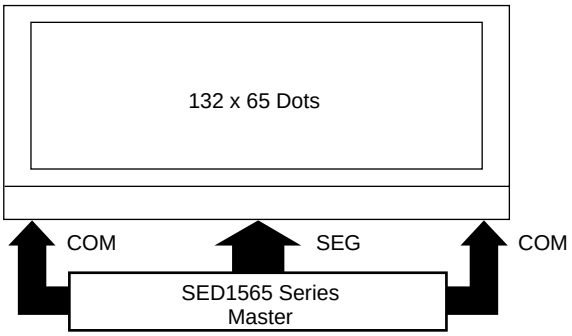


Figure 43-1

(2) Double-chip Structure, #1

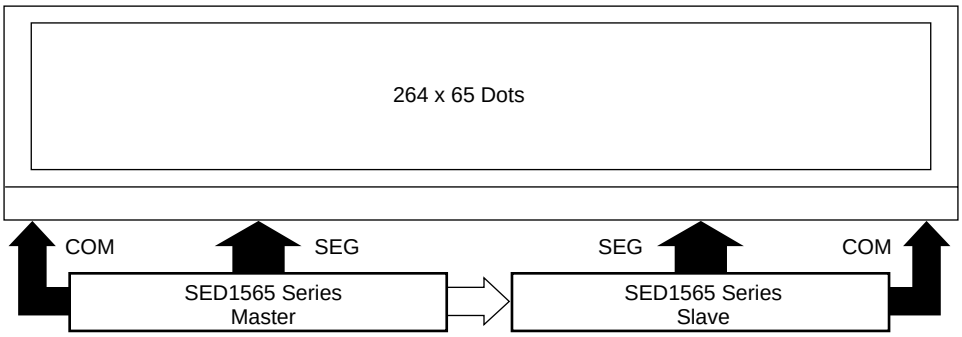
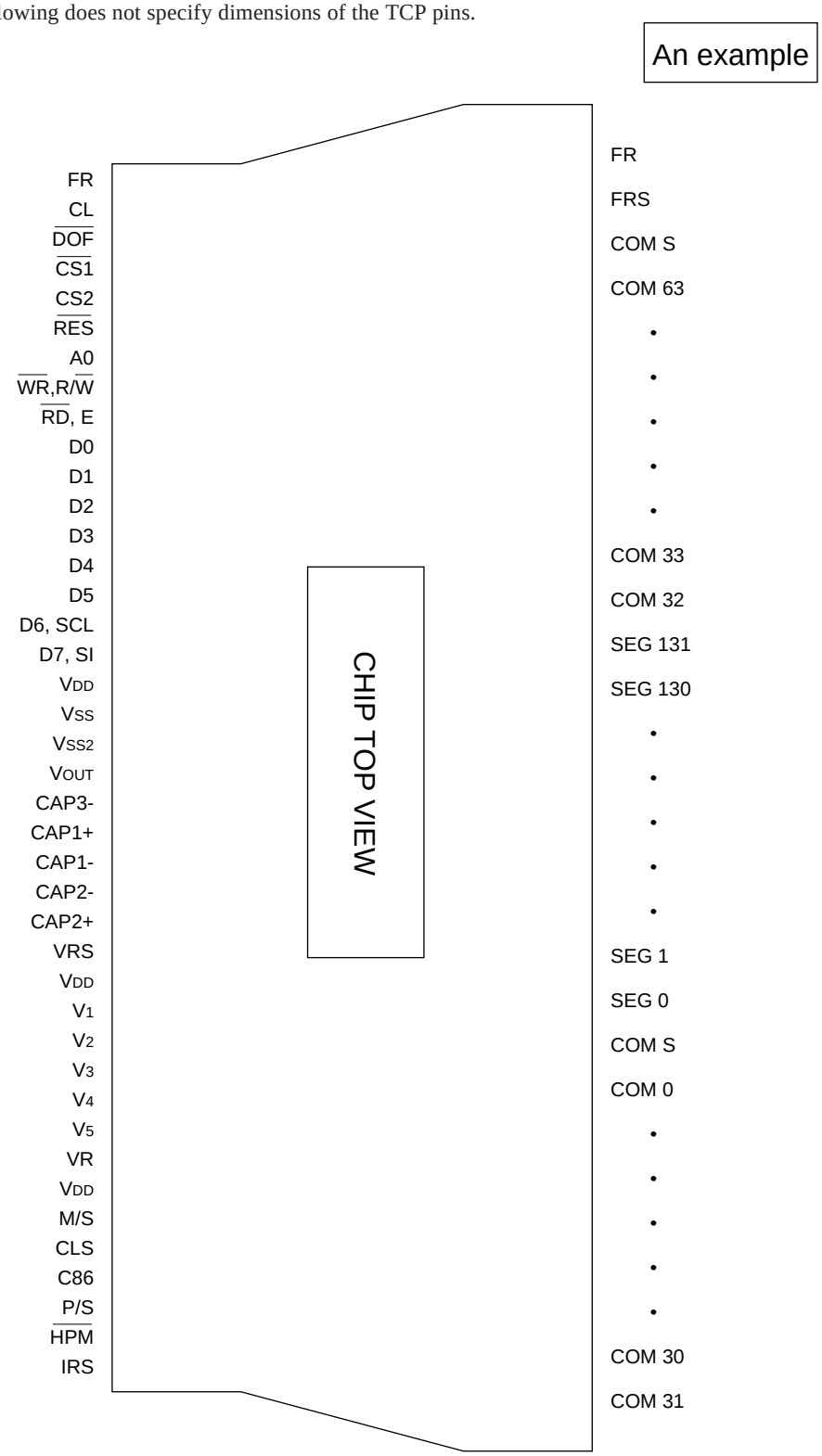


Figure 43-2

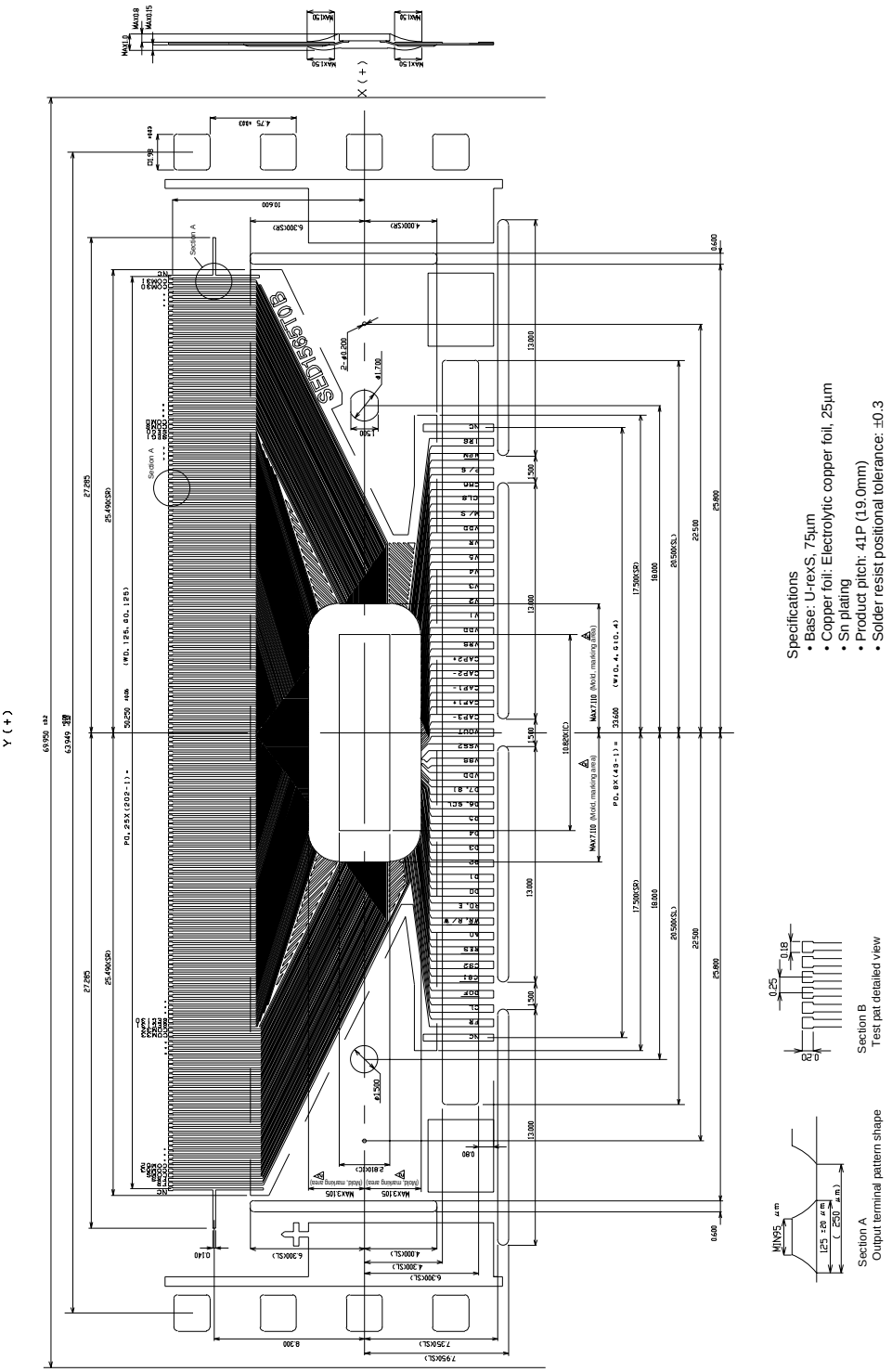
A SAMPLE TCP PIN ASSIGNMENT

SED1565T0B TCP Pin Layout

Note: The following does not specify dimensions of the TCP pins.



EXTERNAL VIEW OF TCP PINS



NOTICE

Please be advised on the following points in the use of this development manual.

1. This manual is subject to change without previous notice.
2. This manual does not guarantee or furnish the industrial property right nor its execution.
   Application examples in the manual are intended to ensure your better understanding of the product. Thus, the manufacturer shall not be liable for any trouble arising in your circuits from using such application example.
   Numerical values provided in the property table of this manual are represented with their magnitude on the numerical line.
3. No part of this manual may not be reproduced, copied or used for commercial purposes without a written permission from the manufacturer.

In handling of semiconductor devices, your attention is required to the following points.

[Precautions on Light]

Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs mounted on the boards or products, make sure that:

(1) Your design and mounting layout done are so that the IC is not exposed to light in actual use.
(2) The IC is protected from light in the inspection process.
(3) The IC is protected from light in its front, rear and side faces.

9. SED1570 Series

Contents

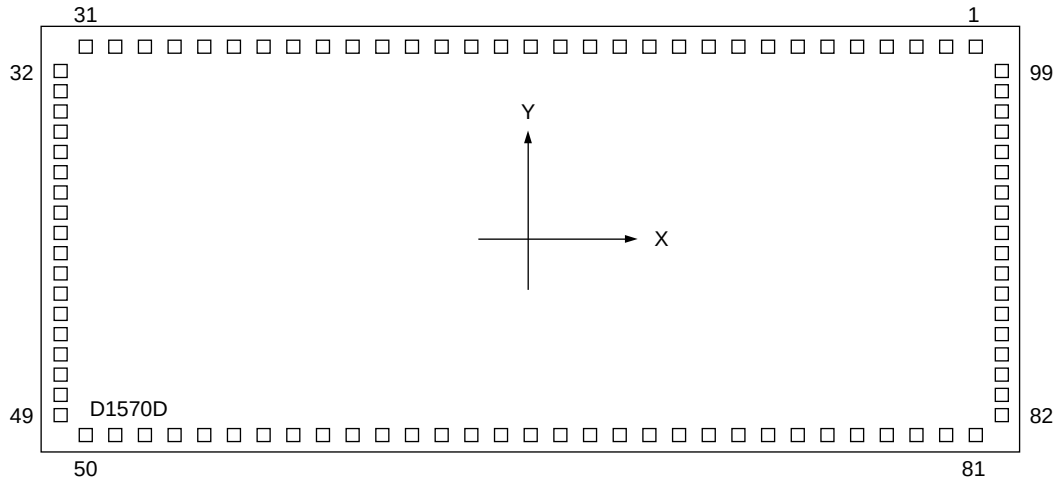
GENERAL DESCRIPTION

The SED1570 is an 80 output segment (column) driver with an internal display RAM. This drive is suitable for driving a dot matrix LCD panel; from a mid-range capacity dot matrix LCD panel to a CGA class dot matrix LCD panel. This device is used with the SED1635.
The display data is stored in the internal display RAM and an LCD panel drive signal is generated. As a result, this device allows configuration of an ultra low power display system since the display data is not transferred unless the display is changed.
In addition, the logic power is low voltage; a wide range of applications is possible.

FEATURES

- Display duty cycle: 1/64 – 1/200
- LCD driver output: 80 out
- Internal display RAM: 200 × 80 bits
- Slim chip
- Ultra low power consumption
- Power $V_{DD} - V_{SS}$ 2.7 V to 5.5 V
  $V_{DD} - V_{EE}$ 8.0 V to 20 V
- High speed and low power date transfer by the 4-bit bus enables chain method
- Non-bias display off function
- Output shift direction-pin selection
- Adjustable LCD power offset bias for V_{DD} level
- Package Chip SED1570D0A (Al pad)
  SED1570D0B (Au bump)

PAD DIMENSIONS



Chip Size	8.04 mm × 3.51 mm
Pad Center Size	100 µm × 100 µm
Pad Pitch	170 µm (Min.)
Chip Thickness	400 µm ±25 µm (Al Pad)
Bump Size	92 µm × 82 µm
Pump Pitch	170 µm (Min.)
Chip Thickness	525 µm
Bump Height	17~28 µm (reference)

PAD COORDINATES

SED1570 Pad Center Coordinates (Al-pad)

Unit: μm

PAD No	PIN Name	X	Y
1	X 75	3640	1595
2	X 76	3432	1595
3	X 77	3224	1595
4	X 78	3016	1595
5	X 79	2808	1595
6	X 80	2600	1595
7	EIO2	2340	1595
8	V_{DD}	2080	1595
9	SHL	1820	1595
10	D_0	1560	1595
11	D_1	1300	1595
12	D_2	1040	1595
13	D_3	780	1595
14	YD	520	1595
15	V_{EE}	260	1595
16	V_5	0	1595
17	V_3	–260	1595
18	V_2	–520	1595
19	V_0	–780	1595
20	FR	–1040	1595
21	XSCL	–1300	1595
22	$\overline{DOFF}$	–1560	1595
23	LP	–1820	1595
24	V_{SS}	–2080	1595
25	EIO1	–2340	1595
26	X 1	–2600	1595
27	X 2	–2808	1595
28	X 3	–3016	1595
29	X 4	–3224	1595
30	X 5	–3432	1595
31	X 6	–3640	1595
32	X 7	–3862	1452
33	X 8	–3862	1282
34	X 9	–3862	1112
35	X 10	–3862	942
36	X 11	–3862	772
37	X 12	–3862	602
38	X 13	–3862	432
39	X 14	–3862	262
40	X 15	–3862	92

PAD No	PIN Name	X	Y
41	X 16	–3862	–78
42	X 17	–3862	–248
43	X 18	–3862	–418
44	X 19	–3862	–588
45	X 20	–3862	–758
46	X 21	–3862	–928
47	X 22	–3862	–1098
48	X 23	–3862	–1268
49	X 24	–3862	–1438
50	X 25	–3641	–1595
51	X 26	–3406	–1595
52	X 27	–3171	–1595
53	X 28	–2936	–1595
54	X 29	–2701	–1595
55	X 30	–2466	–1595
56	X 31	–2231	–1595
57	X 32	–1996	–1595
58	X 33	–1761	–1595
59	X 34	–1526	–1595
60	X 35	–1291	–1595
61	X 36	–1056	–1595
62	X 37	–821	–1595
63	X 38	–586	–1595
64	X 39	–351	–1595
65	X 40	–116	–1595
66	X 41	119	–1595
67	X 42	354	–1595
68	X 43	589	–1595
69	X 44	824	–1595
70	X 45	1059	–1595
71	X 46	1294	–1595
72	X 47	1530	–1595
73	X 48	1765	–1595
74	X 49	2000	–1595
75	X 50	2235	–1595
76	X 51	2470	–1595
77	X 52	2705	–1595
78	X 53	2940	–1595
79	X 54	3175	–1595
80	X 55	3410	–1595

PAD No	PIN Name	X	Y
81	X 56	3645	–1595
82	X 57	3862	–1438
83	X 58	3862	–1268
84	X 59	3862	–1098
85	X 60	3862	–928
86	X 61	3862	–758
87	X 62	3862	–588
88	X 63	3862	–418
89	X 64	3862	–248
90	X 65	3862	–78
91	X 66	3862	92
92	X 67	3862	262
93	X 68	3862	432
94	X 69	3862	602
95	X 70	3862	772
96	X 71	3862	942
97	X 72	3862	1112
98	X 73	3862	1282
99	X 74	3862	1452

(Au-bump) Unit: µm

PAD No	PIN Name	X	Y
1	X 75	3640	1601
2	X 76	3432	
3	X 77	3224	
4	X 78	3016	
5	X 79	2808	
6	X 80	2600	
7	EIO2	2340	
8	V_{DD}	2080	
9	SHL	1820	
10	D_0	1560	
11	D_1	1300	
12	D_2	1040	
13	D_3	780	
14	YD	520	
15	V_{EE}	260	
16	V_5	0	
17	V_3	–260	
18	V_2	–520	
19	V_0	–780	
20	FR	–1040	
21	XSCL	–1300	
22	$\overline{DOFF}$	–1560	
23	LP	–1820	
24	V_{SS}	–2080	
25	EIO1	–2340	
26	X 1	–2600	
27	X 2	–2808	
28	X 3	–3016	
29	X 4	–3224	
30	X 5	–3432	
31	X 6	–3640	
32	X 7	–3868	1452
33	X 8		1282
34	X 9		1112
35	X 10		942
36	X 11		772
37	X 12		602
38	X 13		432
39	X 14		262
40	X 15		92

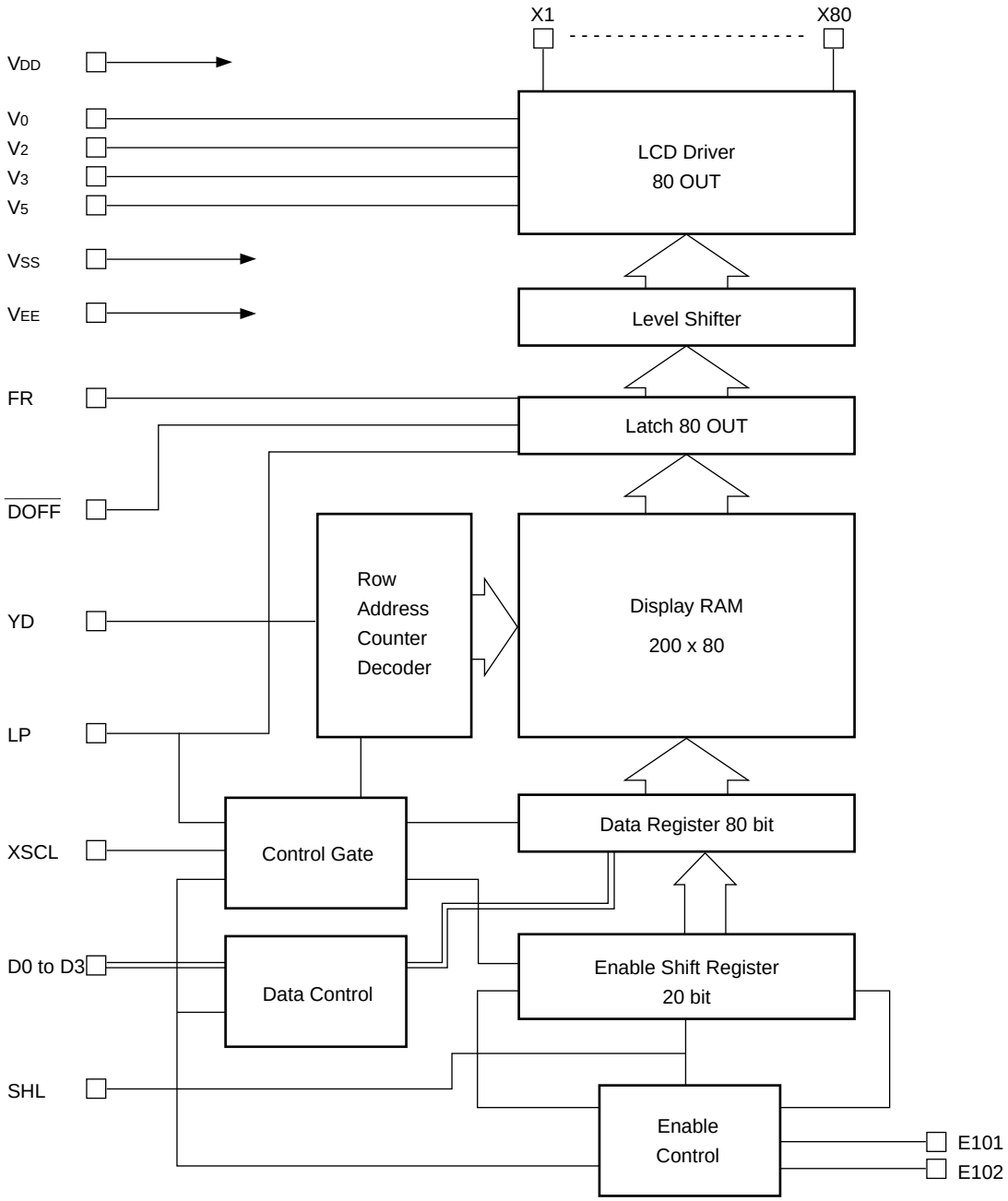
PAD No	PIN Name	X	Y
41	X 16	–3868	–78
42	X 17		–248
43	X 18		–418
44	X 19		–588
45	X 20		–758
46	X 21		–928
47	X 22		–1098
48	X 23		–1268
49	X 24		–1438
50	X 25	–3641	–1601
51	X 26	–3406	
52	X 27	–3171	
53	X 28	–2936	
54	X 29	–2701	
55	X 30	–2466	
56	X 31	–2231	
57	X 32	–1996	
58	X 33	–1761	
59	X 34	–1526	
60	X 35	–1291	
61	X 36	–1056	
62	X 37	–821	
63	X 38	–586	
64	X 39	–351	
65	X 40	–116	
66	X 41	119	
67	X 42	354	
68	X 43	589	
69	X 44	824	
70	X 45	1059	
71	X 46	1294	
72	X 47	1530	
73	X 48	1765	
74	X 49	2000	
75	X 50	2235	
76	X 51	2470	
77	X 52	2705	
78	X 53	2940	
79	X 54	3175	
80	X 55	3410	

PAD No	PIN Name	X	Y
81	X 56	3645	–1601
82	X 57	3868	–1438
83	X 58		–1268
84	X 59		–1098
85	X 60		–928
86	X 61		–758
87	X 62		–588
88	X 63		–418
89	X 64		–248
90	X 65		–78
91	X 66		92
92	X 67		262
93	X 68		432
94	X 69		602
95	X 70		772
96	X 71		942
97	X 72		1112
98	X 73		1282
99	X 74		1452

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>X1 – X80</td><td>O</td><td>LCD drive segment (column) output
The output changes with the LP's trailing edge.</td><td>80</td></tr>
<tr><td>D_0 – D_3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Display data shift clock input
Reads the display data (D_0 – D_3) into the data register with a trailing edge.</td><td>1</td></tr>
<tr><td>LP</td><td>I/O</td><td>Display data latch clock input
• The display RAM data (specified by the low address shift register) is read into the latch with a leading edge, and the LCD display data is output.
• For a specified low address, the contents of the write register are written in the display RAM. (At Data transfer mode)
• Resets the enable control circuit.</td><td>1</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O</td><td>Enable I/O
• Configured by SHL.
• Output is reset to "H" by LP input. When the 80 bit display data is read, the output falls to "L" automatically.
• To connect in cascade format, connect these pins to the next level EIO.</td><td>2</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction and input/output select input
• If the display data is entered in the input (D_3, D_2, D_1, D_0) in the order of (a1, a2, a3, a4) (b1, b2, b3, b4) … (t1, t2, t3, t4), the relationship of the display data and the segment output is as given in the table below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="12">Xn (SEG output)</th><th colspan="2">EIO</th></tr>
<tr><th>80</th><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>…</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a1</td><td>a2</td><td>a3</td><td>a4</td><td>b1</td><td>b2</td><td>…</td><td>s3</td><td>s4</td><td>t1</td><td>t2</td><td>t3</td><td>t4</td><td>O</td><td>I</td></tr>
<tr><td>H</td><td>t4</td><td>t3</td><td>t2</td><td>t1</td><td>s4</td><td>s3</td><td>…</td><td>b2</td><td>b1</td><td>a4</td><td>a3</td><td>a2</td><td>a1</td><td>I</td><td>O</td></tr>
</table></td><td>1</td></tr>
<tr><td>$\overline{DOFF}$</td><td>I</td><td>Forced blank input
In the "L" level, the segment output is forced to the V0 level.
The display RAM data is maintained.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>LCD AC drive signal input</td><td>1</td></tr>
<tr><td>YD</td><td>I</td><td>Scan start input
• Rests the low address counter decoder.
• The number of scanned lines (number of low addresses) for the display RAM is determined by the number of LP pulses, which are input in one YD cycle.</td><td>1</td></tr>
<tr><td>V_0, V_2, V_3, V_5</td><td>Power supply</td><td>LCD drive power input
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$</td><td>4</td></tr>
<tr><td>V_{EE}</td><td>Power supply</td><td>LCD drive power input V_{DD} – V_{EE}</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power input
V_{DD}: connect to the system V_{CC} pin.
V_{SS}: connect to the system GND.</td><td>2</td></tr>
</table>

BLOCK DIAGRAM



BLOCK DESCRIPTION

Enable Shift Register

The order of the display data latched is reversed by the SHL input.

Enable Control and Data Control

If the enable signal is disabled (EIO = "H"), the internal clock signal and the data bus are fixed to "L". This is a power-save mode.
To use multiple segment drivers, connect in cascade format the EIO pin of each driver, and connect the EIO pin of the first driver to the "V_{SS}" pin.
The enable control circuit automatically detects when the 80 bit data has been read and automatically transfers the enable signal. As a result, a control signal by a control LSI is not necessary.

Display RAM

This is a static RAM (200 × 80 bits) that stores the LCD data.
The display RAM data (80 bit) for the low address is read out to the latch with the trailing edge of the LP signal. In addition, with the trailing edge of the LP signal, the contents of the data register is moved to the write register. The contents of the write register are then written in the display RAM area for the low address. The low address is then incremented.
If the XSCL signal does not come in after the trailing edge of the LP signal, the mode is changed to the self-refresh mode. The write register does not write data in the display RAM and the low address is incremented. The mode is then changed to the read out mode to read the next line.

Low Address Counter Decoder

This selects a line of the display RAM in sequence. This decoder catches the "H" of the YD signal at the trailing edge of the LP signal, and resets the low address counter. It then initialize the selected address of the display RAM. In a normal operation, the decoder is incremented after the writing operation into the display RAM. (The writing operation is caused by the trailing edge of the LP signal.) In the self-refresh mode, the decoder is incremented without the writing operation into the display RAM.

Data Register

This 80 bit register controls the write operation into the display RAM. The data is written in the display RAM with the trailing edge of the LP signal. In the self-refresh mode, the data is not written in the display RAM.

Control Circuit

The control circuit detects the self-refresh mode, allows the write register to write the data into the display RAM, and controls and low address count signal.

Latch

This reads the 80 bit data for the low address of the display RAM with the trailing edge of the LP signal, and sends the output signal to the level shifter.

Level Shifter

This is the level interface circuit that converts the signal voltage level from $V_{DD} – V_{SS}$ to $V_{DD} – V_{EE}$ (LCD driver power).

LCD Driver

The LCD driver outputs the LCD driver voltage.
The table below shows the relationship between the display signals ($D_3 – D_0$), LCD AC-drive wave form (FR) and the segment output voltage.

$\overline{DOFF}$	$D_0 – D_3$	FR	X Output Voltage
H	H	H	V_0
		L	V_5
	L	H	V_2
		L	V_3
L	—	—	V_0

Self-Refresh Function

Setting self-refresh mode

The self-refresh mode functions as follows: if the displayed contents do not change, there is no transfer of the display data from the display controller to the SED1570. The SED1570 automatically detects this and power-down is displayed.

The SED1570 is set to the self-refresh mode by maintaining the shift clock (XSCLK) in the "L" level for 1 horizontal display period (LP signal cycle) after the row data for 1 line has been input. The SED1570 checks the mode (whether or not the mode is changed to the self-refresh mode) every 1 horizontal display period. During 1 horizontal display period in which XSCL stops working, the display data is not written into the SED1570 display RAM.

To stop XSCL, terminate display data (D0 – D3) transfer from the display controller (because of the power down), and set XSCL to "H" or "L". At this time, the display control must periodically send the LP, YD, and FR signals to the SED1570 the same way as when data is transferred. The SED1570 inputs these signals, reads the display data periodically from the internal display RAM and refreshes the display.

The display-off function is available in the self-refresh mode.

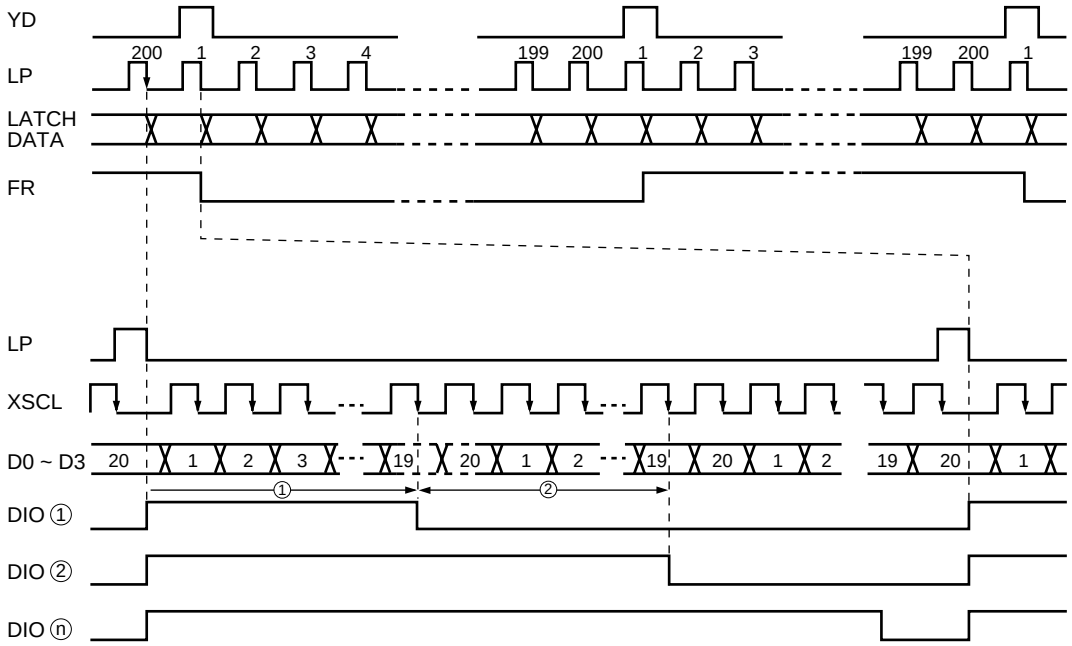
Canceling self-refresh mode

The self-refresh mode is canceled as follows: The display controller inputs the shift clock (XSCL) into the SED1570 for one horizontal display period or longer. This should be down with the trailing edge of the LP signal and in the data transfer timing. After the mode is canceled, the line data, which has been sent in the horizontal display period, is written in the display RAM at the time of the next trailing edge of the LP signal.

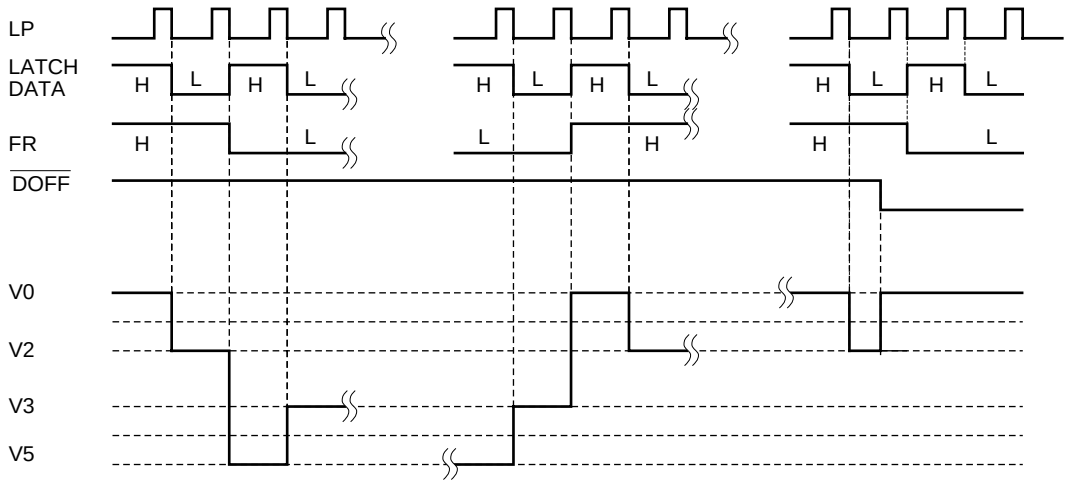
If the SED1570s are connected in cascade format, the self-refresh modes of all SED1570s are not canceled unless the appropriate number of the XSCL clocks for the cascaded SED1570s are entered.

Timing Diagram

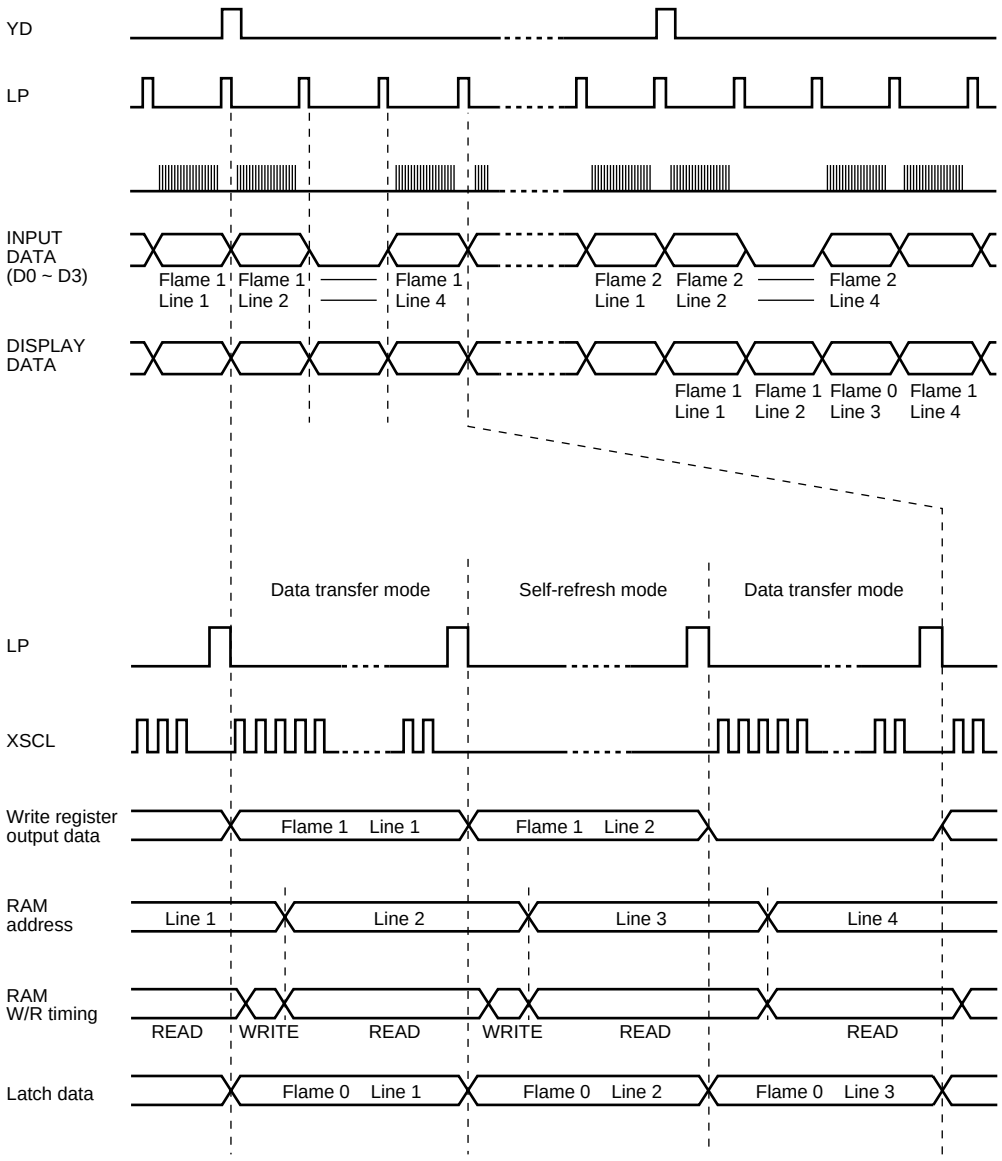
Sample of 1/200 duty



① ~ ⓝ serial conection number of Driver IC



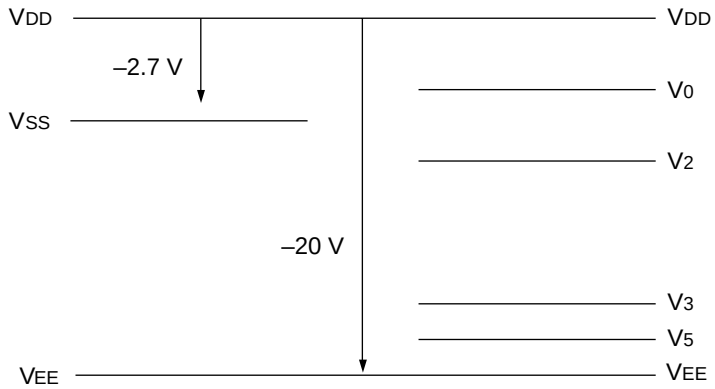
Self-refresh mode timing



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{SS}	–7.0 to +0.3	V
Supply voltage 2	V_{EE}	–22.0 to +0.3	V
Supply voltage 3	V_0, V_2, V_3, V_5	V_{EE} –0.3 to V_{DD} +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I01	20	mA
Operating temperature	Topr	–40 to +85	deg. C
Storage temperature 1	Tstg1	–65 to +150	deg. C
Storage temperature 2	Tstg2	–55 to +100	deg. C

Notes: 1. All voltages are given relative to V_{DD} = 0 V.
2. For storage temperature 1 – Plastic package
For storage temperature 2 – TAB mounted
3. V_0, V_2, V_3, and V_5 must satisfy the condition
$V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$



4. If the logic power is being floated or if the Vss voltage exceeds -2.5 Vdc during LCD power-on, the LSI chips may be damaged permanently. Take care not to damage the chips especially in the system power on/off sequence.

ELECTRICAL CHARACTERISTICS

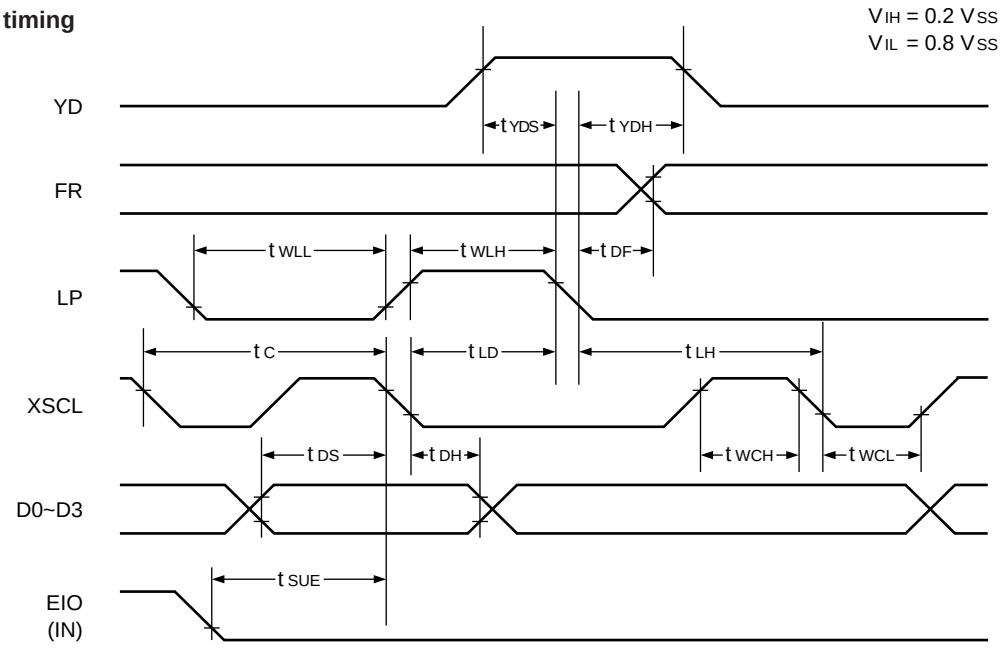
DC Characteristics

V_{DD} = V_0 = 0 V, V_{SS} = –5.0 V ±10%, Ta = –40 to 85°C

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin
Supply voltage (1)		V_{SS}			–5.5	–5.0	–2.7	V	V_{SS}
Recommended operation voltage		V_{EE}	V_{SS} = –2.7 to –5.5V		–20.0		–8.0	V	V_{EE}
Supply voltage (2)		V_0	Recommended value		V_{DD} –2.5		V_{DD}	V	V_0
Supply voltage (3)		V_2	Recommended value		2/9 V_{EE}			V	V_2
Supply voltage (4)		V_3	Recommended value				7/9 V_{EE}	V	V_3
Supply voltage (5)		V_5	Recommended value		V_{EE}		V_{EE} +2.5	V	V_5
Input high voltage		V_{IH}	V_{SS} = –2.7 to –5.5V		0.2•V_{SS}			V	EIO1, EIO2, FR, D0 to D3, YD, LP, SHL, DOFF, XSCL
Input low voltage		V_{IL}					0.8•V_{SS}	V	
Output high voltage		V_{OH}	V_{SS} = –2.7	I_{OH} = –0.6mA	V_{DD} –0.4			V	EIO1, EIO2
Output low voltage		V_{OL}	to –5.5 V	I_{OL} = 0.6mA			V_{DD} +0.4	V	
Input leakage current		I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$				2.0	µA	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O leakage current		$I_{LI/O}$	$V_{SS} \le V_{IN} \le V_{DD}$				5.0	µA	EIO1, EIO2
Static current		I_{SS}	V_5 = –20.0 to –10.0 V V_{IH} = V_{DD}, V_{IL} = V_{SS}				25	µA	V_{SS}
On resistance		R_{SEG}	ΔV_{ON} = 0.5 V, V_0 = V_{DD}, V_3 = 7/9•V_{EE}, V_2 = 2/9•V_{EE} V_{EE} = V_5 = –14.0 V			1.0	1.4	KΩ	X1 to X80
Average current consumption (1)	Data transfer mode	I_{DDT}	V_{SS} = –5.0 V, V_{IH} = V_{DD} V_{IL} = V_{SS}, f_{XSCL} = 4.0 MHz f_{LP} = 14 kHz, f_{FR} = 70 Hz Checkered pattern, non-burden V_{DD} = V_0 = 0V V_2 = –4 V V_3 = –16 V, V_{EE} = V_5 = –20 V			0.3	0.8	mA	V_{DD}
	Self-refresh mode	I_{DDS}	f_{XSCL} = 0 Hz = V_{SS} Another place is same as I_{DDT} item			70	200	µA	
Average current consumption (2)		I_{EE}	V_{SS} = –5.0 V, V_0 = 0.0 V V_2 = –4 V, V_3 = –16 V I_{EE} = V_5 = –20.0 V Another place is same as I_{DDT} item			25	70	µA	V_{EE}
Input capacitance		C_I	Freq. = 1 MHz, Ta = 25°C Simple substance of CHIP				8	pF	D_0 to D_3, LP, FR, YD, XSCL, SHL, DOFF
I/O capacitance		$C_{I/O}$					15	pF	EIO1, EIO2

AC Timing

Input timing



VSS = –5.0 V ±10%, Ta = –40 to 85°C

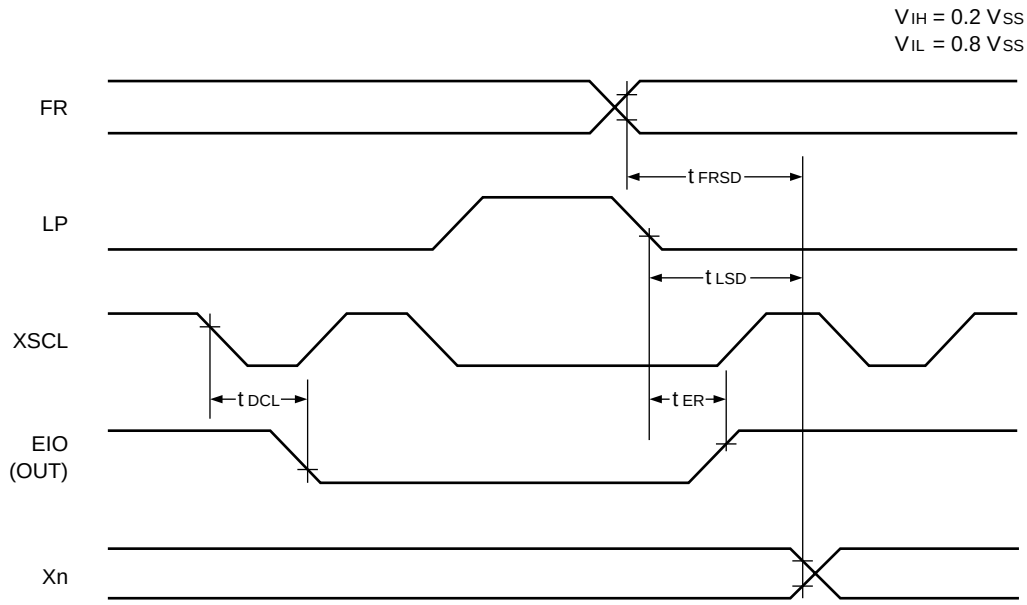
Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		150		ns
XSCL high level pulse width	t_{WCH}		30		ns
XSCL low level pulse width	t_{WCL}		30		ns
Data setup time	t_{DS}		20		ns
Data hold time	t_{DH}		15		ns
XSCL ↓ → LP ↓	t_{LD}		10		ns
LP ↓ → XSCL ↓	t_{LH}		70		ns
LP high level pulse width	t_{WLH}	*	40		ns
LP low level pulse width	t_{WLL}		600		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		35		ns
YD setup time	t_{YDS}		40		ns
YD hold time	t_{YDH}		40		ns
Rise/fall time	t_r, t_f			30	ns

VSS = –4.5 V to –2.7 V, Ta = –40 to 85°C

Item	Symbol	Condition	Min.	Max.	Unit
XSCL cycle time	t_C		250		ns
XSCL high level pulse width	t_{WCH}		70		ns
XSCL low level pulse width	t_{WCL}		70		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		50		ns
XSCL ↓ → LP ↓	t_{LD}		80		ns
LP ↓ → XSCL ↓	t_{LH}		140		ns
LP high level pulse width	t_{WLH}	*	75		ns
LP low level pulse width	t_{WLL}		1200		ns
FR phase difference	t_{DF}		–300	+300	ns
EIO setup time	t_{SUE}		50		ns
YD setup time	t_{YDS}		80		ns
YD hold time	t_{YDH}		80		ns
Rise/fall time	t_r, t_f			30	ns

*: Recommended t_{WLH} value = t_C

Output Timing



VDD = –5.0 ±10%, VEE = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF			90	ns
EIO output delay time	t_{DCL}	(EIO)	V_{SS} = –2.7 V		55	ns
LP → Xn output delay time	t_{LSD}	C_L = 100 pF			400	ns
FR → Xn output delay time	t_{FRSD}				400	ns

VDD = –4.5 V to –2.7 V, VEE = –8.0 to –20.0 V, Ta = –40 to 85°C

Item	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF			150	ns
EIO output delay time	t_{DCL}	(EIO)	V_{SS} = –2.7 V		95	ns
LP → Xn output delay time	t_{LSD}	C_L = 100 pF			800	ns
FR → Xn output delay time	t_{FRSD}				800	ns

LCD DRIVER POWER SUPPLY

Generating LCD Drive Voltages

To obtain individual voltage levels for LCD driver, register-split the potential between V_{EE} – V_{DD} and drive the LCD with the voltage follower using the operation amplifier. When using an operation amplifier, V_0 and V_{DD}, V_5 and V_{EE} are separated.

However, if the potential of V_0 is lower than V_{DD} potential or V_5 is higher than V_{EE} and the potential difference increases, the LCD driver capability decreases. To avoid this, set V_{DD} and V_0 or V_5 and V_{EE} within 0 V to 2.5 V. If an operation amplifier is not used, connect V_0 and V_{DD}, V_5 and V_{EE}.

If there are direct resistors on the V_{EE} (V_{DD}) power line, voltage falls in V_{EE} (V_{DD}) at the LSI power pins. This is caused by I_{DD} (I_{EE}) at the time of signal change. As a result, the relationship ($V_{DD} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{EE}$) for intermediate potential of LCD can not be maintained and the LSI may be damaged.

To insert a protective resistor, the voltage must be stabilized according to the capacity.

System Power-up

This LSI has high LCD drive voltage. As a result, if the logic power is being floated or if the V_{SS} voltage is kept above –2.5Vdc and high voltage is applied in the LCD driver, the LSI may be damaged because of the excess current.

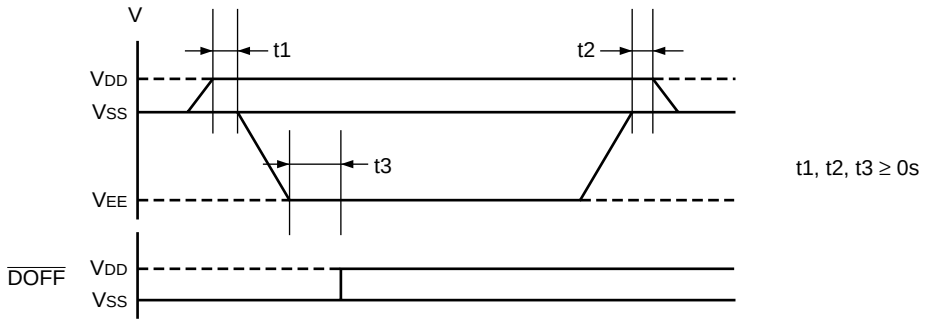
Until the LCD drive voltage is stabilized, use the display off function ($\overline{DOFF}$) to set the potential of the LCD drive output to V0 level.

Follow the sequence given below when turning the power on/off.

To turn on the power – Turn on the logic power
→ Turn the LCD driver on.
(On turn them on simultaneously.)

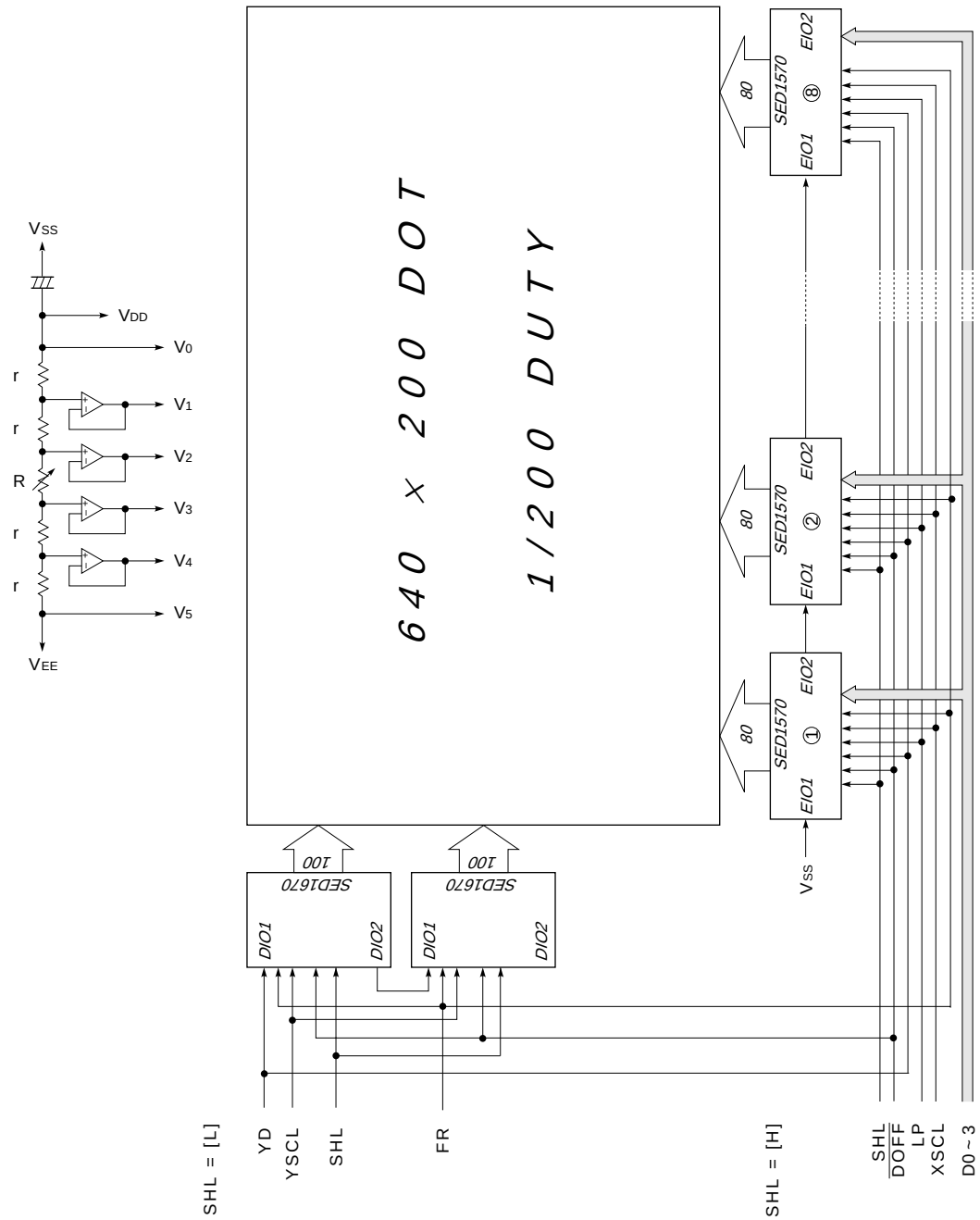
To turn off the power – Turn off the LCD driver
→ Turn off the logic power.
(Or turn them off simultaneously.)

To avoid excess current, insert the high-speed fuse in series with the LCD power. Select the appropriate value for a protective resistor according to the capacity of a LCD cell.



EXAMPLE OF APPLICATION

Constitution of LCD



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